ENGINEERING CONSULTING SERVICES

Technical Note: Composite Load and Distributed PV Model Validation in PSCAD™/EMTDC™ using SMIB System

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Contents

1 Introduction

The Power System Technology Centre (PTC), a division of Manitoba Hydro International Ltd. (MHI), was contacted by the Australian Energy Market Operator (AEMO) to validate composite load (CMLD) and distributed PV (DER) models [1][2] of the National Electricity Market (NEM) using PSCAD™/EMTDC™ platform. These models are validated by comparing simulation results obtained from seven PSS®E cases representing historical events in the NEM and high-speed measurements (HSM) recorded for the same historical events. AEMO had previously validated the PSS®E models against HSM taken from historical events [3].

As a precursor to the PSCAD™/EMTDC™ model validation using a wide area NEM system model, MHI has performed a comparison of PSCAD™/EMTDC™ model responses against PSS®E model responses using a Single Machine to Infinite Bus (SMIB) system. The SMIB based test results are presented in this technical note. In order to provide a range of system conditions, Short Circuit Ratio (SCR) and X/R ratio seen at the terminal changed from 3 to 10 and 3 to 14, respectively.

Section 2 and section 0 of this report discuss the DER and CMLD model verification tests, respectively. The test result plots are attached to this report as Appendix B.1, Appendix B.2 and Appendix C.

The tests were performed using PSS®E version 34.9.4 (Python version 3.9.13 32-bit) and PSCAD™/EMTDC™ version 4.6.3.

2 DER Model

2.1 Modified SMIB Model setup

In order to validate different parameter sets used in the DER model, four parameter sets used in the NEM case dated 22nd February 2021 were used. The DER SMIB type model in PSS®E platform is shown in Figure 1.

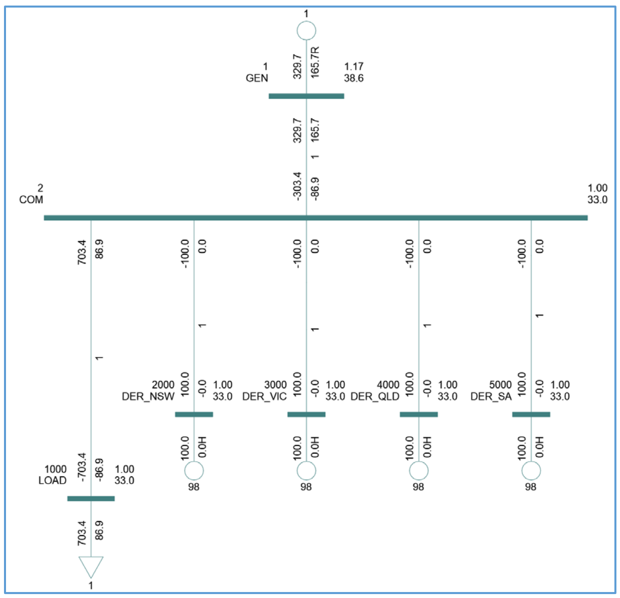


Figure 1: Modified SMIB model used in model validation - PSS®E

Four DER models representing the DER parameters of each area were connected to the common bus in parallel[1] to reduce the number of simulations. Following is a summary of the modified SMIB network set up in PSS®E.

- Bus 1 is the "grid" and is connected to the common bus through an equivalent impedance corresponding to the selected SCR and X/R ratio.
- There is a DER model for each area of mainland NEM connected to the common bus through a zero impedance line, each with an output of P = 100 MW and Q = 0 MVAr.
- A constant admittance load is connected to the common bus.
- The common bus voltage is controlled to 1.0 pu by setting an appropriate grid voltage.
- The machine at bus 1 is modeled using the "PLBVFU1" model. Disturbances are applied by either applying faults to the common bus or by applying a pre-determined bus voltage profile.
- The dynamic model parameters of the DER models were taken from a wide area NEM case dated 22nd February 2021. These parameters are listed in section 6.1.

[1] Alternatively, one DER model instant could be connected to the common bus while the other three model instants are out of service.

The DER SMIB model in PSCAD™/EMTDC™ platform is shown in Figure 2.

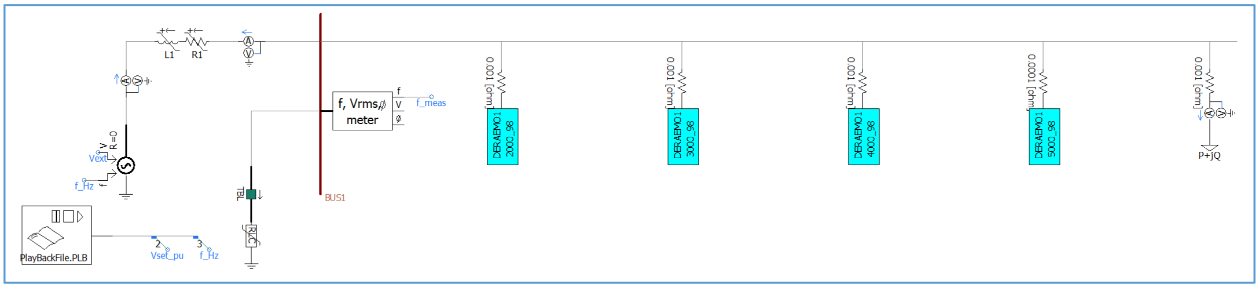


Figure 2: Modified SMIB model used in model validation - PSCAD™/EMTDC™

Following is a summary of the modified SMIB network set up in PSCAD™/EMTDC™.

- The test network is the same as the PSS®E model.
- Disturbances are applied by either playing back grid voltage and frequency from a file or applying a fault. A fault is applied by closing the breaker connected to the RLC component.
  - PSS®E cannot perform explicit unbalanced faults, but instead applies an equivalent three phase fault (i.e. connects a fixed shunt) with conductance (G) and susceptance (B) values calculated based on sequence data.
  - The fault resistance and inductance in the PSCAD™/EMTDC™ model are set based on the shunt element G and B values determined by PSS®E for the corresponding fault.
- The PSCAD™/EMTDC™ DER model has an additional "Phase angle trip" logic that is not present in the PSS®E model. The parameters of this additional phase angle trip logic are listed in section 6.1.1.

2.2 Disturbance List

The list of disturbances applied to the DER SMIB model is shown in Table 1 and Table 2. "Phase angle trip" logic is disabled in the PSCAD™/EMTDC™ DER model for nine tests tabulated in Table 1 so that the results can be compared with results obtained from PSS®E.

*Table 1: Disturbances applied to DER SMIB models – phase angle trip logic **disabled** in PSCAD™/EMTDC™ model*

Test No.	Test Description	Expected result
1	LG fault for 100 ms	Partial trip due to undervoltage
2	LLG fault for 100 ms	Partial trip due to undervoltage
3	3PH-G fault for 100 ms	Partial trip due to undervoltage
4	~115% Voltage disturbance for 2.5 s	Partial trip due to overvoltage
5	~120% Voltage disturbance for 500 ms	Full trip due to overvoltage
6	~80% Voltage disturbance for 1 sec	Partial trip due to undervoltage
7	51.5 Hz frequency step for 2.5 sec (4 Hz/s)	Partial trip due to overfrequency
8	48.5 Hz frequency step for 2.5 sec (4 Hz/s)	Partial trip due to underfrequency
9	49.1 Hz slow frequency ramp (0.5 Hz/s)	Partial trip due to ROCOF

“Phase angle trip” logic is enabled in the PSCAD™/EMTDC™ DER model for the four tests in Table 2. These tests were performed to show the accurate implementation of “Phase angle trip” in PSCAD™/EMTDC™ and the impact on the active power output during the post-fault window. The settings of the phase angle trip logic are given in section 6.1.1.

*Table 2: Disturbances applied to DER SMIB models – phase angle trip logic **enabled** in PSCAD™/EMTDC™ model*

Test No.	Test Description	Expected result
10	20° phase angle step	15 MW trip for each DER due to >15° phase angle step in PSCAD™/EMTDC™ model (i.e., 85% of 100 MW = 85 MW remaining). No trip in PSS®E model.
11	40° phase angle step	23 MW trip for each DER due to >30° phase angle step in PSCAD™/EMTDC™ model (i.e., 77% of 100 MW = 77 MW remaining). No trip in PSS®E model.
12	60° phase angle step	38 MW trip for each DER due to >45° phase angle step in PSCAD™/EMTDC™ model (i.e., 62% of 100 MW = 62 MW remaining). No trip in PSS®E model.
13	120° phase angle step	54 MW trip for each DER due to >90° phase angle step in PSCAD™/EMTDC™ model (i.e., 46% of 100 MW = 46 MW remaining). No trip in PSS®E model.

Note: The above tests were repeated for all combinations of the SCR values of 3 and 10 and X/R values of 3 and 14 (i.e., four combinations).

2.3 Results

2.3.1 Results with phase angle trip logic disabled

The results for the DER tests with phase angle trip logic disabled are shown in Appendix B.1. The pre-contingency steady-state terminal active and reactive powers are identical between the PSS®E and PSCAD™/EMTDC™ models. However, there are differences in active and reactive power output of the PSS®E and PSCAD™/EMTDC™ models during and after the disturbance. These differences are a result of the minor modeling differences between PSS®E and PSCAD™/EMTDC™ models. A summary of these differences for tests 1-9 is shown in Table 3.

Table 3: DER SMIB test results – phase angle trip logic disabled

Test No.	Test	SCR	X/R	Result	
				Active Power	Reactive Power
1	LG fault for 100 ms	3	3	Mismatch ~1 MW each[b]	Mismatch during transient[a]
		3	14	Mismatch ~2 MW each[b]	
		10	3	Good match	
		10	14	Good match	
2	LLG fault for 100 ms	3	3	Good match	
		3	14	Good match	
		10	3	Good match	
		10	14	Good match	
3	3PH-G fault for 100 ms	3	3	Mismatch ~7 MW each[c]	
		3	14	Mismatch ~5 MW each[c]	
		10	3	Mismatch ~4 MW each[c]	
		10	14	Mismatch ~1 MW each[c]	
4	~115% Voltage disturbance for 2.5 sec	3	3	Good match	
		3	14	Good match	
		10	3	Good match	
		10	14	Good match	
5	~120% Voltage disturbance for 500 ms	3	3	Good match	
		3	14	Good match	
		10	3	Good match	
		10	14	Good match	
6	~80% Voltage disturbance for 1 sec	3	3	Mismatch ~ 2 MW each[b]	
		3	14	Mismatch ~ 2 MW each[b]	
		10	3	Mismatch ~ 2 MW each[b]	
		10	14	Mismatch ~ 2 MW each[b]	
7	51.5 Hz frequency step for 2.5 sec (4 Hz/sec)	3	3	Good match	
		3	14	Good match	
		10	3	Good match	
		10	14	Good match	
8	48.5 Hz frequency step for 2.5 sec (4 Hz/sec)	3	3	Good match	
		3	14	Good match	
		10	3	Good match	
		10	14	Good match	

Test No.	Test	SCR	X/R	Result	
				Active Power	**Reactive Power**
9	49.1 Hz slow frequency ramp (0.5 Hz/sec)	3	3	Good match	Mismatch during transient[a]
		3	14	Good match	
		10	3	Good match	
		10	14	Good match	

[a]The reactive power output of the DER model showed mismatches during transients since the PSCAD™/EMTDC™ model includes PLL and dq-decoupling controller dynamics. The PSS®E model performs a direct current injection using a known internal phase angle. The mismatch in transient reactive power is larger for SCR = 3 than for SCR = 10, and larger for X/R = 3 than for X/R = 14.

[b]Since the terminal voltage is between 'vl0' and 'vl1' [3] during the disturbance (about 0.8 pu), the amount of DER that trips depends on the voltage measured at the time of 'tvl1' (about 34 ms) after voltage drops below 'vl1' (0.9 pu). The voltage measurement at this moment is slightly different between PSCAD™/EMTDC™ and PSS®E models, leading to slightly different undervoltage tripping amounts. For test #1 (LG fault), this difference is higher for X/R = 14 than for X/R = 3.

[c]The PSS®E model experiences a large frequency spike upon inception of the three-phase-to-ground fault (a well-known phenomenon for solid faults in PSS®E) that activates the frequency droop control causing 'Pord' [3] to decrease. Since 'dPmax' = 0, 'Pord' does not return to its initial value after clearing the disturbance. The PSCAD™/EMTDC™ model does not experience this frequency spike; therefore, 'Pord' does not decrease. The response of the PSCAD™/EMTDC™ model is more realistic than the PSS®E model response. The mismatch increases as SCR decreases and as X/R decreases. A further discussion of this result is given in section 7.

2.3.2 Results with phase angle trip logic enabled

The result plots for the DER tests with phase angle trip logic enabled are shown in Appendix B.2. The pre-contingency steady-state terminal active and reactive powers are identical between the PSS®E and PSCAD™/EMTDC™ models. However, as expected, there are differences in active and reactive power output of the PSS®E and PSCAD™/EMTDC™ models during and after the disturbance. A summary of these differences for tests 10-13 is shown in Table 4, as well as the expected and actual MW trip due to the phase angle trip logic.

Table 4: DER SMIB test results – phase angle trip logic enabled

Test No.	Test	SCR	X/R	MW Trip (each)		Comparison between PSS®E and PSCAD™/EMTDC™	
				Expected	Actual PSCAD™/EMTDC™	Active Power	Reactive Power
10	20° phase angle step	3	3	15	15	DER trip in PSCAD™/EMTDC™ matches with the expected value. DER active power reduction in PSS®E has a mismatch ranging from 10 MW to 20 MW[a].	Mismatch during transient[b]
		3	14		15		
		10	3		15		
		10	14		15		
11	40° phase angle step	3	3	23	23		
		3	14		23		
		10	3		23		
		10	14		23		
12	60° phase angle step	3	3	38	38		
		3	14		38		
		10	3		38		
		10	14		38		
13	120° phase angle step	3	3	54	54		
		3	14		54		
		10	3		54		
		10	14		54		

[a]There is a mismatch in the active power output of the DER model since the PSCAD™/EMTDC™ model includes an additional "Phase angle trip" logic and the PSS®E model does not. When the phase angle is stepped for the test, it is equivalent to applying a momentary frequency spike from the grid (i.e., since the frequency is the first derivative of the phase angle). The PSS®E model experiences this frequency spike when the phase angle is stepped, which activates the frequency droop control causing 'Pord' to decrease. Since 'dPmax' = 0, 'Pord' does not return to its initial value after clearing the disturbance. In contrast, the PSCAD™/EMTDC™ model includes an improved frequency measurement model that does not produce large spikes in frequency when the phase angle is stepped, enabling the PSCAD™/EMTDC™ model to avoid providing a frequency droop response when there is a sudden phase angle step. Due to the difference in tripping amount between PSS®E and PSCAD™/EMTDC™ models, the net load connected to the common bus is different, leading to different common bus voltage (based on the network SCR and X/R).

[b]The reactive power output of the DER model shows mismatches during transients, as shown in Figure 3. The PSCAD™/EMTDC™ model includes PLL and dq-decoupling controller dynamics while the PSS®E model performs a direct current injection using a known internal phase angle. Therefore, these differences are expected (i.e., due to the difference in EMT and RMS simulation platforms).

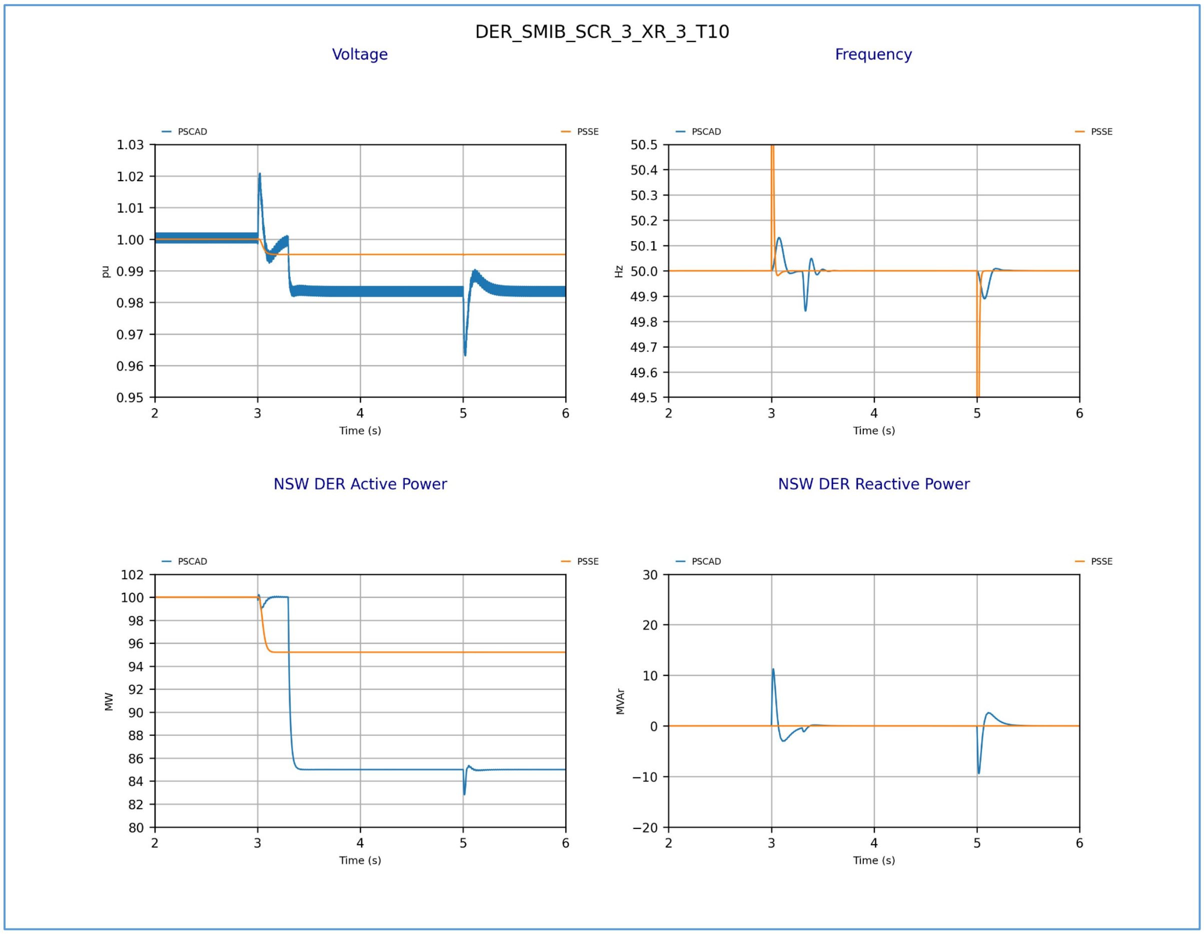


Figure 3: NSW DER response, Test No. 10, SCR = 3, X/R = 3

As shown in Figure 3, the PSCAD™/EMTDC™ model shows a transient in reactive power when the phase shift disturbance is applied and again when the phase shift disturbance is cleared, whereas the PSS®E model outputs 0 MVAr throughout.

3 CMLD Model

3.1 Modified SMIB Model setup

The CMLD model was updated as discussed in section 8. In order to validate different parameter sets used for the CMLD model, various parameter sets used in the NEM cases were used. The CMLD SMIB type model in PSS®E platform is shown in Figure 4.

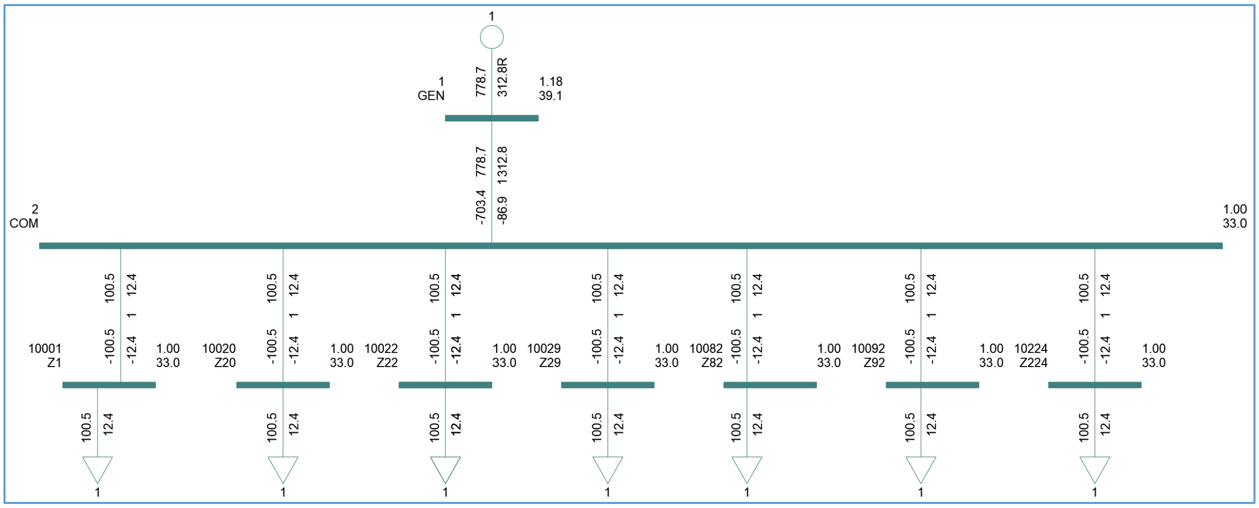


Figure 4: Modified SMIB model used in model validation - PSS®E

Seven CMLD models representing CMLD parameters of different zones were connected to the common bus in parallel[2] to reduce the number of simulations. Following is a summary of the modified SMIB network set up in PSS®E.

- Bus 1 is the "grid" and is connected to the common bus through an equivalent impedance corresponding to the selected SCR and X/R ratio.
- There is a CMLD model for each of the seven (7) zones connected to the common bus through a zero impedance line, each with a constant power load of P = 100.49 MW and Q = 12.42 MVAr.
- The common bus voltage is controlled to 1.0 pu by setting an appropriate grid voltage.
- The machine at bus 1 is modeled using the "PLBVFU1" model. Disturbances are applied by either applying faults to the common bus or playing back grid voltage and frequency from a file.
- The dynamic parameters for the CMLD models are listed in section 6.2.

[2] Alternatively, one CMLD model instance could be connected to the common bus while the other six model instances are out of service.

The CMLD SMIB model in PSCAD™/EMTDC™ platform is shown in Figure 5.

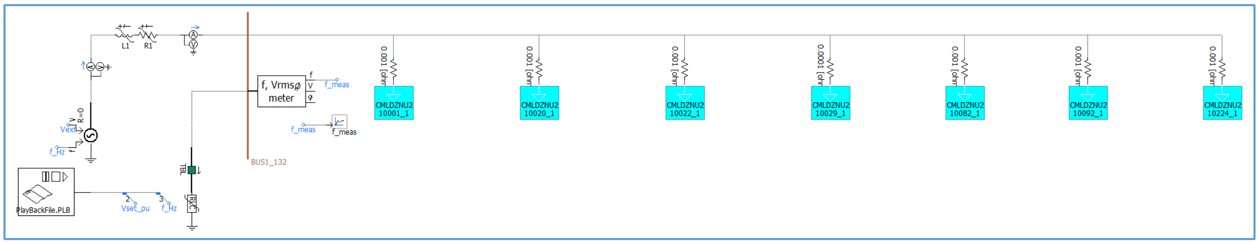


Figure 5: Modified SMIB model used in model validation - PSCAD™/EMTDC™

Following is a summary of the modified SMIB network set up in PSCAD™/EMTDC™.

- The modified SMIB network is comparable to the PSS®E model.
- Disturbances are applied by either applying faults (by closing the TBL breaker onto the RL component) or playing back grid voltage and frequency from a file.
  - PSS®E cannot perform true unbalanced faults, instead connecting a fixed shunt element with conductance (G) and susceptance (B) values that approximate the unbalanced fault.
  - The fault resistance and inductance in the PSCAD™/EMTDC™ model are set based on the shunt element G and B values determined by PSS®E for the corresponding fault.

3.2 Disturbance List

The list of disturbances applied to the CMLD SMIB model is shown in Table 5.

Table 5: Disturbances applied to CMLD SMIB models

Test No.	Test Description	Expected result
2	LLG fault for 100 ms	Partial trip due to undervoltage
3	3PH-G fault for 100 ms	Partial trip due to undervoltage
4	~115% Voltage disturbance for 2.5 s	Loads remain connected
5	~120% Voltage disturbance for 500 ms	Loads remain connected
6	~80% Voltage disturbance for 1 sec	Partial trip due to undervoltage
7	51.5 Hz frequency step for 2.5 sec (4 Hz/s)	Loads remain connected
8	48.5 Hz frequency step for 2.5 sec (4 Hz/s)	Loads remain connected
9	49.1 Hz slow frequency ramp (0.5 Hz/s)	Loads remain connected

Note: The tests are repeated for all combinations of the SCR values of 3 and 10 and X/R values of 3 and 14 (i.e., four combinations). LG fault is not applied to the CMLD SMIB model due to the absence of zero sequence impedance information in the PSS®E case.

3.3 Results

The result plots for the CMLD tests are shown in Appendix C. The pre-contingency steady-state terminal active and reactive power are nearly identical between the PSS®E and PSCAD™/EMTDC™ models. However, there are differences in active and reactive power output of the PSS®E and PSCAD™/EMTDC™ models during and after the disturbance. These differences are a result of the minor modeling differences between PSS®E and PSCAD™/EMTDC™ models. A summary of these differences for tests 2-9 is shown in Table 6.

Table 6: CMLD SMIB test results

Test No.	Test	SCR	X/R	Result	
				Active Power	**Reactive Power**
2	LLG fault for 100 ms	3	3	Good match	Mismatch during transient[a]
		3	14	Good match	Mismatch during transient[a]
		10	3	Z20/Z29 mismatch ~5 MW[b]	Mismatch during transient[a]. Z20/Z29 mismatch ~5 MVAr[2]
		10	14	Good match	Mismatch during transient[a]
3	3PH-G fault for 100 ms	3	3	Good match	Mismatch during transient[a]
		3	14	Good match	Mismatch during transient[a]
		10	3	Good match	Mismatch during transient[a]
		10	14	Good match	Mismatch during transient[a]
4	~115% Voltage disturbance for 2.5 sec	3	3	Good match	Good match
		3	14	Good match	Good match
		10	3	Good match	Good match
		10	14	Good match	Good match
5	~120% Voltage disturbance for 500 ms	3	3	Good match	Good match
		3	14	Good match	Good match
		10	3	Good match	Good match
		10	14	Good match	Good match
6	~80% Voltage disturbance for 1 sec	3	3	Z92 mismatch increases ~1.5 MW[c]	Z92 mismatch increases ~2 MVAr[c]
		3	14	Z82 mismatch increases ~1.5 MW[c]	Good match
		10	3	Good match	Good match
		10	14	Good match	Good match
7	51.5 Hz frequency step for 2.5 sec (4 Hz/sec)	3	3	Good match	Good match
		3	14	Good match	Good match
		10	3	Good match	Good match
		10	14	Good match	Good match
8	48.5 Hz frequency step for 2.5 sec (4 Hz/sec)	3	3	Good match	Good match
		3	14	Good match	Good match
		10	3	Good match	Good match
		10	14	Good match	Good match
9	49.1 Hz slow frequency ramp (0.5 Hz/sec)	3	3	Good match	Mismatch during transient[d]
		3	14	Good match	Mismatch during transient[d]
		10	3	Good match	Mismatch during transient[d]
		10	14	Good match	Mismatch during transient[d]

[a]The PSS®E model shows larger spikes in reactive power just after fault inception and fault clearance than the PSCAD™ model. These spikes in reactive power are due to sudden changes in the voltage. If a measurement filter of 20 ms (same as the PSCAD™ model) is applied to the PSS®E response, the reactive power response matches well between the PSS®E and PSCAD™ models as shown in Figure 6.

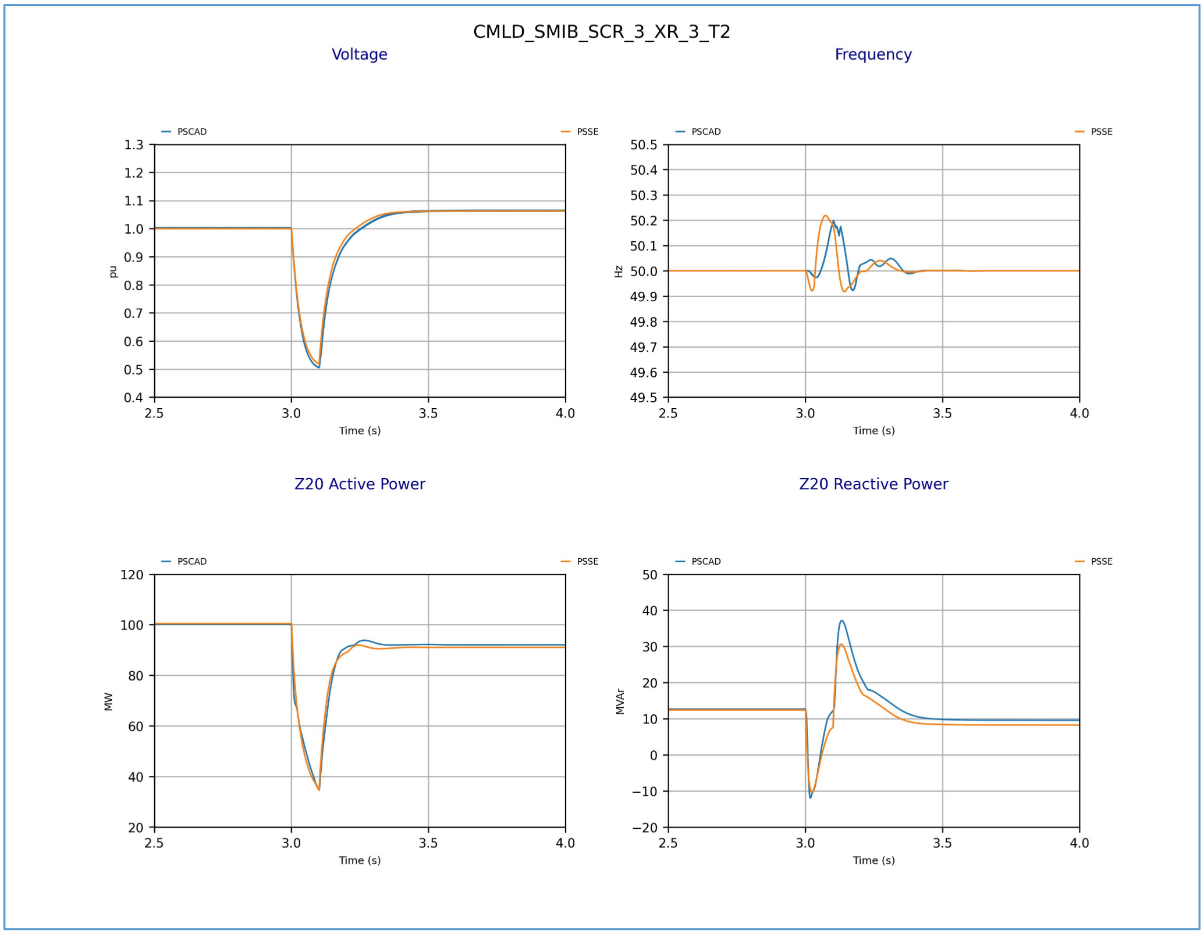


Figure 6: Zone 20 total active and reactive power response with 20 ms filtering for all PSS®E traces, Test No. 2, SCR = 3, X/R = 3

[b]During the fault, the load bus voltage drops just below Motor D stall threshold of Vstall = 0.49 pu. The Motor D stall after delay time 'Tstall' = 40 ms. Due to the measurement time constant[3] in PSCAD™/EMTDC™, the voltage measurement in the PSCAD™/EMTDC™ model only spends 30 ms below the threshold of 0.49 pu before the fault is cleared, whereas the measured voltage in the PSS®E model spends > 40 ms below the threshold. Therefore, Motor D stalls in the PSS®E model but not in the PSCAD™/EMTDC™ model, as shown in Figure 7.

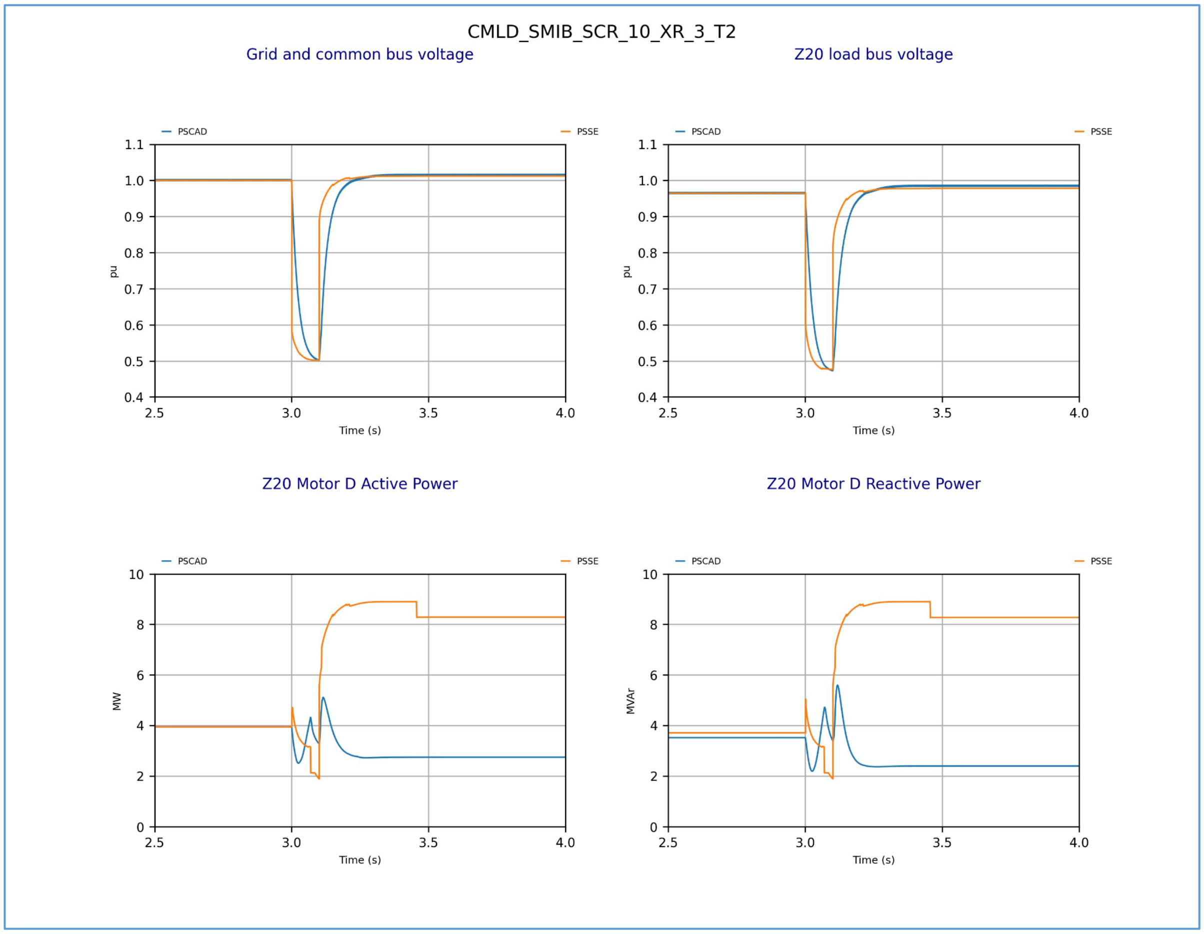


Figure 7: Zone 20 Motor D response, Test No. 2, SCR = 10, X/R = 3

[3] Voltage measurement smoothing time constant in the PSCAD™/EMTDC™ represents actual voltage measurement delay.

[c]Motor A trips 'Ftr1' = 10% on Undervoltage (voltage less than 'Vtr1' = 0.75 pu for 'Ttr1' = 60 ms) in PSCAD™/EMTDC™ and not in PSS®E since the load bus voltage is marginally below the threshold of 0.75 pu in the PSCAD™/EMTDC™ model (about 0.744 - 0.748 pu) and marginally above the threshold of 0.75 pu in the PSS®E model (about 0.752 - 0.755 pu).

Differences due to signals being marginally close to a tripping threshold have to be expected. This would only impact local load trip percentages and is unlikely to impact system-level dynamic response conclusions.

[d]There are differences in the reactive power responses, especially for zones 20 and 82, where the PSS®E and PSCAD™ reactive power move in opposite directions, as shown in Figure 8. The differences are marginal (the deviation in Q is very small and should not be used to make conclusions on the overall trend and will not impact overall system dynamic response conclusions).

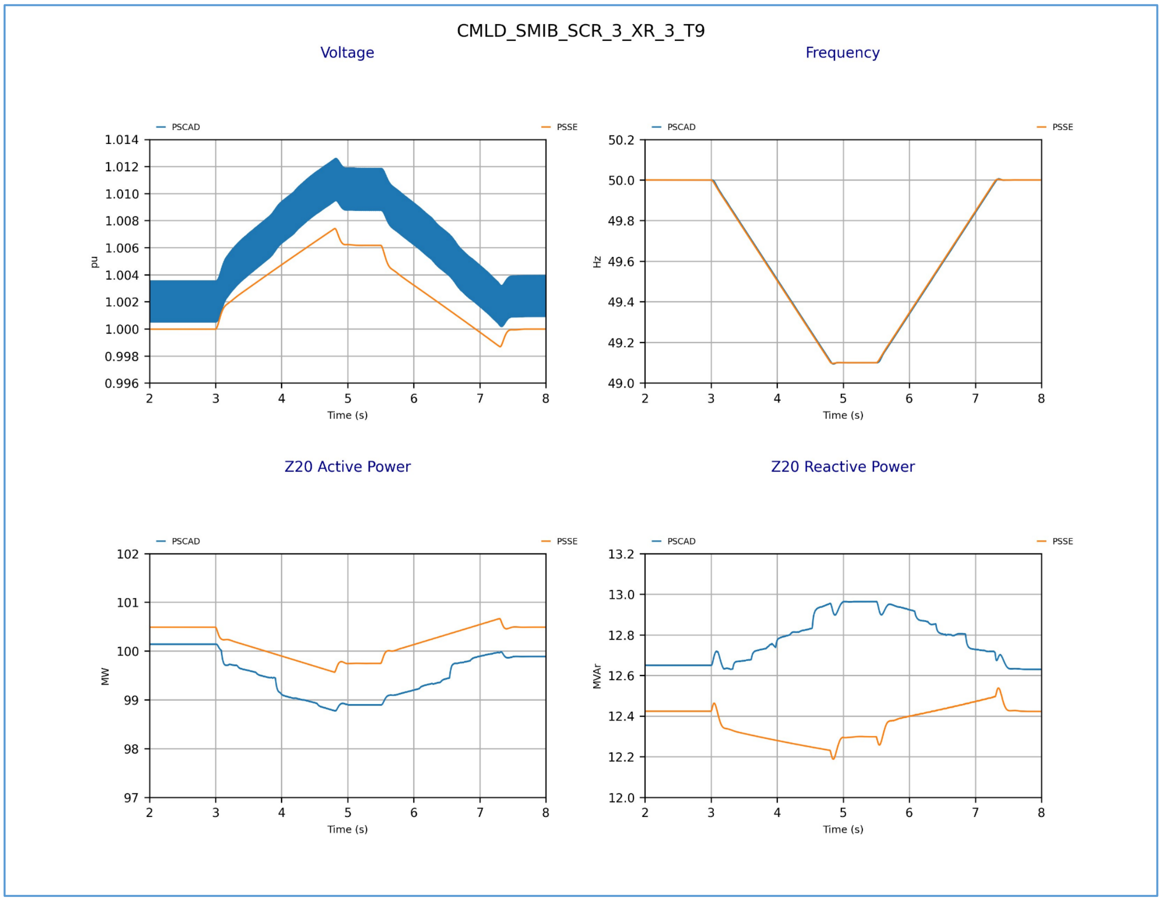


Figure 8: Zone 20 total active and reactive power response, Test No. 2, SCR = 3, X/R = 3

This is due to the network frequency dependence not enabled in the PSS®E simulation parameters.

Figure 9 shows the comparison of zone 20 active and reactive power with the network frequency dependence enabled in the PSS®E dynamic simulation settings.

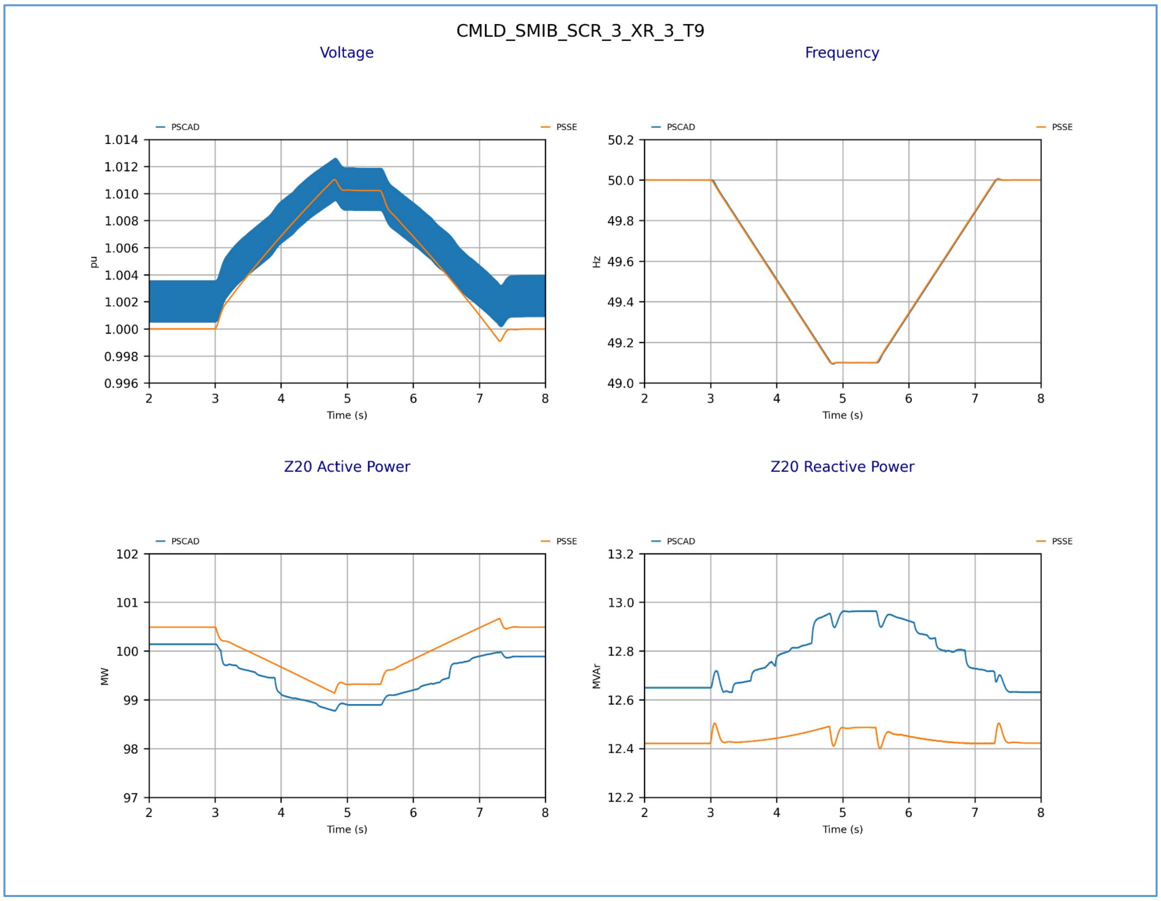


Figure 9: Zone 20 total active and reactive power response with network frequency dependence in PSS®E model, Test No. 2, SCR = 3, X/R = 3

The reactive power response of zone 20 in the PSS®E model now moves in the same direction as the PSCAD™ model.

4 Conclusions

- The pre-contingency steady-state active and reactive power output of the PSCAD™/EMTDC™ models match closely with that of the PSS®E models.
- The PSCAD™/EMTDC™ model behaviour during and after the tested disturbances match closely with that of the PSS®E models except for the following situations:
    - DER model:
        - The reactive power output of the DER model shows mismatches during transients since the PSCAD™/EMTDC™ model includes PLL and dq-decoupling controller dynamics which are absent in the PSS®E model.
        - LG fault with SCR = 3 or 80% voltage disturbance – Since the terminal voltage measurement in the models is slightly different during the fault, there are slightly different undervoltage tripping amounts.
        - 3PH-G fault – The PSS®E model experiences a large frequency spike upon inception of the three-phase-to-ground fault leading to reduced active power output.
        - Phase angle steps – The PSCAD™/EMTDC™ model has an additional "Phase angle trip" logic that is not present in the PSS®E model. The PSS®E model experiences large frequency spikes when the phase angle is stepped leading to reduced active power output.

  The differences listed above are unlikely to have a material impact on overall system study conclusions.
    - CMLD model:
        - LG faults and LLG faults show larger reactive power spikes in the PSS®E model than in the PSCAD™ model.
        - LLG fault with SCR = 10 and X/R = 3 – Motor D stalls in the PSS®E model but not in the PSCAD™/EMTDC™ model due to differences in the voltage measurement signal filtering.
        - 80% voltage disturbance with SCR = 3 – Motor A trips 10% on undervoltage in PSCAD™/EMTDC™ and not in PSS®E since the load bus voltage is marginally below the threshold of 0.75 pu in the PSCAD™/EMTDC™ model (about 0.744 - 0.748 pu) and marginally above the threshold of 0.75 pu in the PSS®E model (about 0.752 - 0.755 pu).
        - Small difference in reactive power response during frequency disturbances due to disabled network frequency dependence PSS®E dynamic simulation option.

  The differences listed above are unlikely to have a material impact on overall system study conclusions.

5 References

[1] "Distributed Energy Resource (DER) PSCAD model User Guide", MHI, January 2021.
[2] "Composite Load CMLDZNU2 PSCAD model User Guide", MHI, January 2021.
[3] "PSS®E models for load and distributed PV: Model development and validation", AEMO, November 2022.

6 Appendix A: Dynamic Model Parameters

6.1 DER Model

The ICONs and CONs of the DER model for each area of mainland NEM are listed in Table 7 and Table 8, respectively.

Table 7: DER model ICONs

ICONs	Name	Area			
		NSW	VIC	QLD	SA
M	PF Flag	1	1	1	1
M+1	Freq Flag	1	1	1	1
M+2	PQ Flag	1	1	1	1
M+3	Gen Flag	1	1	1	1
M+4	Vtrip Flag	1	1	1	1
M+5	Ftrip Flag	1	1	1	1

Table 8: DER model CONs

CONs	Name	Area			
		NSW	VIC	QLD	SA
J	Trv (s)	0.02	0.02	0.02	0.02
J+1	Trf (s)	0.02	0.02	0.02	0.02
J+2	dbd1 (pu)	-0.0435	-0.0435	-0.0435	-0.0435
J+3	dbd2 (pu)	0.0717	0.0478	0.0435	0.0783
J+4	Trocof (s)	0.02	0.02	0.02	0.02
J+5	Vref0 (pu)	1	1	1	1
J+6	Tp (s)	0.02	0.02	0.02	0.02
J+7	Tiq (s)	0.02	0.02	0.02	0.02
J+8	Ddn(pu)	7.0898	6.7409	6.1639	6.0622
J+9	Dup (pu)	0	0	0	0
J+10	fdbd1 (pu)	-0.005	-0.005	-0.005	-0.005
J+11	fdbd2 (pu)	1	1	1	1
J+12	femax (pu)	99	99	99	99
J+13	femin (pu)	-99	-99	-99	-99
J+14	PMAX (pu)	1	1	1	1
J+15	PMIN (pu)	0	0	0	0
J+16	dPmax (pu/s)	0	0	0	0
J+17	dPmin (pu/s)	-99	-99	-99	-99
J+18	Tpord (s)	0.02	0.02	0.02	0.02
J+19	Kpg (pu)	0	0	0	0
J+20	Kig (pu)	10	10	10	10
J+21	Imax (pu)	1.199	1.1984	1.1974	1.1972
J+22	vl0 (pu)	0.5728	0.5815	0.5959	0.5984
J+23	vl1 (pu)	0.9	0.9	0.9	0.9
J+24	vh0 (pu)	1.18	1.18	1.18	1.18
J+25	vh1 (pu)	1.1304	1.1304	1.1304	1.1304

CONs	Name	Area			
		NSW	VIC	QLD	SA
J+26	tvl0 (s)	1.7126	1.7062	1.6957	1.6938
J+27	tvl1 (s)	0.0343	0.034	0.0334	0.0333
J+28	tvh0 (s)	0.3687	0.3938	0.4354	0.4427
J+29	tvh1 (s)	1.894	1.8965	1.9005	1.9012
J+30	vrfrac	0.6874	0.6843	0.6792	0.6783
J+31	Kqv1 (pu)	0	0	0	0
J+32	Kqv2 (pu)	0	0	0	0
J+33	-	0	0	0	0
J+34	-	0	0	0	0
J+35	Tg (s)	0.02	0.02	0.02	0.02
J+36	rrpwr (pu/s)	10	10	10	10
J+37	Tv (s)	0.02	0.02	0.02	0.02
J+38	Vpr (pu)	0.9	0.9	0.9	0.9
J+39	Iqh1 (pu)	0.252	0.1521	0.1239	0.1635
J+40	Iql1 (pu)	-0.252	-0.1521	-0.1239	-0.232
J+41	fl1 (Hz)	49.6	49.6	49.6	49.6
J+42	fl2 (Hz)	49.01	49.01	49.01	49.01
J+43	fl3 (Hz)	49	49	49	49
J+44	fl4 (Hz)	49	49	49	49
J+45	fl5 (Hz)	49	49	49	49
J+46	fl6 (Hz)	48.52	48.52	48.52	48.52
J+47	fl7 (Hz)	47.6	47.6	47.6	47.6
J+48	fl8 (Hz)	47.55	47.55	47.55	47.55
J+49	fl9 (Hz)	47.5	47.5	47.5	47.5
J+50	fl10 (Hz)	47.1	47.1	47.1	47.1
J+51	fl11 (Hz)	47	47	47	47
J+52	fl12 (Hz)	47	47	47	47
J+53	fl13 (Hz)	47	47	47	47
J+54	tfl1 (s)	1.9	1.9	1.9	1.9
J+55	tfl2 (s)	0.18	0.18	0.18	0.18
J+56	tfl3 (s)	0.06	0.06	0.06	0.06
J+57	tfl4 (s)	1.96	1.96	1.96	1.96
J+58	tfl5 (s)	2	2	2	2
J+59	tfl6 (s)	2	2	2	2
J+60	tfl7 (s)	1.8	1.8	1.8	1.8
J+61	tfl8 (s)	0.2	0.2	0.2	0.2
J+62	tfl9 (s)	1.8	1.8	1.8	1.8
J+63	tfl10 (s)	1.8	1.8	1.8	1.8
J+64	tfl11 (s)	1.6	1.6	1.6	1.6
J+65	tfl12 (s)	0.1	0.1	0.1	0.1
J+66	tfl13 (s)	1.6469	1.6469	1.6469	1.6469
J+67	frac_fl1	0.0129	0.0133	0.0138	0.0139
J+68	frac_fl2	0.0126	0.0274	0.0147	0.0101
J+69	frac_fl3	0.0827	0.0884	0.0638	0.0668
J+70	frac_fl4	0.0252	0.0547	0.0236	0.0176
J+71	frac_fl5	0.0006	0.0019	0.0006	0.0019

CONs	Name	Area			
		NSW	VIC	QLD	SA
J+72	frac_fl6	0.0084	0.0033	0.0055	0.0063
J+73	frac_fl7	0.0529	0.0225	0.0131	0.0223
J+74	frac_fl8	0.0187	0.0146	0.0166	0.0286
J+75	frac_fl9	0.0523	0.0345	0.0726	0.0307
J+76	frac_fl10	0.0594	0.061	0.1301	0.0537
J+77	frac_fl11	0.009	0.0119	0.0055	0.0056
J+78	frac_fl12	0.3144	0.3328	0.3348	0.4425
J+79	frac_fl13	0.3509	0.3337	0.3051	0.3001
J+80	fh1 (Hz)	50.5	50.5	50.5	50.5
J+81	fh2 (Hz)	50.8	50.8	50.8	50.8
J+82	fh3 (Hz)	51	51	51	51
J+83	fh4 (Hz)	51	51	51	51
J+84	fh5 (Hz)	51	51	51	51
J+85	fh6 (Hz)	51.58	51.58	51.58	51.58
J+86	fh7 (Hz)	51.9	51.9	51.9	51.9
J+87	fh8 (Hz)	52	52	52	52
J+88	fh9 (Hz)	52	52	52	52
J+89	fh10 (Hz)	52.45	52.45	52.45	52.45
J+90	fh11 (Hz)	52.9	52.9	52.9	52.9
J+91	fh12 (Hz)	53	53	53	53
J+92	fh13 (Hz)	53	53	53	53
J+93	tfh1 (s)	1.9	1.9	1.9	1.9
J+94	tfh2 (s)	1.9	1.9	1.9	1.9
J+95	tfh3 (s)	0.06	0.06	0.06	0.06
J+96	tfh4 (s)	1.96	1.96	1.96	1.96
J+97	tfh5 (s)	2	2	2	2
J+98	tfh6 (s)	2	2	2	2
J+99	tfh7 (s)	1.8	1.8	1.8	1.8
J+100	tfh8 (s)	1.6	1.6	1.6	1.6
J+101	tfh9 (s)	1.8	1.8	1.8	1.8
J+102	tfh10 (s)	0.2	0.2	0.2	0.2
J+103	tfh11 (s)	1.8	1.8	1.8	1.8
J+104	tfh12 (s)	0.1	0.1	0.1	0.1
J+105	tfh13 (s)	0.1515	0.1515	0.1515	0.1515
J+106	frac_fh1	0.0452	0.0464	0.0484	0.0488
J+107	frac_fh2	0.0216	0.023	0.0253	0.0258
J+108	frac_fh3	0.0606	0.0781	0.0388	0.0359
J+109	frac_fh4	0.0185	0.0483	0.0144	0.0095
J+110	frac_fh5	0.0004	0.0017	0.0004	0.001
J+111	frac_fh6	0.0084	0.0033	0.0055	0.0063
J+112	frac_fh7	0.0529	0.0225	0.0131	0.0223
J+113	frac_fh8	0.009	0.0119	0.0166	0.0286
J+114	frac_fh9	0.0523	0.0345	0.0726	0.0307
J+115	frac_fh10	0.0187	0.0146	0.1301	0.0537
J+116	frac_fh11	0.0594	0.061	0.0055	0.0056
J+117	frac_fh12	0.3144	0.3328	0.3348	0.4425

CONs	Name	Area			
		NSW	VIC	QLD	SA
J+118	frac_fh13	0.3385	0.3219	0.2943	0.2895
J+119	RoCoF_1 (Hz/s)	0.008	0.008	0.008	0.008
J+120	RoCoF_2 (Hz/s)	0.02	0.02	0.02	0.02
J+121	RoCoF_3 (Hz/s)	0.08	0.08	0.08	0.08
J+122	tRoCoF_1	1.41	1.41	1.41	1.41
J+123	tRoCoF_2	0.825	0.825	0.825	0.825
J+124	tRoCoF_3	0.29	0.29	0.29	0.29
J+125	frac_RoCOF_1	0.0372	0.036	0.0408	0.0353
J+126	frac_RoCOF_2	0.0437	0.0462	0.0983	0.0449
J+127	frac_RoCOF_3	0	0	0	0

6.1.1 Parameters of additional phase angle trip logic in the PSCAD™/EMTDC™ model

In the PSCAD™/EMTDC™ model, there is an additional phase angle trip logic that is not present in the PSS®E model. The phase angle trip settings (provided by AEMO) are hard-coded into the PSCAD™/EMTDC™ model and are the same for all areas (i.e., the settings are the same for NSW, VIC, QLD and SA). The phase angle trip settings are listed in Table 9.

Table 9: DER model phase angle trip settings (PSCAD™/EMTDC™ model only)

Trip level	Phase angle step threshold	DER remaining after trip
1	15°	85%
2	30°	77%
3	45°	62%
4	90°	46%

6.2 CMLD Model

The CMLD model CONs for each zone are listed in Table 10.

Table 10: CMLD model CONs

CONs	Name	Zone						
		Z1	Z20	Z22	Z29	Z82	Z92	Z224
J	Load base for xfr & feeder, MVA or calculated if <= 0	-0.8	-0.8	-0.8	-0.8	-0.8	-0.8	-0.8
J+1	Substation compensation B, pu on load base	0	0	0	0	0	0	0
J+2	Rfdr - Feeder resistance, pu on load base	0.04	0.04	0	0.04	0.01	0.01	0.01
J+3	Xfdr - Feeder reactance, pu on load base	0.04	0.04	0	0.04	0.01	0.01	0.01
J+4	Fb - Not used, Fb = 0.0	0.75	0.75	0.75	0.75	0.75	0.75	0.75
J+5	Xxf - Transformer reactance, pu on load base	0.08	0	0.06	0.08	0	0.08	0.08
J+6	Tfixhs - High side fixed transformer tap	1	1	1	1	1	1	1
J+7	Tfixls - Low side fixed transformer tap	1	1	1	1	1	1	1
J+8	LTC - LTC flag (1=active, 0=inactive)	1	0	0	1	0	1	1
J+9	Tmin - LTC min tap (on low side)	0.9	0.9	1	0.9	0.9	0.9	0.9
J+10	Tmax - LTC max tap (on low side)	1.1	1.1	1	1.1	1.1	1.1	1.1
J+11	Step - LTC Tstep (on low side)	0.0063	0.0062	0.0062	0.0062	0.0062	0.0062	0.0063
J+12	Vmin - Min value of V target range on xfr low side	1	1	1	1	1	1	1
J+13	Vmax - Max value of V target range on xfr low side	1.02	1.02	1.02	1.02	1.02	1.02	1.02
J+14	TD - LTC control time delay, s	30	30	30	30	30	30	30
J+15	TC - LTC tap adjustment time delay, s	5	5	5	5	5	5	5
J+16	Rcmp - xfr compensating R, pu on load base	0	0	0	0	0	0	0
J+17	Xcmp - xfr compensating X, pu on load base	0	0	0	0	0	0	0
J+18	FmA - Composite load motor A fraction	0.12	0.1072	0.05	0.1072	0.15	0.15	0
J+19	FmB - Composite load motor B fraction	0.1	0.1455	0.5	0.1455	0.25	0.25	0.2
J+20	FmC - Composite load motor C fraction	0.09	0.1267	0.25	0.1267	0.4	0.4	0.32
J+21	FmD - Composite load motor D fraction	0.06	0.0406	0	0.0406	0	0	0
J+22	Fel - Composite load electronic fraction	0.24	0.2989	0.15	0.2989	0.15	0.15	0.46
J+23	PFel - Electronic load power factor	1	1	1	1	1	1	1
J+24	Vd1 - Voltage electronic loads start to drop	0.8	0.85	0.85	0.85	0.85	0.85	0.85
J+25	Vd2 - Voltage all electronic load has dropped	0.4	0.5	0.5	0.5	0.5	0.5	0.5
J+26	PFs - Static load lower lactor	1	1	1	1	1	1	1
J+27	P1e - First exponent for static load P	1	1	1	1	1	1	1
J+28	P1c - First coeff for static load P	0.35	0.1829	1	0.1829	1	1	1

CONs	Name	Zone						
		Z1	Z20	Z22	Z29	Z82	Z92	Z224
J+29	P2e - Second exponent for static load P	2	2	2	2	2	2	2
J+30	P2c - Second coeff for static load P	0.65	0.8171	0	0.8171	0	0	0
J+31	Pfrq - Frequency sensitivity for static P	0	0	0	0	0	0	0
J+32	Q1e - First exponent for static load Q	1	1	1	1	1	1	1
J+33	Q1c - First coeff for static load Q	0.35	0.1829	1	0.1829	1	1	1
J+34	Q2e - Second exponent for static load Q	2	2	2	2	2	2	2
J+35	Q2c - Second coeff for static load Q	0.65	0.8171	0	0.8171	0	0	0
J+36	Qfrq - Frequency sensitivity for static load Q	-1	-1	-1	-1	-1	-1	-1
J+37	Mtyp - Motor A phase, always 3	3	3	3	3	3	3	3
J+38	LF - Motor A real power to power base ratio	0.75	0.75	0.75	0.75	0.75	0.75	0.75
J+39	Ra - Motor A stator resistance, pu on motor base	0.04	0.02	0.02	0.02	0.02	0.02	0.02
J+40	X - Motor A synchronous reactance, pu	1.8	1.8	1.8	1.8	1.8	1.8	1.8
J+41	X' - Motor A transient reactance, pu	0.12	0.12	0.12	0.12	0.12	0.12	0.12
J+42	X" - Motor A subtransient reactance, pu	0.104	0.104	0.104	0.104	0.104	0.104	0.104
J+43	To' - Motor A transient open circuit time constant, s	0.095	0.095	0.095	0.095	0.095	0.095	0.095
J+44	To" - Motor A subtransient open cir time constant, s	0.0021	0.0021	0.0021	0.0021	0.0021	0.0021	0.0021
J+45	H - Motor A inertia constant	0.1	0.1	0.1	0.1	0.1	0.1	0.1
J+46	etrq - Motor A exp for variation of torque with speed	0	0	0	0	0	0	0
J+47	Vtr1 - Motor A 1st undervoltage trip voltage, pu	0.75	0.75	0.75	0.75	0.75	0.75	0.75
J+48	Ttr1 - Motor A 1st undervoltage trip delay, s	0.09	0.06	0.06	0.06	0.06	0.06	0.06
J+49	Ftr1 - Motor A 1st undervoltage trip fraction	0.6	0.1	0.1	0.1	0.1	0.1	0.1
J+50	Vrc1 - Motor A 1st undervoltage reclose voltage, pu	0.8	0.8	0.8	0.8	0.8	0.8	0.8
J+51	Trc1 - Motor A 1st undervoltage reclose delay, s	99999	99999	99999	99999	99999	99999	99999
J+52	Vtr2 - Motor A 2nd undervoltage trip voltage, pu	0.62	0.62	0.62	0.62	0.62	0.62	0.62
J+53	Ttr2 - Motor A 2nd undervoltage trip delay, s	0.021	0.021	0.021	0.021	0.021	0.021	0.021
J+54	Ftr2 - Motor A 2nd undervoltage trip fraction	0.4	0.2	0.2	0.2	0.2	0.2	0.2
J+55	Vrc2 - Motor A 2nd undervoltage reclose voltage, pu	0.7	0.7	0.7	0.7	0.7	0.7	0.7
J+56	Trc2 - Motor A 2nd undervoltage reclose delay, s	0.1	0.1	0.1	0.1	0.1	0.1	0.1
J+57	Mtyp - Motor B phase, always 3	3	3	3	3	3	3	3
J+58	LF - Motor B real power to power base ratio	0.75	0.75	0.75	0.75	0.75	0.75	0.75
J+59	Ra - Motor B stator resistance, pu on motor base	0.03	0.03	0.03	0.03	0.03	0.03	0.03
J+60	X - Motor B synchronous reactance, pu	1.8	1.8	1.8	1.8	1.8	1.8	1.8
J+61	X' - Motor B transient reactance, pu	0.19	0.19	0.19	0.19	0.19	0.19	0.19
J+62	X" - Motor B subtransient reactance, pu	0.14	0.14	0.14	0.14	0.14	0.14	0.14
J+63	To' - Motor B transient open circuit time constant, s	0.2	0.2	0.2	0.2	0.2	0.2	0.2

CONs	Name	Zone						
		Z1	Z20	Z22	Z29	Z82	Z92	Z224
J+64	To" - Motor B subtransient open cir time constant, s	0.0026	0.0026	0.0026	0.0026	0.0026	0.0026	0.0026
J+65	H - Motor B inertia constant	0.5	0.5	0.5	0.5	0.5	0.5	0.5
J+66	etrq - Motor B torque speed exponent	2	2	2	2	2	2	2
J+67	Vtr1 - Motor B 1st undervoltage trip voltage, pu	0.7	0.7	0.7	0.7	0.7	0.7	0.7
J+68	Ttr1 - Motor B 1st undervoltage trip delay, s	0.02	0.02	0.02	0.02	0.02	0.02	0.02
J+69	Ftr1 - Motor B 1st undervoltage trip fraction	0.3	0.1	0.1	0.1	0.1	0.1	0.1
J+70	Vrc1 - Motor B 1st undervoltage reclose voltage, pu	0.75	0.75	0.75	0.75	0.75	0.75	0.75
J+71	Trc1 - Motor B 1st undervoltage reclose delay, s	0.05	0.05	0.05	0.05	0.05	0.05	0.05
J+72	Vtr2 - Motor B 2nd undervoltage trip voltage, pu	0.45	0.45	0.45	0.45	0.45	0.45	0.45
J+73	Ttr2 - Motor B 2nd undervoltage trip delay, s	0.021	0.021	0.021	0.021	0.021	0.021	0.021
J+74	Ftr2 - Motor B 2nd undervoltage trip fraction	0.4	0.2	0.2	0.2	0.2	0.2	0.2
J+75	Vrc2 - Motor B 2nd undervoltage reclose voltage, pu	0.6	0.6	0.6	0.6	0.6	0.6	0.6
J+76	Trc2 - Motor B 2nd undervoltage reclose delay, s	0.05	0.05	0.05	0.05	0.05	0.05	0.05
J+77	Mtyp - Motor C phase, always 3	3	3	3	3	3	3	3
J+78	LF - Motor C real power to power base ratio	0.75	0.75	0.75	0.75	0.75	0.75	0.75
J+79	Ra - Motor C stator resistance, pu on motor base	0.03	0.03	0.03	0.03	0.03	0.03	0.03
J+80	X - Motor C synchronous reactance, pu	1.8	1.8	1.8	1.8	1.8	1.8	1.8
J+81	X' - Motor C transient reactance, pu	0.19	0.19	0.19	0.19	0.19	0.19	0.19
J+82	X" - Motor C subtransient reactance, pu	0.14	0.14	0.14	0.14	0.14	0.14	0.14
J+83	To' - Motor C transient open circuit time constant, s	0.2	0.2	0.2	0.2	0.2	0.2	0.2
J+84	To" - Motor C subtransient open cir time constant, s	0.0026	0.0026	0.0026	0.0026	0.0026	0.0026	0.0026
J+85	H - Motor C inertia constant	0.1	0.1	0.1	0.1	0.1	0.1	0.1
J+86	etrq - Motor C torque speed exponent	2	2	2	2	2	2	2
J+87	Vtr1 - Motor C 1st undervoltage trip voltage, pu	0.75	0.8	0.8	0.8	0.8	0.8	0.8
J+88	Ttr1 - Motor C 1st undervoltage trip delay, s	0.03	0.03	0.03	0.03	0.03	0.03	0.03
J+89	Ftr1 - Motor C 1st undervoltage trip fraction	0.6	0.1	0.1	0.1	0.1	0.1	0.8
J+90	Vrc1 - Motor C 1st undervoltage reclose voltage, pu	0.8	0.8	0.8	0.8	0.8	0.8	0.8
J+91	Trc1 - Motor C 1st undervoltage reclose delay, s	9999	9999	9999	9999	9999	9999	9999
J+92	Vtr2 - Motor C 2nd undervoltage trip voltage, pu	0.5	0.5	0.5	0.5	0.5	0.5	0.5
J+93	Ttr2 - Motor C 2nd undervoltage trip delay, s	0.03	0.03	0.03	0.03	0.03	0.03	0.03
J+94	Ftr2 - Motor C 2nd undervoltage trip fraction	0.4	0.2	0.2	0.2	0.2	0.2	0.2
J+95	Vrc2 - Motor C 2nd undervoltage reclose voltage, pu	0.6	0.6	0.6	0.6	0.6	0.6	0.6
J+96	Trc2 - Motor C 2nd undervoltage reclose delay, s	0.11	0.11	0.11	0.11	0.11	0.11	0.11
J+97	Tstall - Motor D stall delay time, s	0.03	0.04	0.04	0.04	0.04	0.04	0.04
J+98	Trestart - Motor D restart from stall delay time, s	0.3	0.3	0.3	0.3	0.3	0.3	0.3

CONs	Name	Zone						
		Z1	Z20	Z22	Z29	Z82	Z92	Z224
J+99	Tv - Motor D voltage time constant for contactors, s	0.025	0.025	0.025	0.025	0.025	0.025	0.025
J+100	Tf - Motor D frequency time constant for contactors, s	0.1	0.1	0.1	0.1	0.1	0.1	0.1
J+101	CompLF - Motor D real power to motor base ratio	1	1	1	1	1	1	1
J+102	CompPF - Motor D power factor at 1.0 pu voltage	0.98	0.71	0.71	0.71	0.71	0.71	0.71
J+103	Vstall - Motor D stall Voltage, pu	0.45	0.49	0.49	0.49	0.49	0.49	0.49
J+104	Rstall - Motor D stall resistance, pu of motor base	0.1	0.143	0.143	0.143	0.143	0.143	0.143
J+105	Xstall - Motor D stall reactance, pu of motor base	0.1	0.143	0.143	0.143	0.143	0.143	0.143
J+106	LFadj - Adjustment to stall voltage if COMPLF /= 1.0	0	0	0	0	0	0	0
J+107	Kp1 - Motor D real power coeff when voltage > Vbrk	0	0	0	0	0	0	0
J+108	Np1 - Motor D real power exp when voltage > Vbrk	1	1	1	1	1	1	1
J+109	Kq1 - Motor D reactive power coeff when voltage > Vbrk	6	6	6	6	6	6	6
J+110	Nq1 - Motor D reactive power exp when voltage>Vbrk	2	2	2	2	2	2	2
J+111	Kp2 - Motor D real power coeff when voltage < Vbrk	12	12	12	12	12	12	12
J+112	Np2 - Motor D real power exp when voltage < Vbrk	3.2	3.2	3.2	3.2	3.2	3.2	3.2
J+113	Kq2 - Motor D reactive power coeff when voltage < Vbrk	11	11	11	11	11	11	11
J+114	Nq2 - Motor D reactive power exp when voltage<Vbrk	2.5	2.5	2.5	2.5	2.5	2.5	2.5
J+115	Vbrk - Motor D "break-down" voltage,	0.86	0.86	0.86	0.86	0.86	0.86	0.86
J+116	Frst - Motor D fraction capable of restart after stall	0.2	0.1	0.1	0.1	0.1	0.1	0.1
J+117	Vrst - Motor D voltage for restart after stall, pu	0.95	0.95	0.95	0.95	0.95	0.95	0.95
J+118	CmpKpf - Motor D real power frequency dependency	1	1	1	1	1	1	1
J+119	CmpKqf - Motor D reactive power freq dependency	-3.3	-3.3	-3.3	-3.3	-3.3	-3.3	-3.3
J+120	Vc1off - Motor D voltage at which contactors start opening, pu	0.5	0.5	0.5	0.5	0.5	0.5	0.5
J+121	Vc2off - Motor D voltage at which all contactors are opened, pu	0.4	0.4	0.4	0.4	0.4	0.4	0.4
J+122	Vc1on - Motor D voltage at which all contactors are reclosed, pu	0.6	0.6	0.6	0.6	0.6	0.6	0.6
J+123	Vc2on - Motor D voltage at which contactors start reclosing, pu	0.52	0.52	0.52	0.52	0.52	0.52	0.52
J+124	Tth - Motor D heating time constant, s	15	15	15	15	15	15	15
J+125	Th1t - Motor D temperature where tripping begins, pu	0.7	1.98	1.98	1.98	1.98	1.98	1.98
J+126	Th2t - Motor D temperature where completely tripped	1.9	4.59	4.59	4.59	4.59	4.59	4.59
J+127	Fuvr - Motor D fraction with undervoltage relays	0.1	0.325	0.325	0.325	0.325	0.325	0.325
J+128	UVtr1 - Motor D 1st undervoltage pick-up, pu	0.5	0.55	0.55	0.55	0.55	0.55	0.55
J+129	Ttr1 - Motor D 1st undervoltage trip delay, s	0.02	0.06	0.06	0.06	0.06	0.06	0.06
J+130	UVtr2 - Motor D 2nd undervoltage pick-up, pu	0.1	0.1	0.1	0.1	0.1	0.1	0.1
J+131	Ttr2 - Motor D 2nd under voltage trip delay, s	9999	9999	9999	9999	9999	9999	9999
J+132	frcel - Fraction electronic load that can reconnect	0.95	0.7	0.7	0.7	0.7	0.7	0.86

7 Appendix B: DER test results

7.1 DER test results with phase angle trip logic disabled

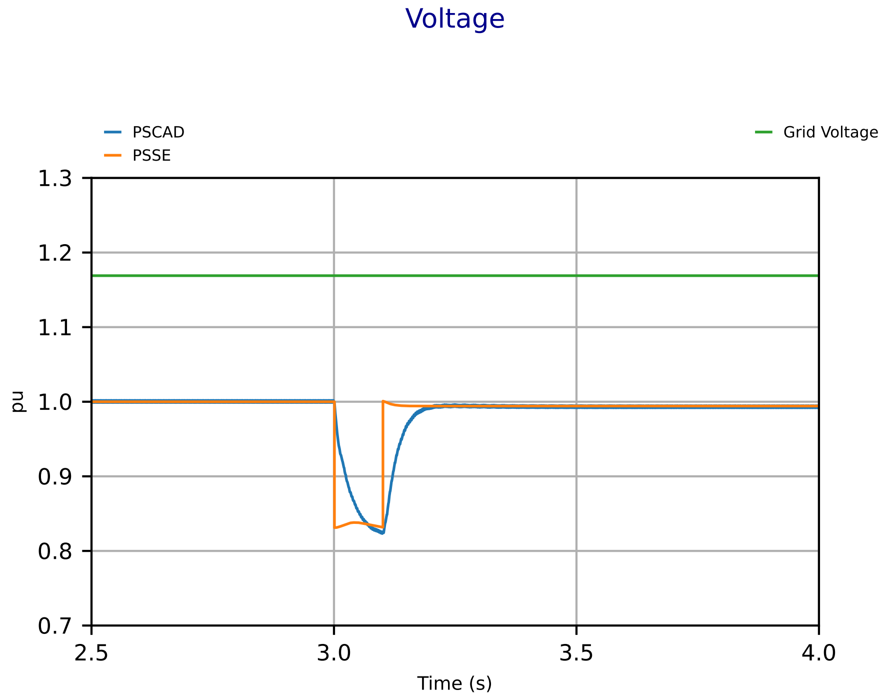
DER SMIB

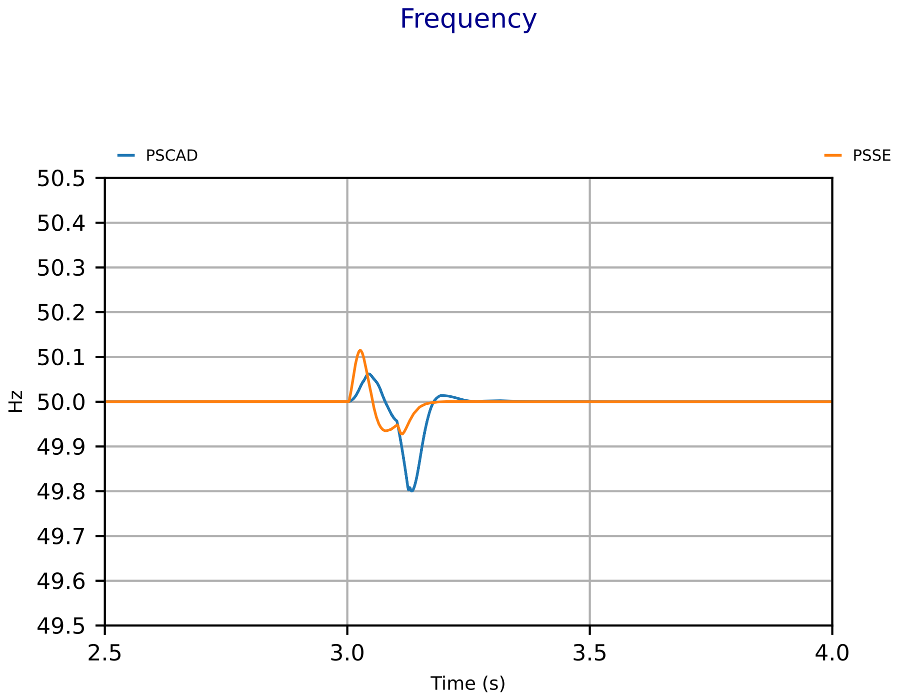
SCR = 3, X/R = 3

Test #1:

LG fault for 100 ms

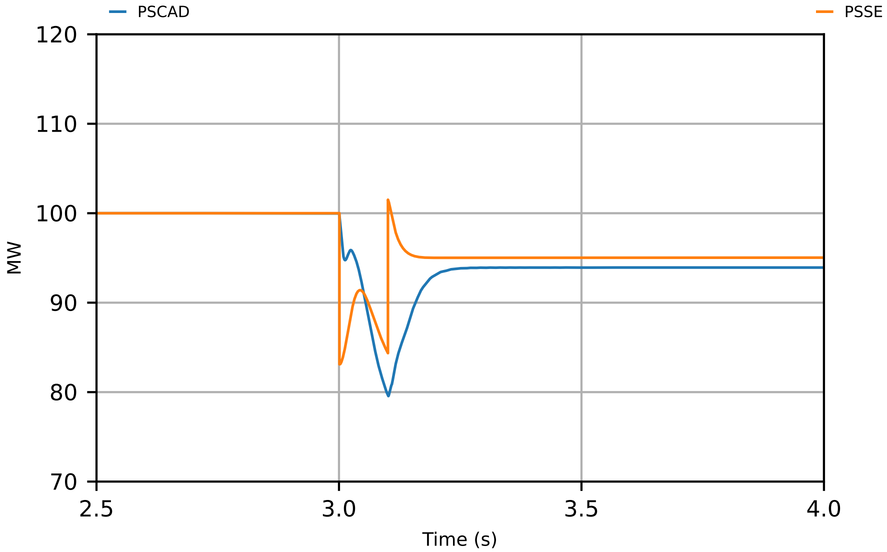
DER_SMIB_SCR_3_XR_3_T1_1



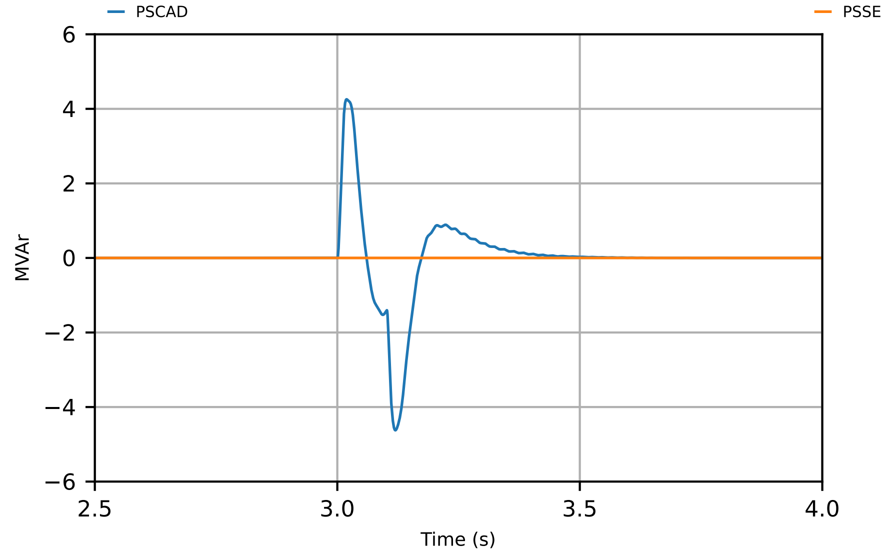


DER_SMIB_SCR_3_XR_3_T1_2

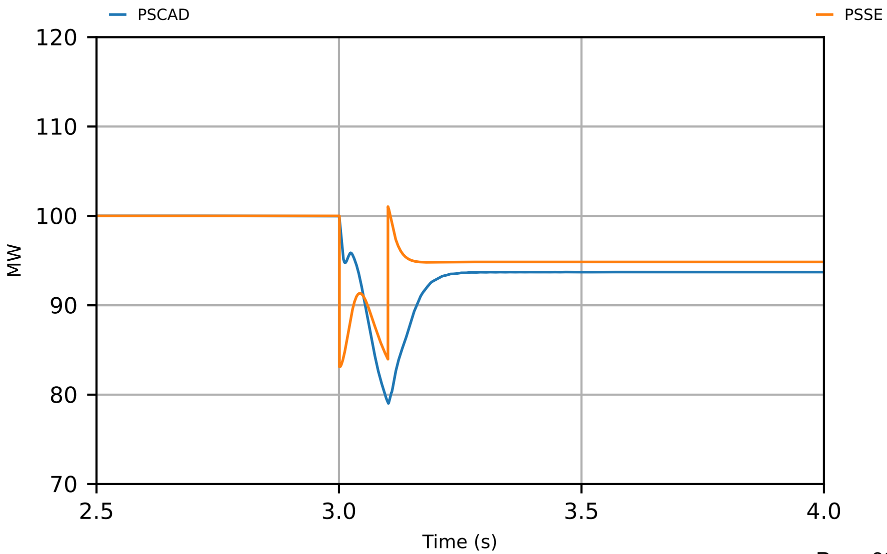
NSW DER Active Power



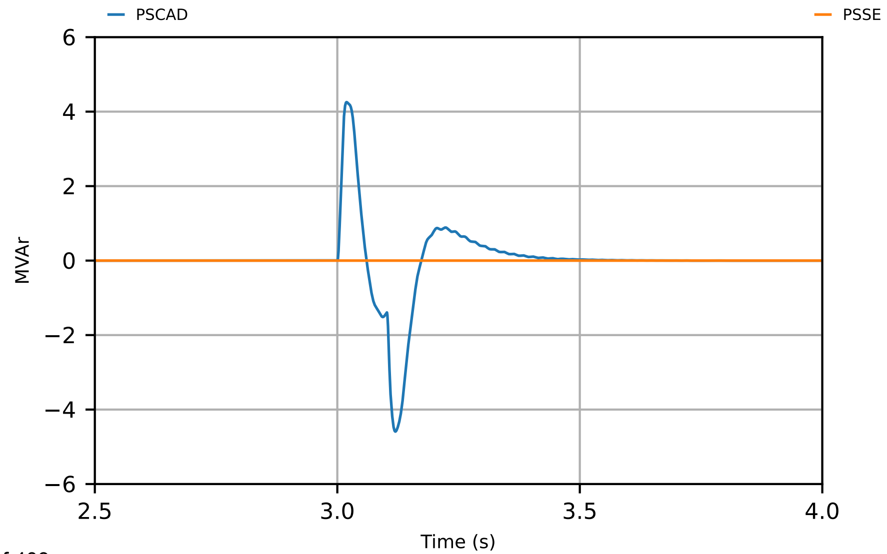
NSW DER Reactive Power



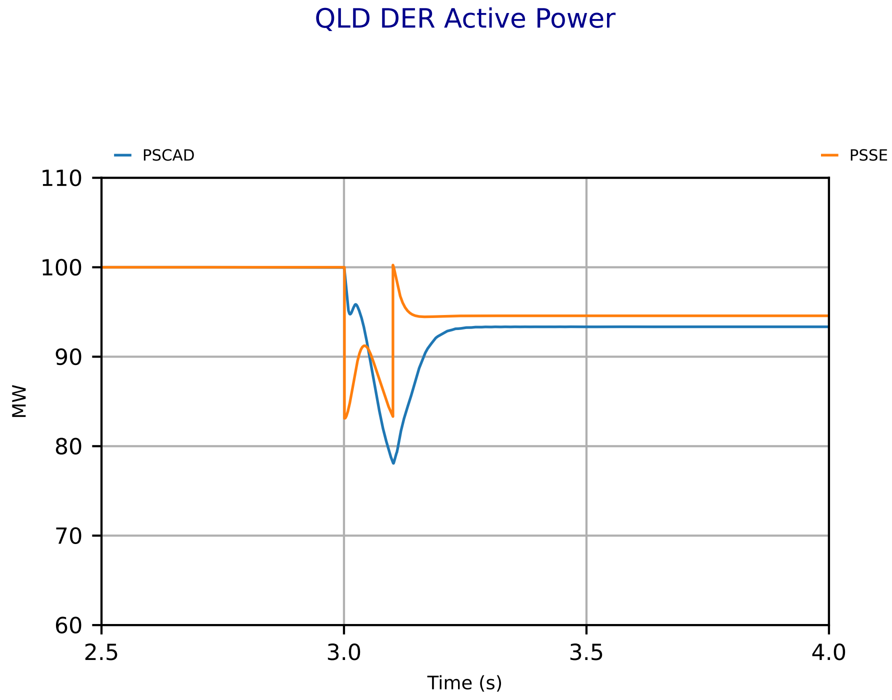
VIC DER Active Power

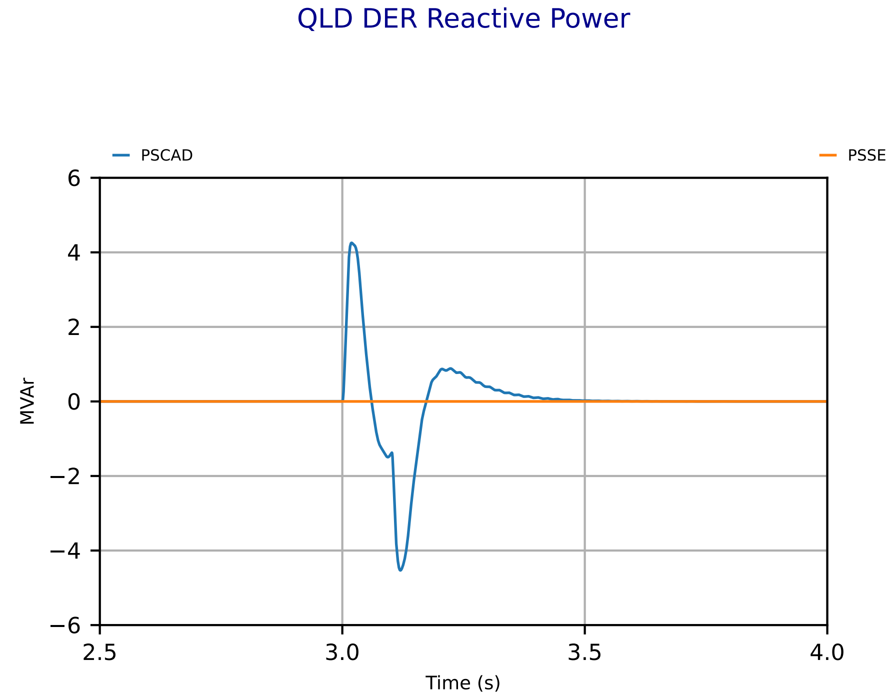


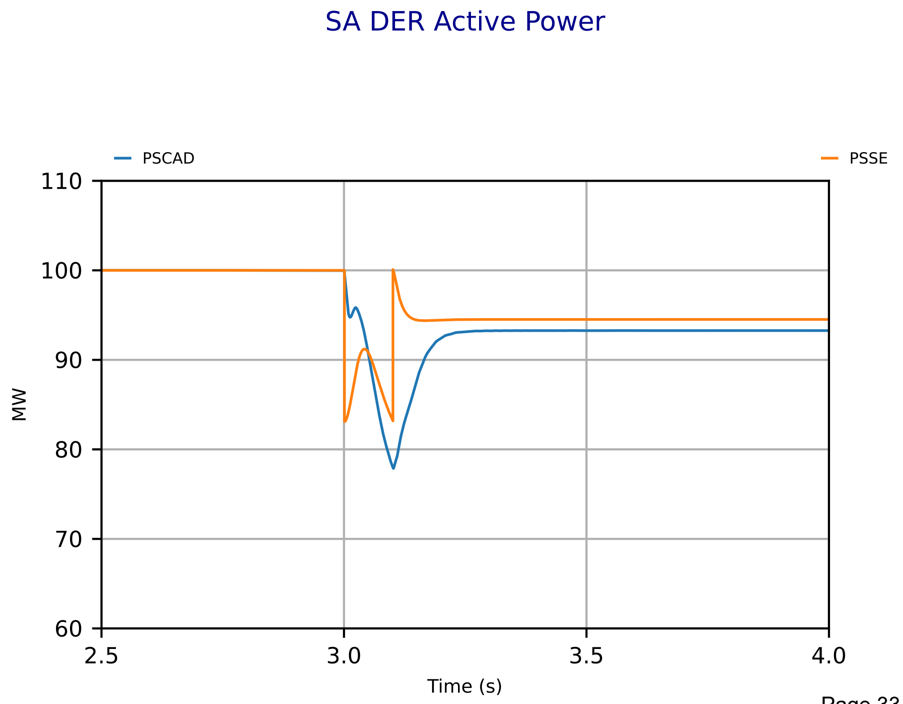
VIC DER Reactive Power

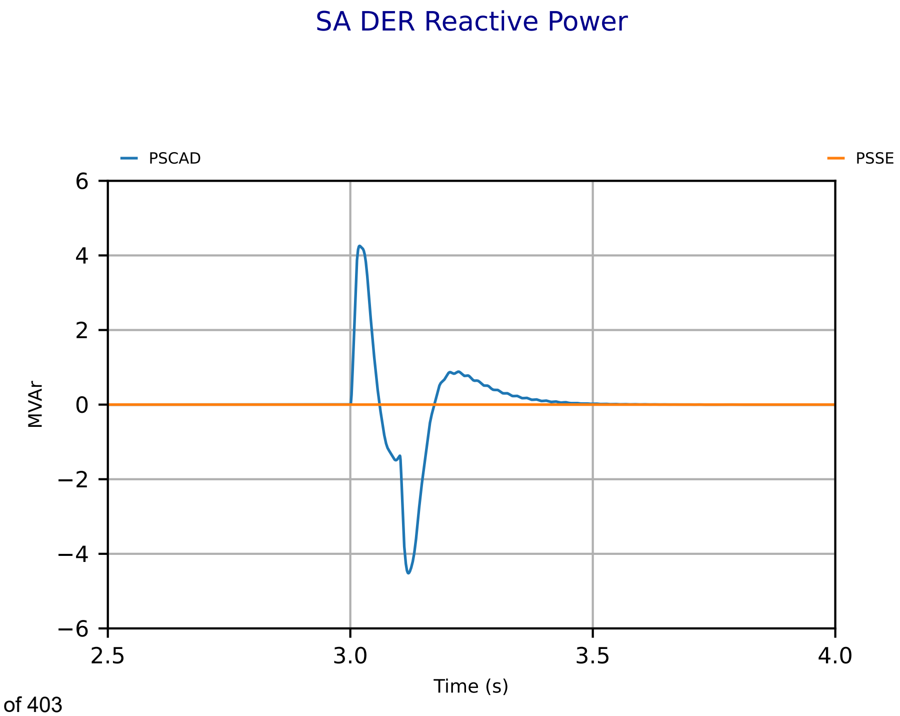


DER_SMIB_SCR_3_XR_3_T1_3







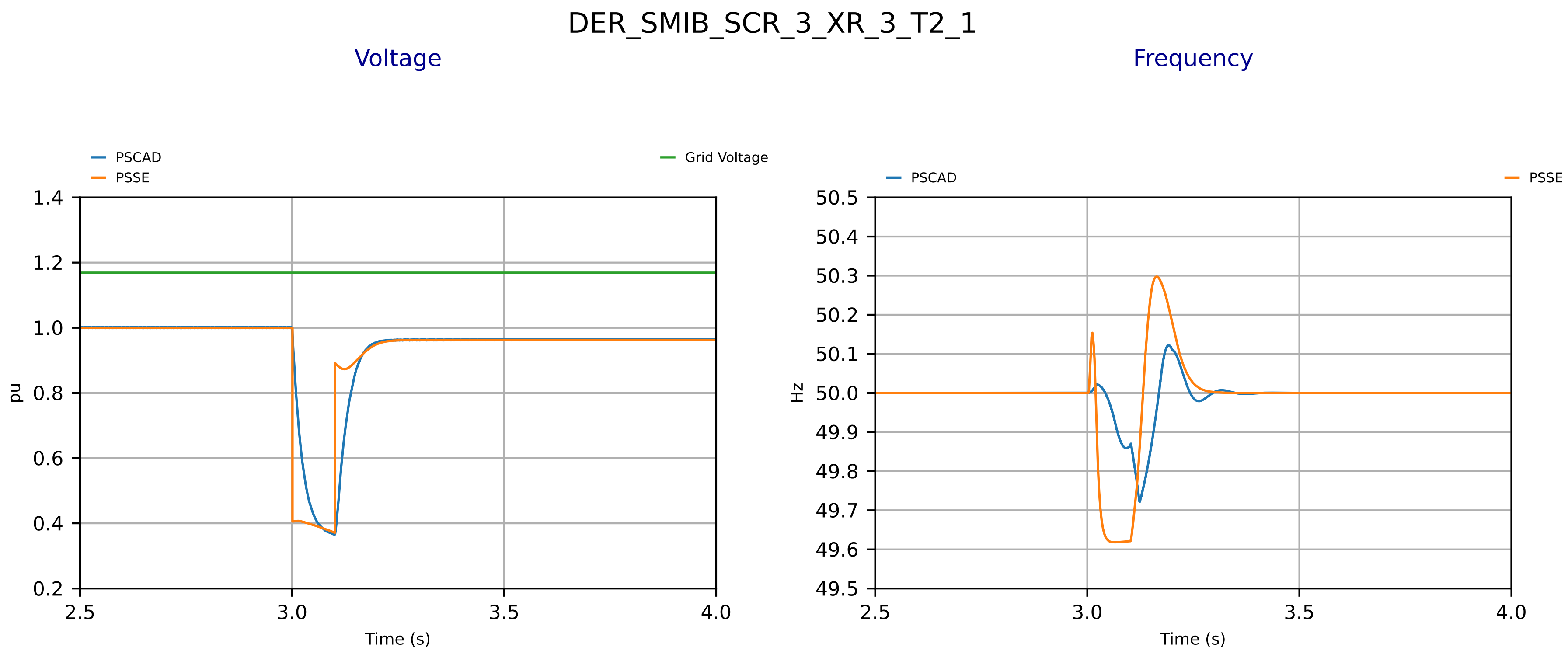


DER SMIB

SCR = 3, X/R = 3

Test #2:

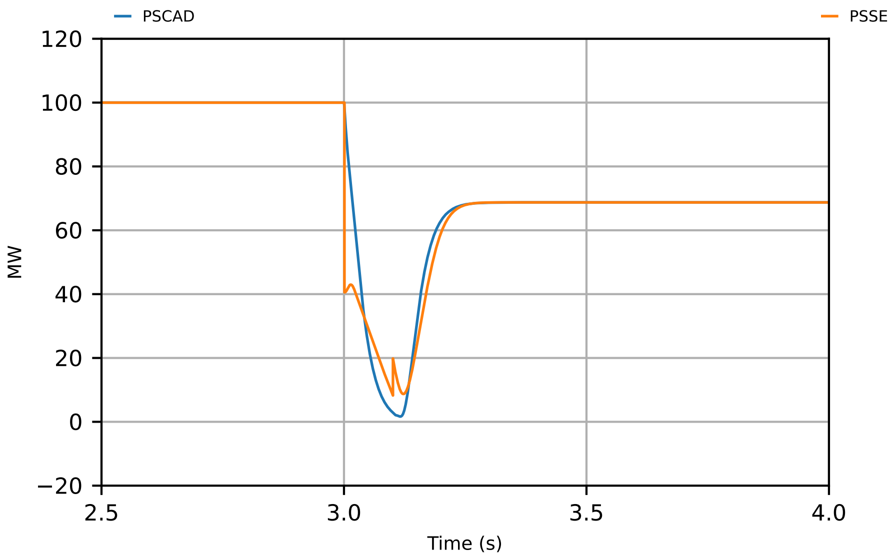
LLG fault for 100 ms



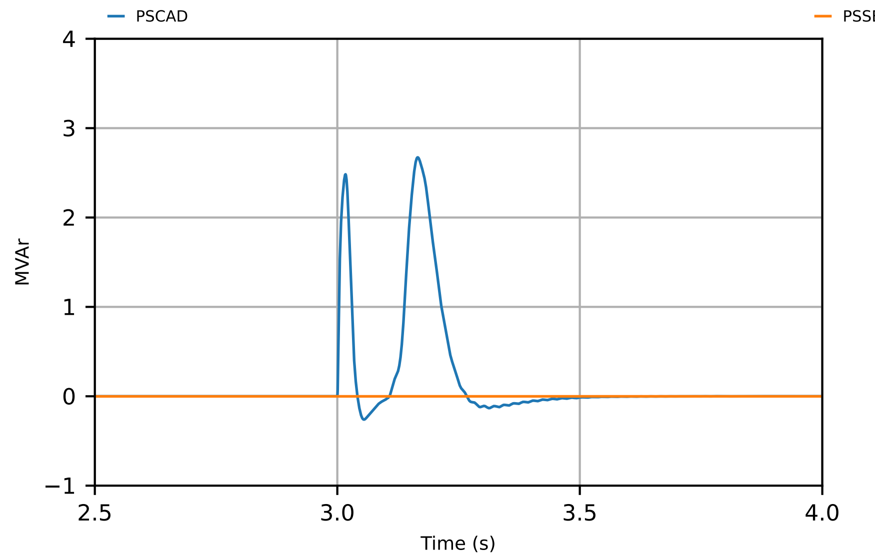
DER_SMIB_SCR_3_XR_3_T2_1
Voltage
Frequency
PSCAD
PSSE
Grid Voltage
1.4
1.2
1.0
0.8
0.6
0.4
0.2
pu
2.5
3.0
3.5
4.0
Time (s)
PSCAD
PSSE
50.5
50.4
50.3
50.2
50.1
50.0
49.9
49.8
49.7
49.6
49.5
Hz
2.5
3.0
3.5
4.0
Time (s)

DER_SMIB_SCR_3_XR_3_T2_2

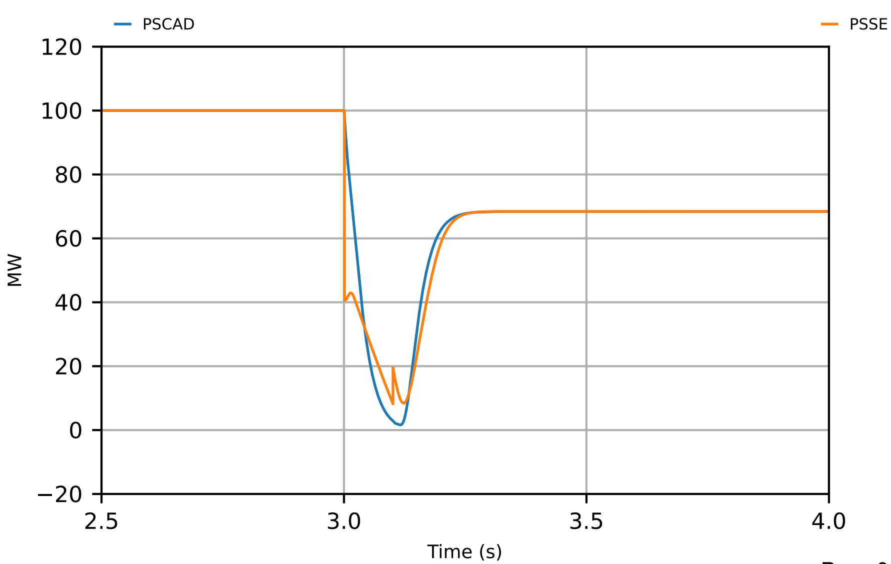
NSW DER Active Power



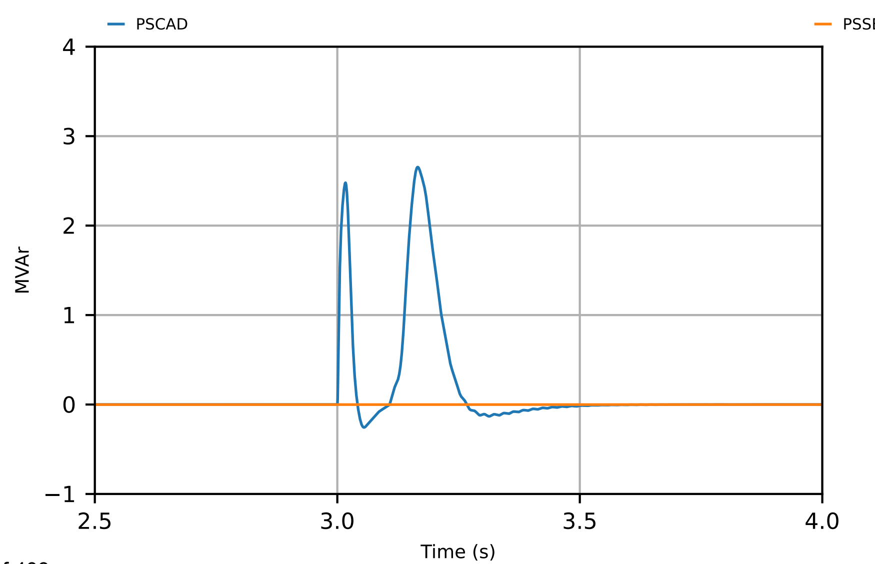
NSW DER Reactive Power



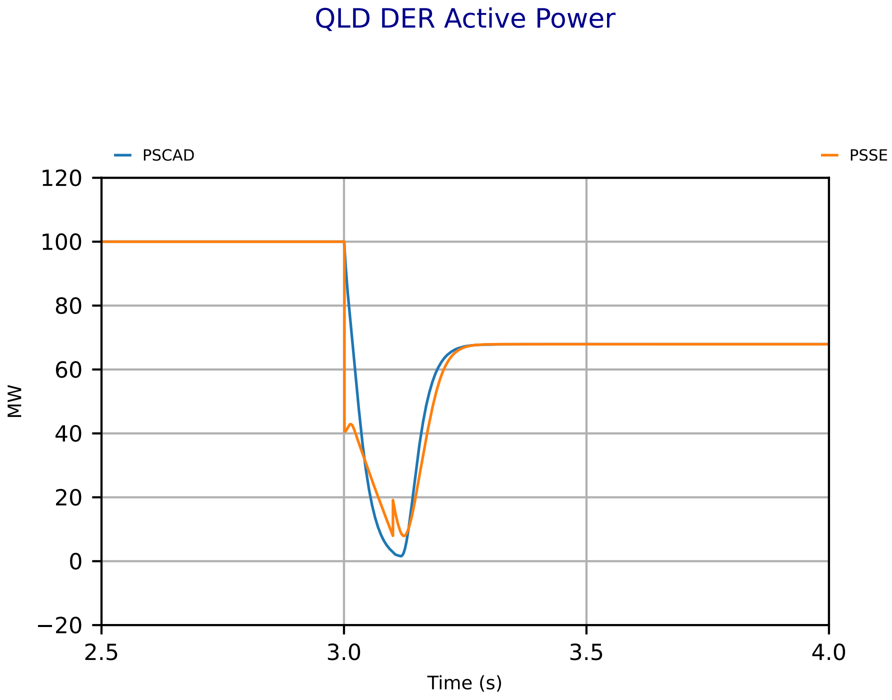
VIC DER Active Power

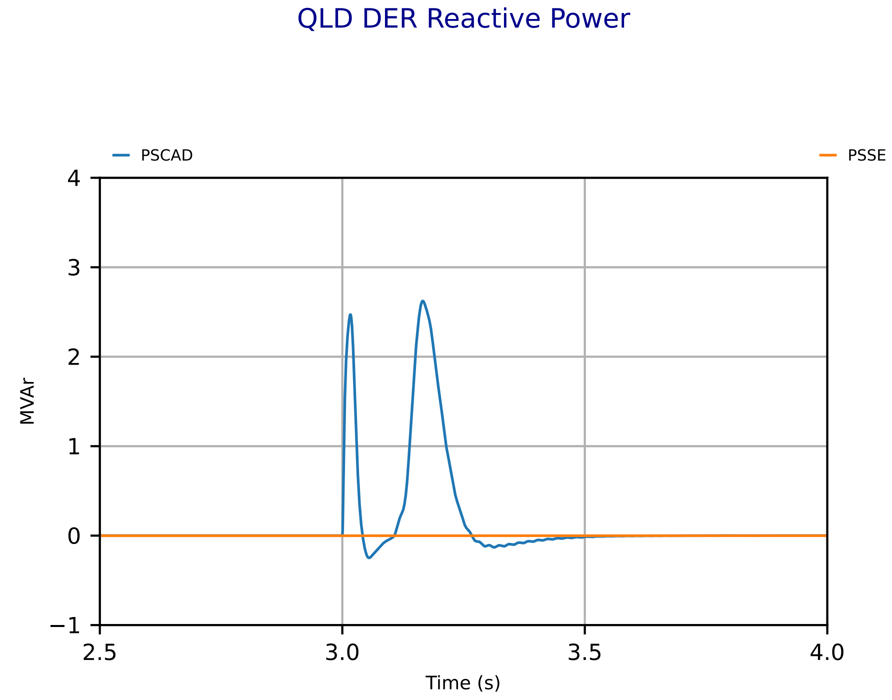


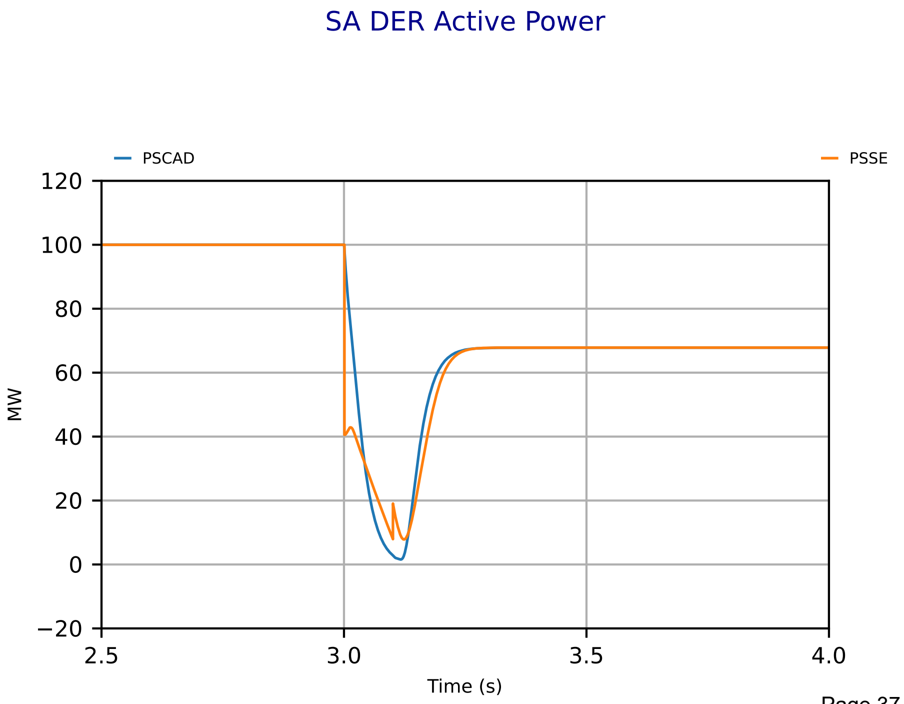
VIC DER Reactive Power

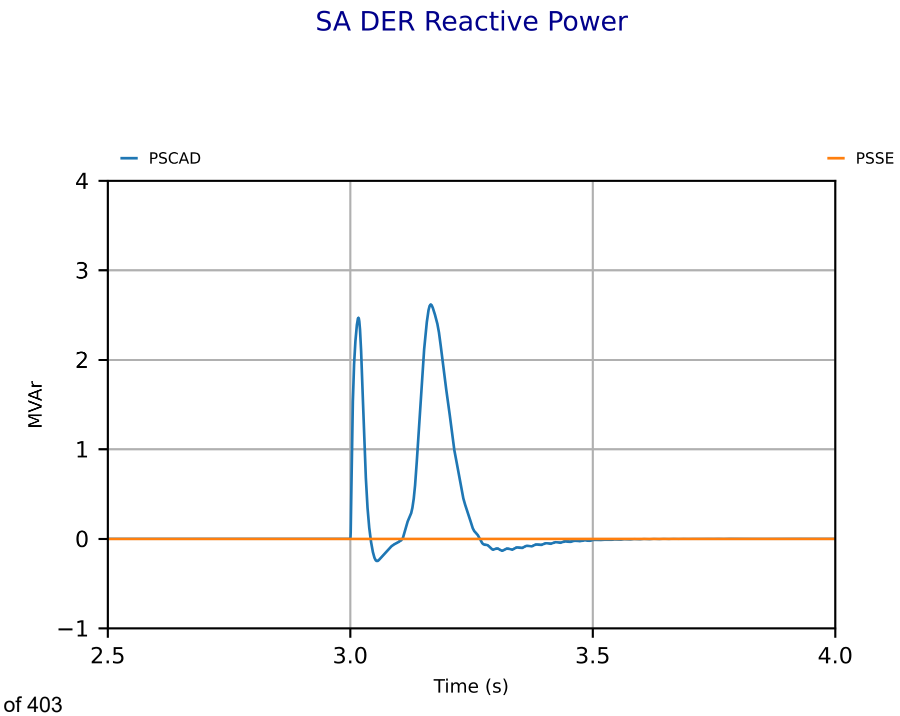


DER_SMIB_SCR_3_XR_3_T2_3









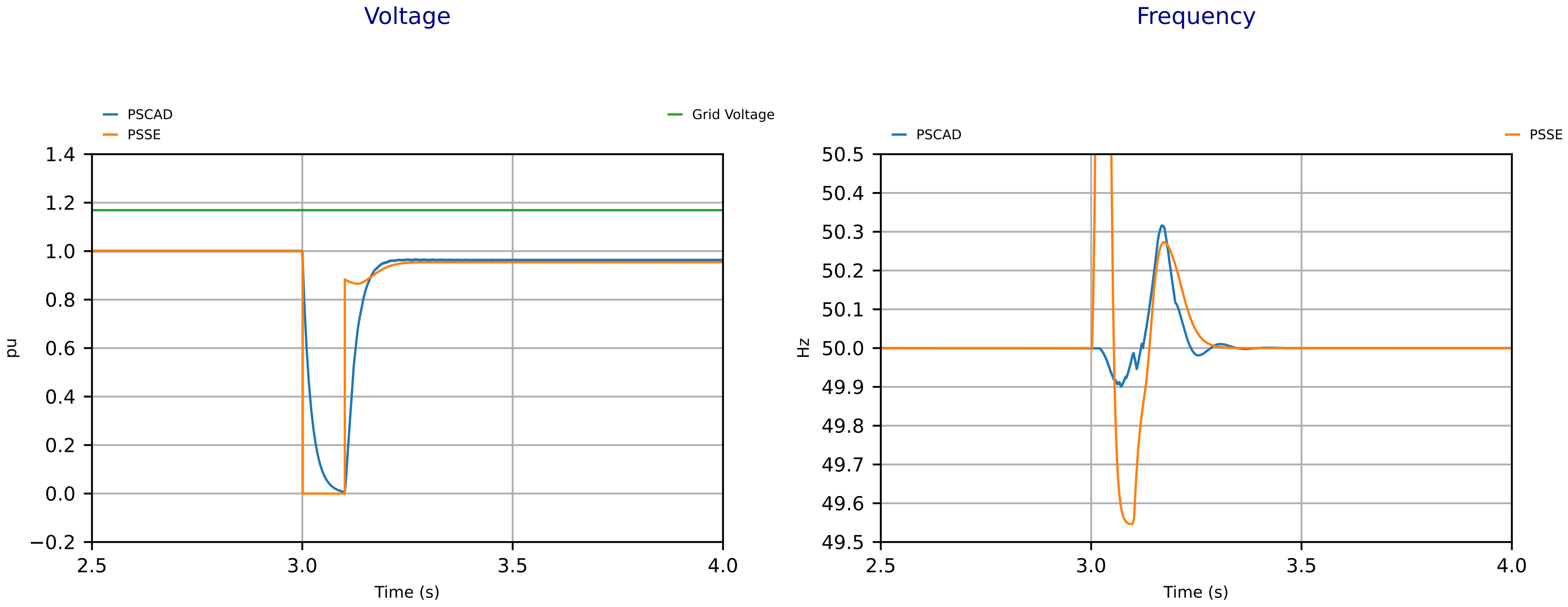
DER SMIB

SCR = 3, X/R = 3

Test #3:

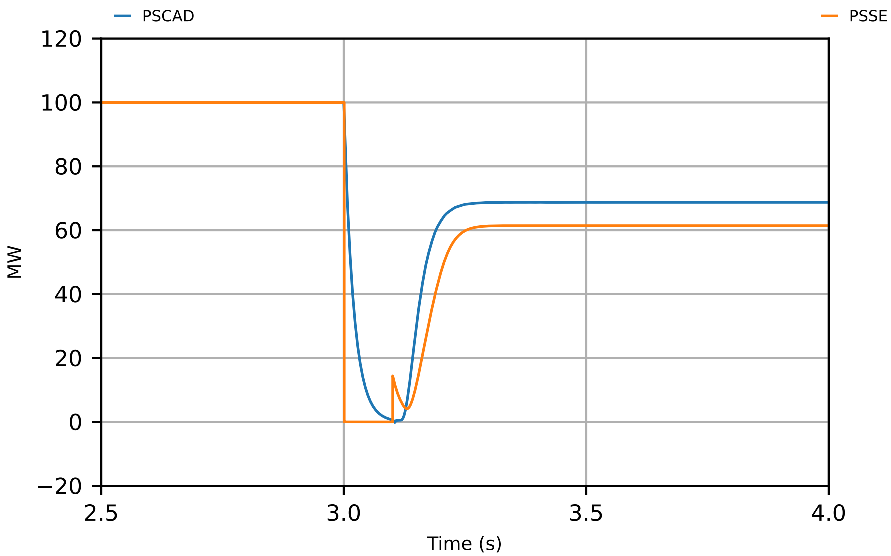
3PH-G fault for 100 ms

DER_SMIB_SCR_3_XR_3_T3_1

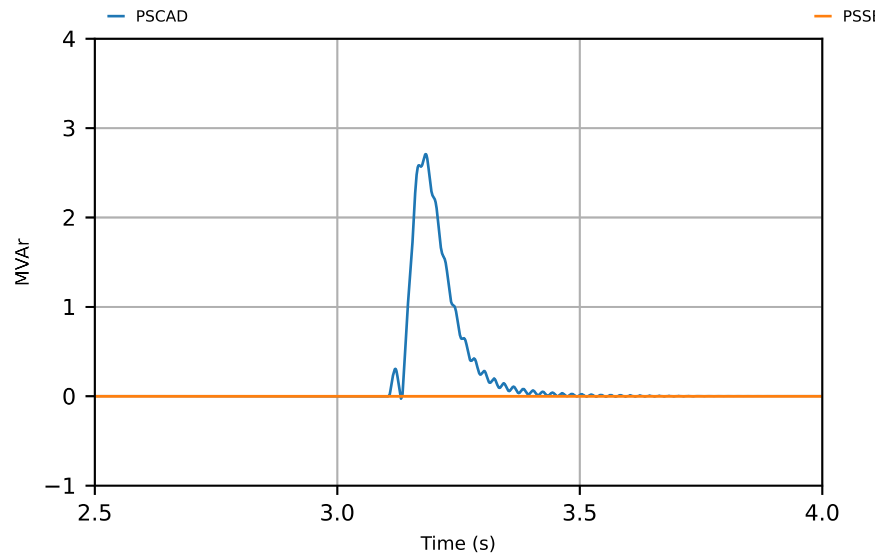


DER_SMIB_SCR_3_XR_3_T3_2

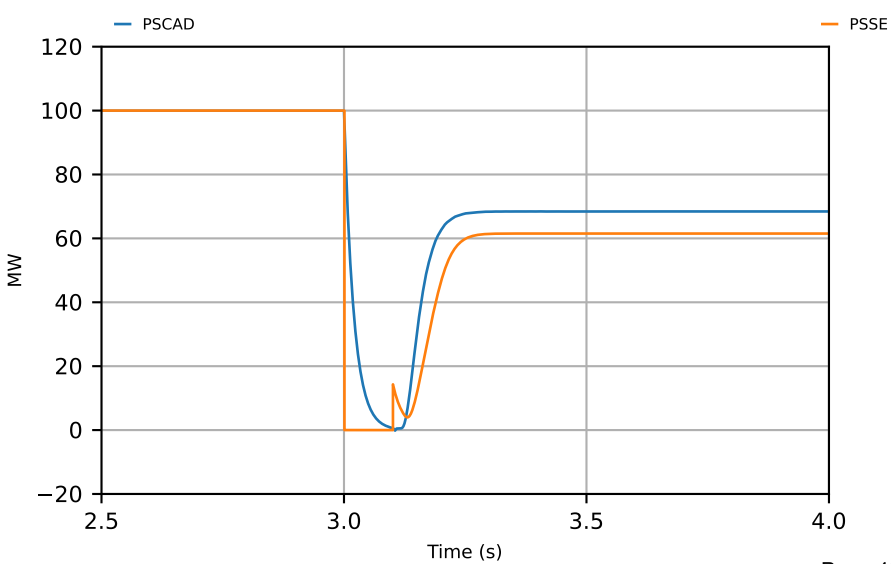
NSW DER Active Power



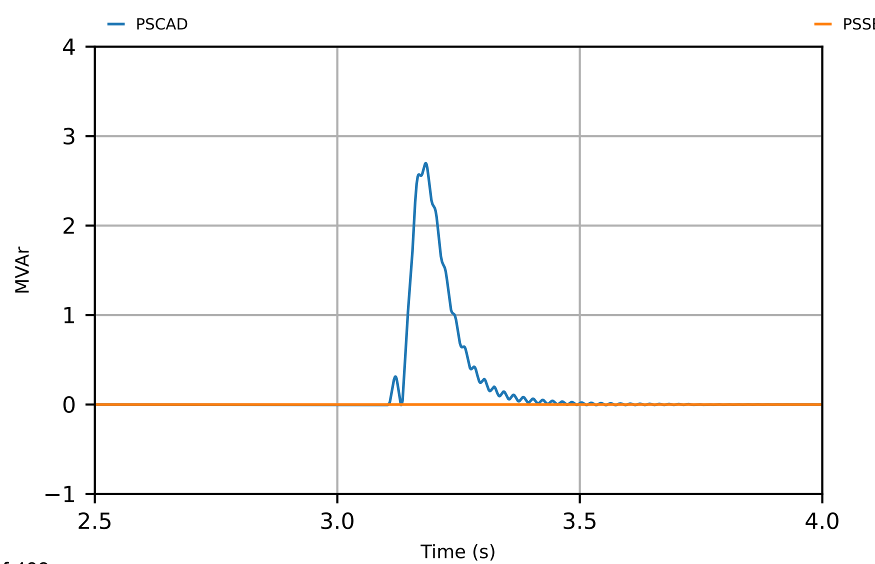
NSW DER Reactive Power



VIC DER Active Power

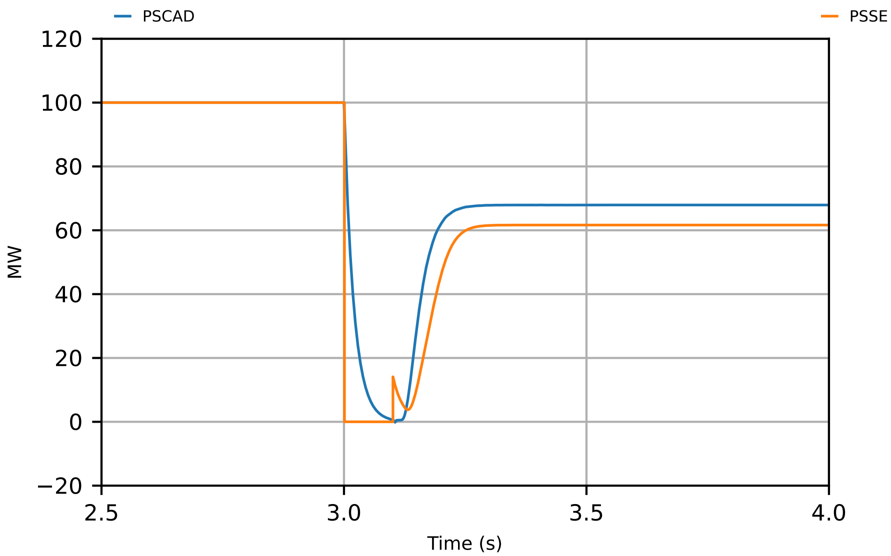


VIC DER Reactive Power

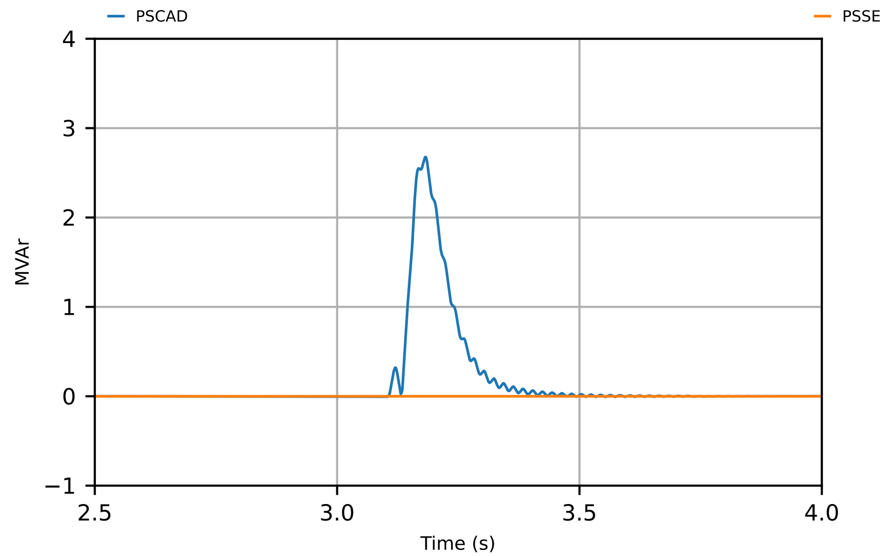


DER_SMIB_SCR_3_XR_3_T3_3

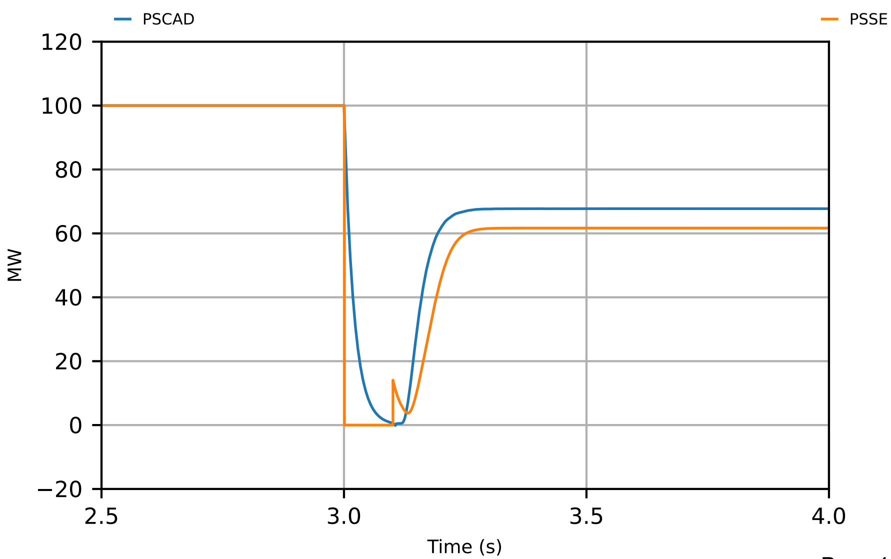
QLD DER Active Power



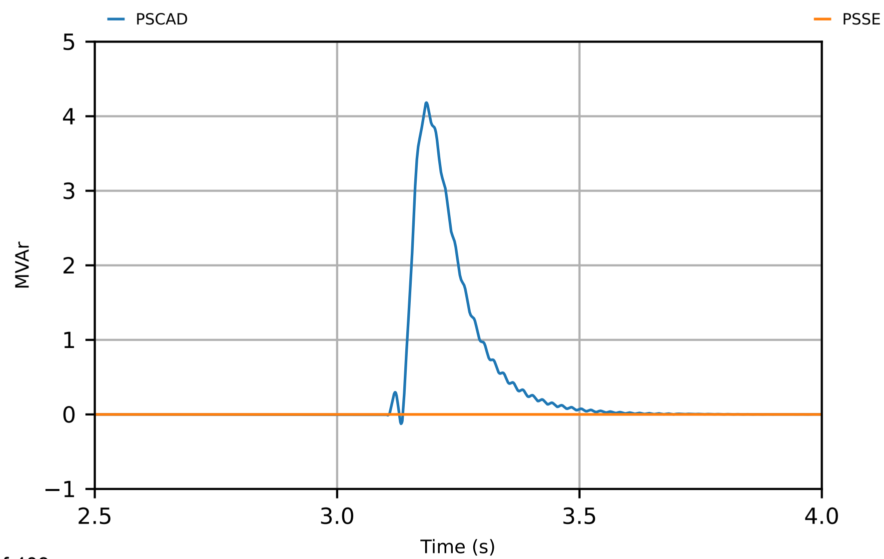
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power

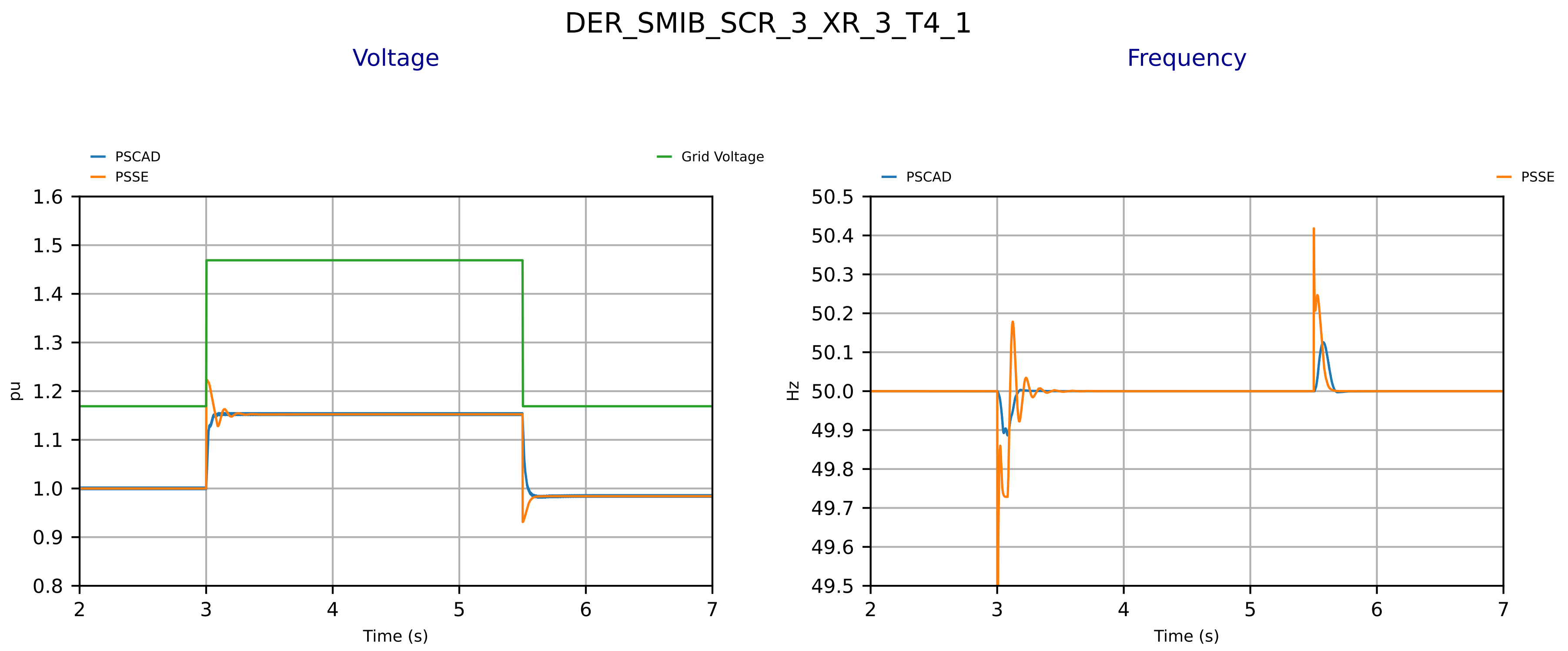


DER SMIB

SCR = 3, X/R = 3

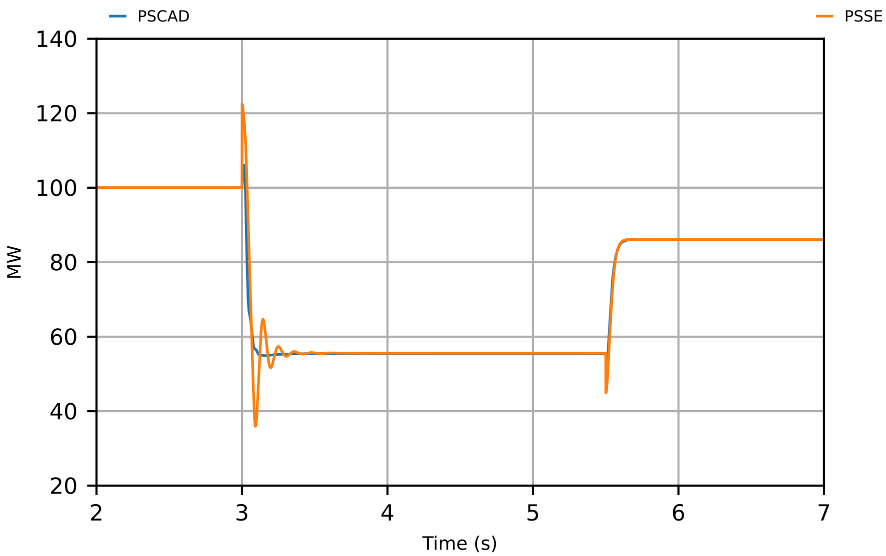
Test #4:

~115% Voltage disturbance for 2.5 s

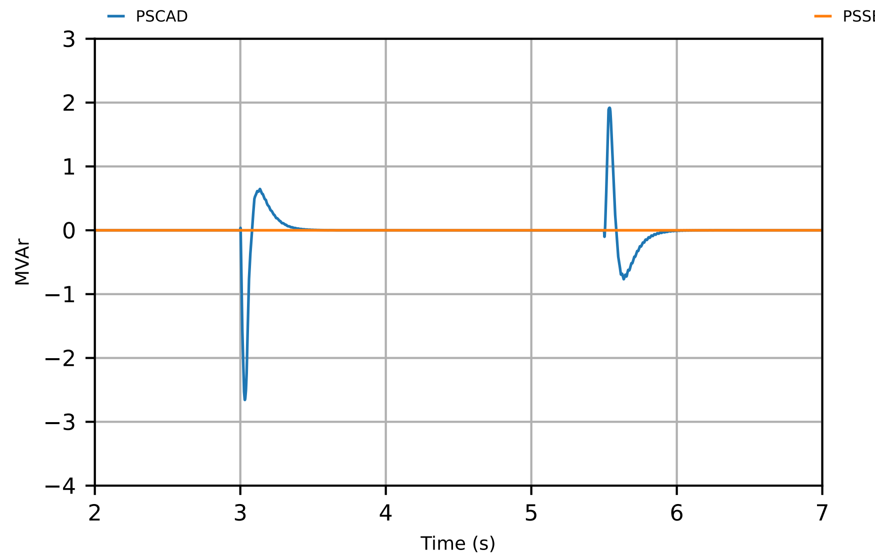

DER_SMIB_SCR_3_XR_3_T4_1
Voltage
PSCAD
PSSE
Grid Voltage
pu
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
2
3
4
5
6
7
Time (s)
Frequency
PSCAD
PSSE
Hz
50.5
50.4
50.3
50.2
50.1
50.0
49.9
49.8
49.7
49.6
49.5
2
3
4
5
6
7
Time (s)

DER_SMIB_SCR_3_XR_3_T4_2

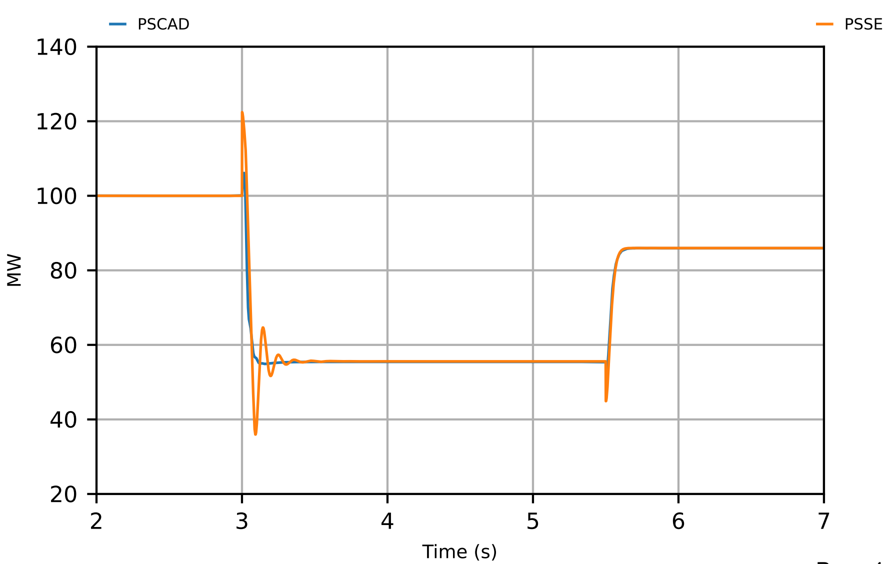
NSW DER Active Power



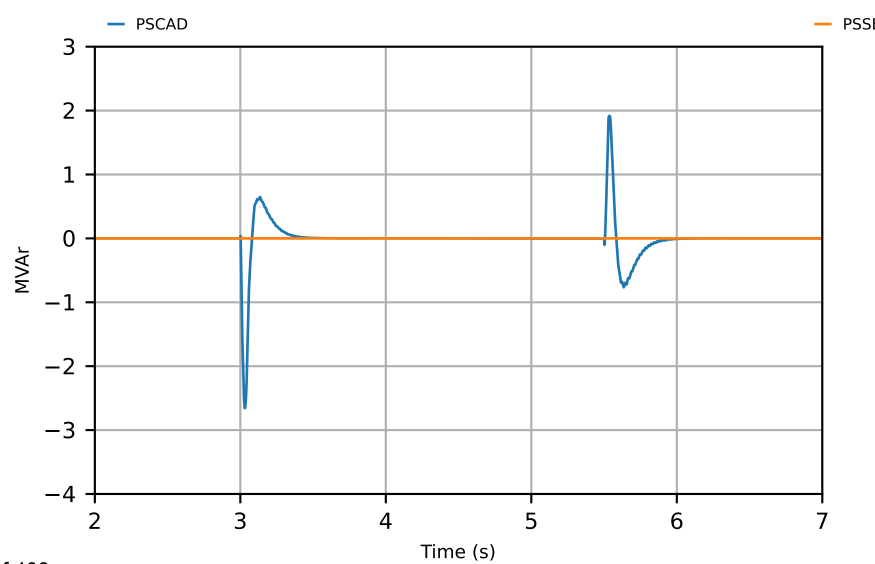
NSW DER Reactive Power



VIC DER Active Power

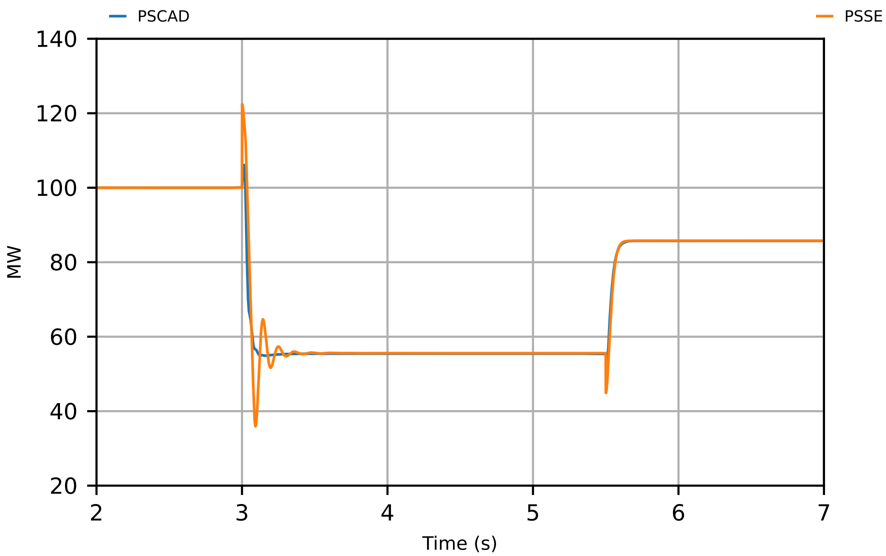


VIC DER Reactive Power

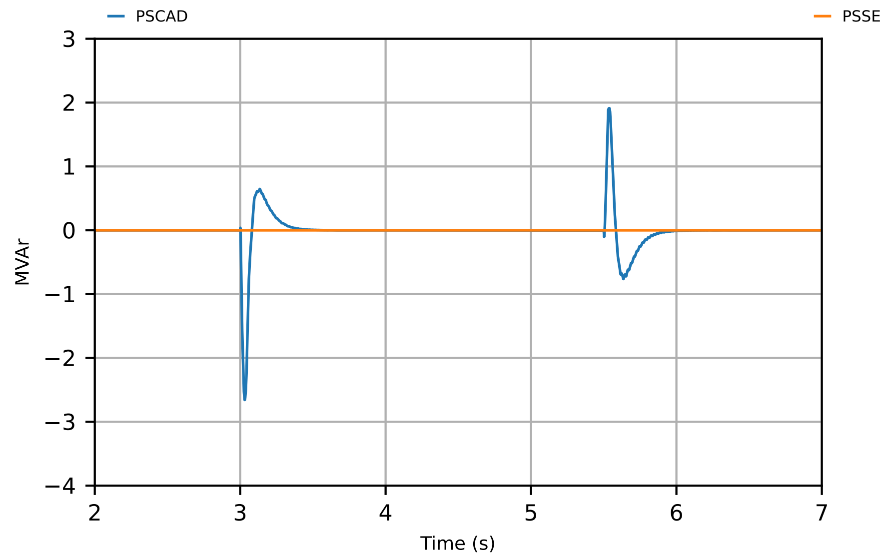


DER_SMIB_SCR_3_XR_3_T4_3

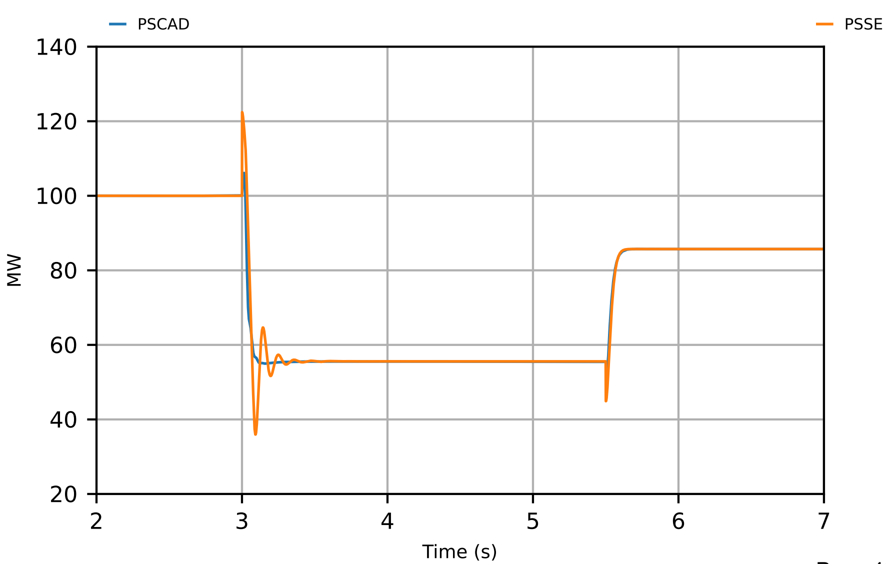
QLD DER Active Power



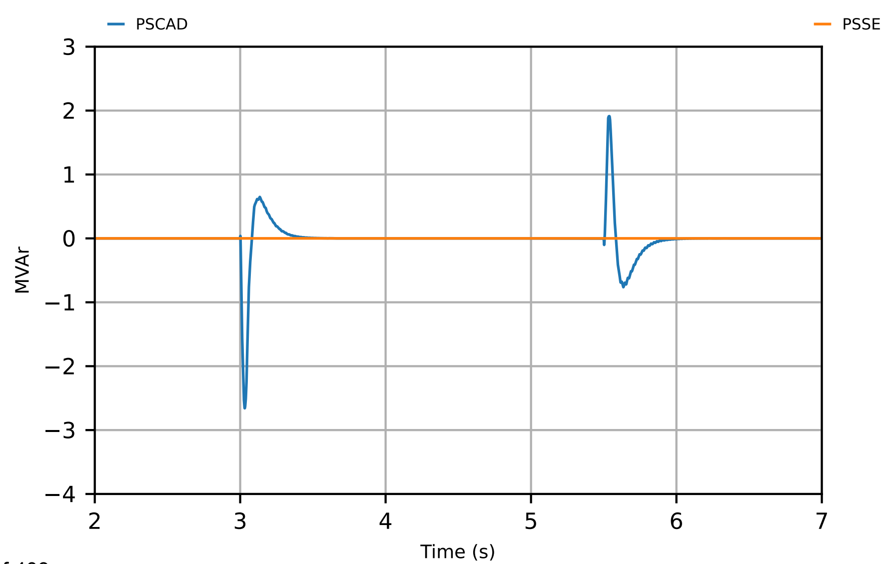
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power

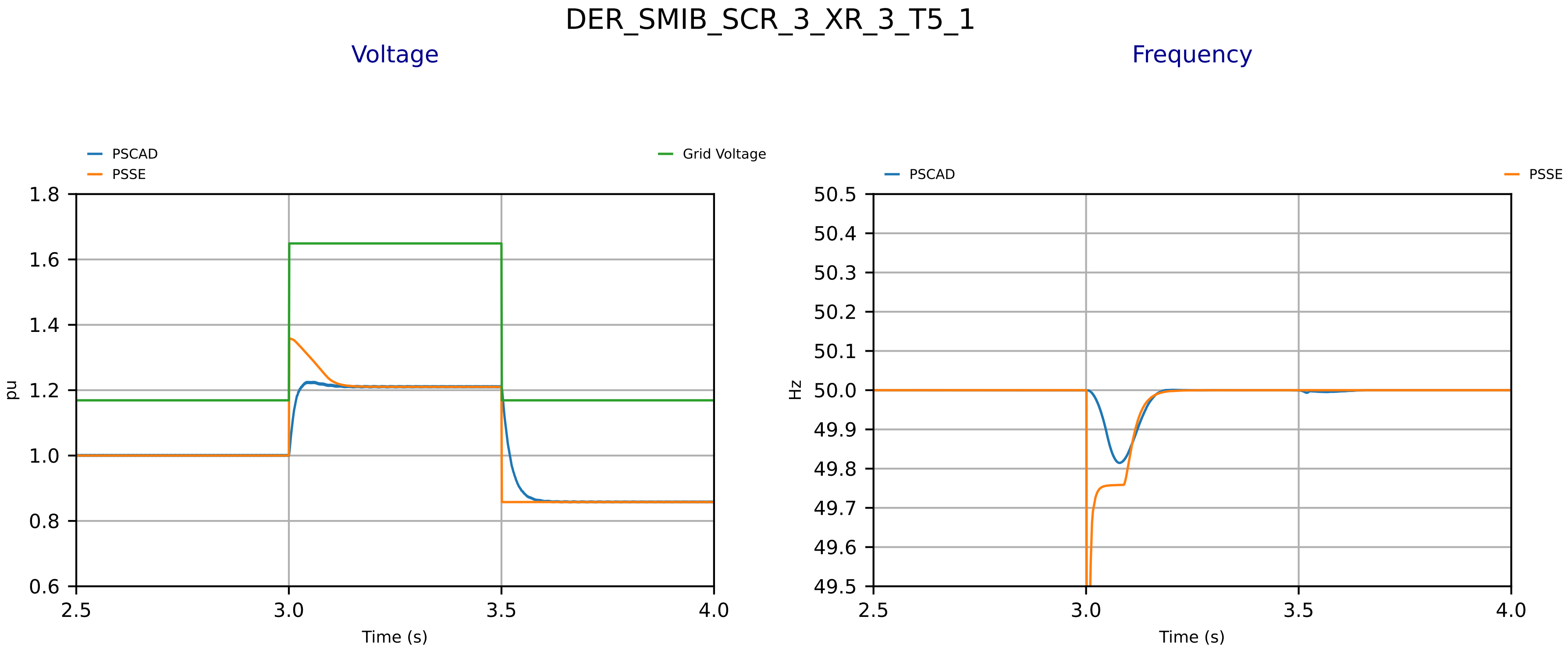


DER SMIB

SCR = 3, X/R = 3

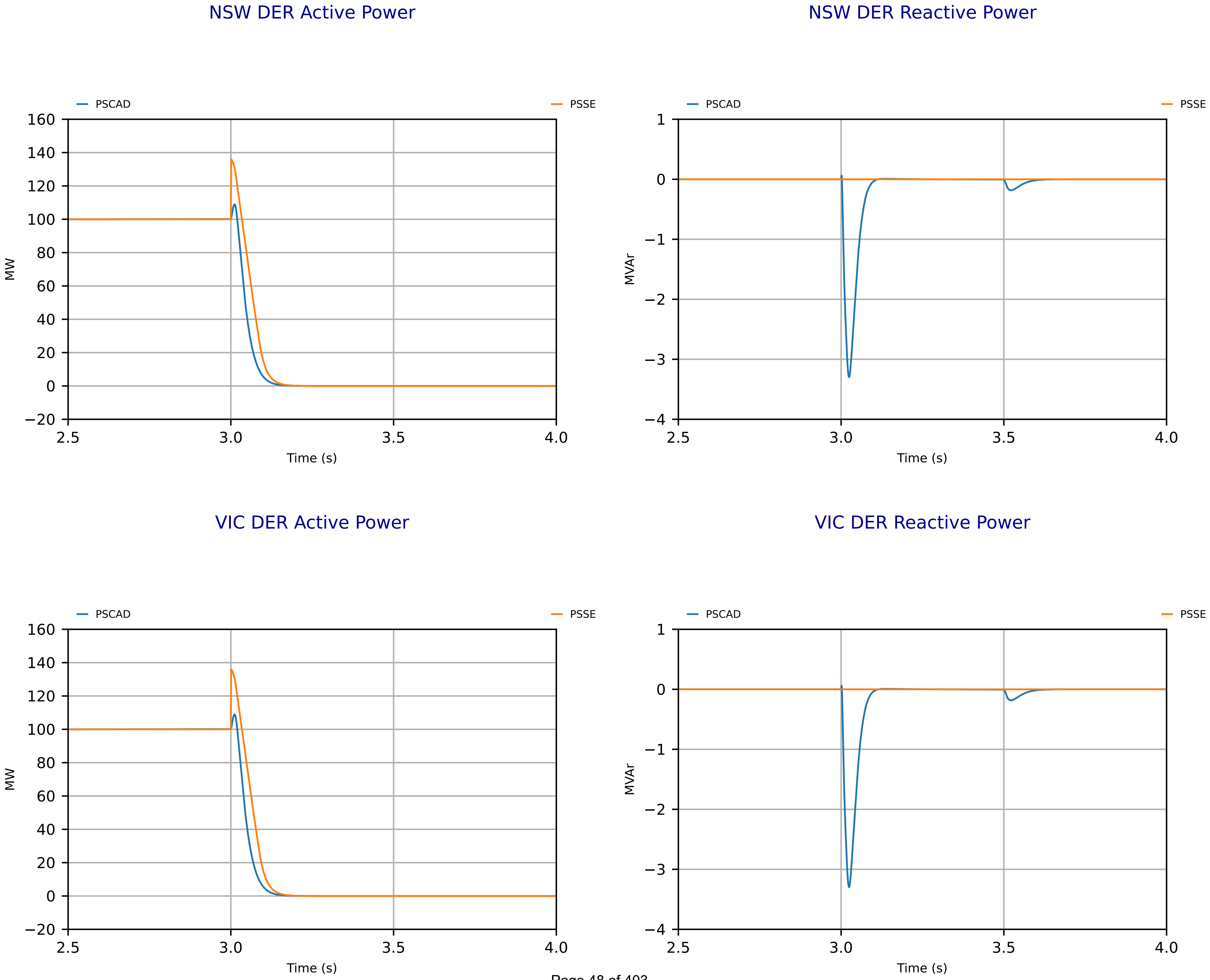
Test #5:

~120% Voltage disturbance for 500 ms



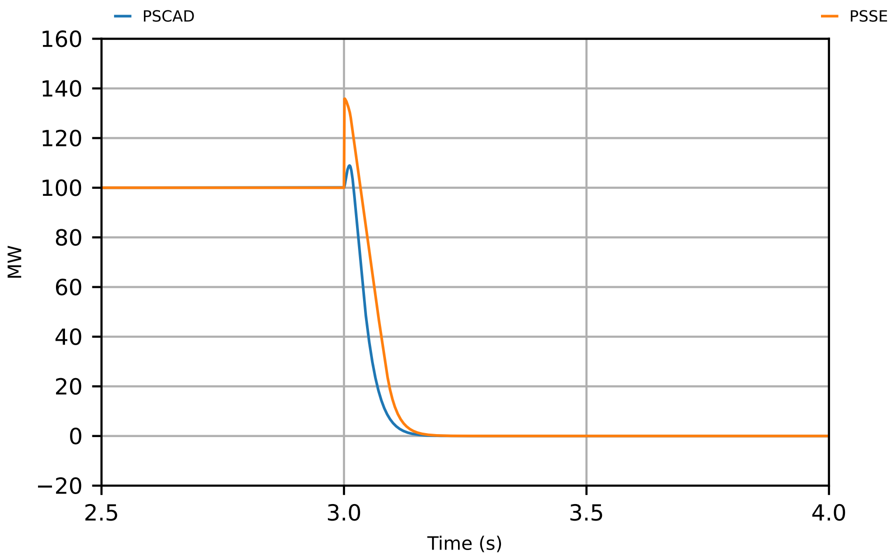
DER_SMIB_SCR_3_XR_3_T5_1
Voltage
Frequency
PSCAD
PSSE
Grid Voltage
pu
Hz
Time (s)
Time (s)

DER_SMIB_SCR_3_XR_3_T5_2

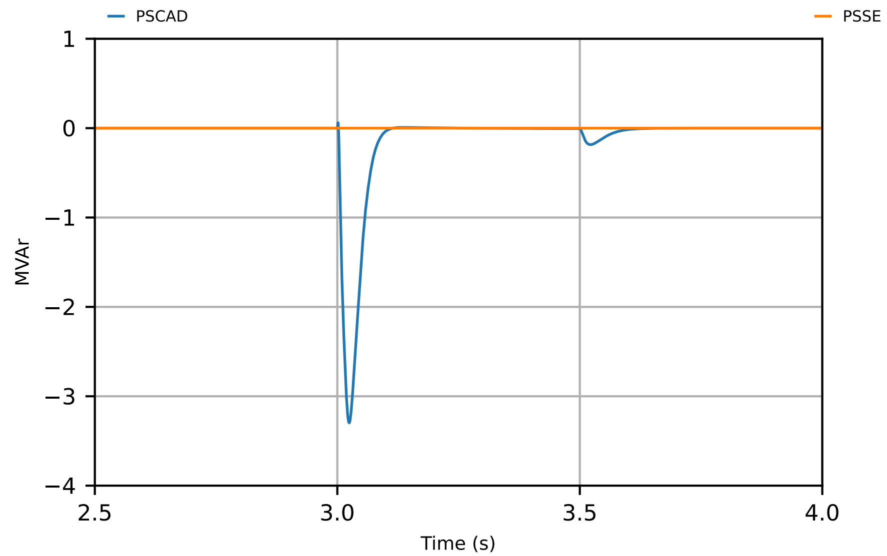


DER_SMIB_SCR_3_XR_3_T5_3

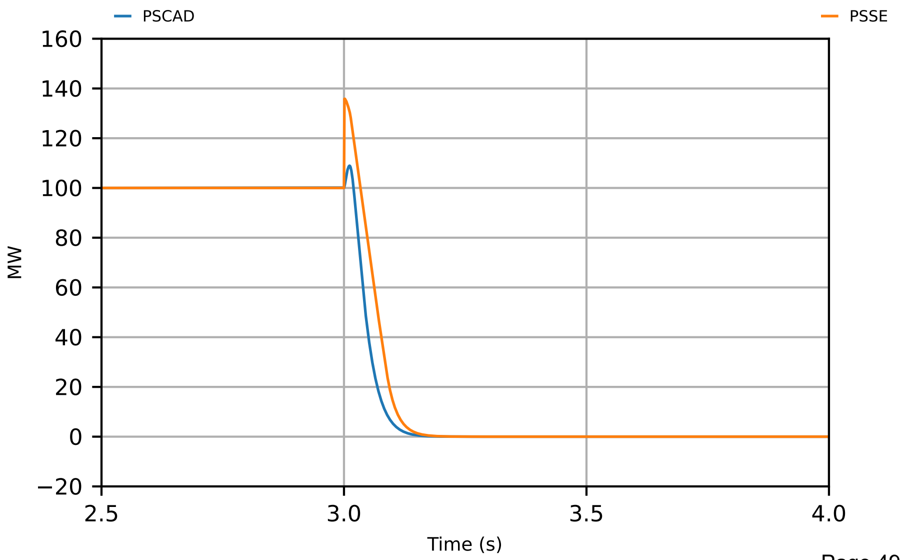
QLD DER Active Power



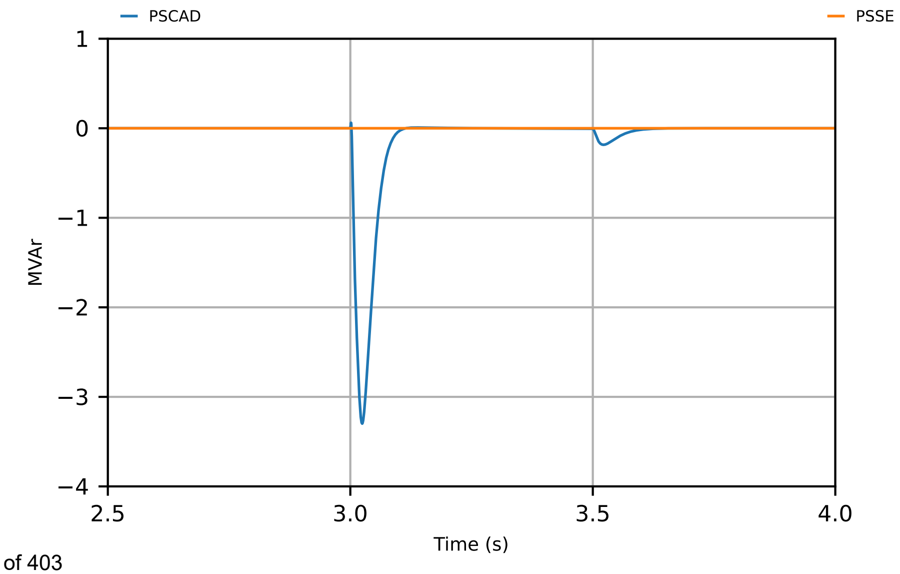
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



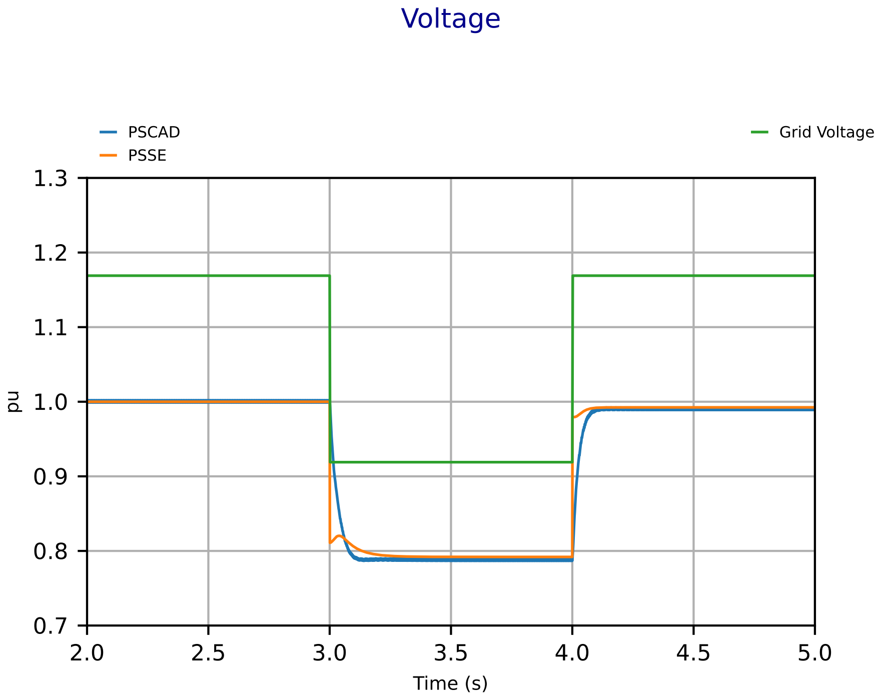
DER SMIB

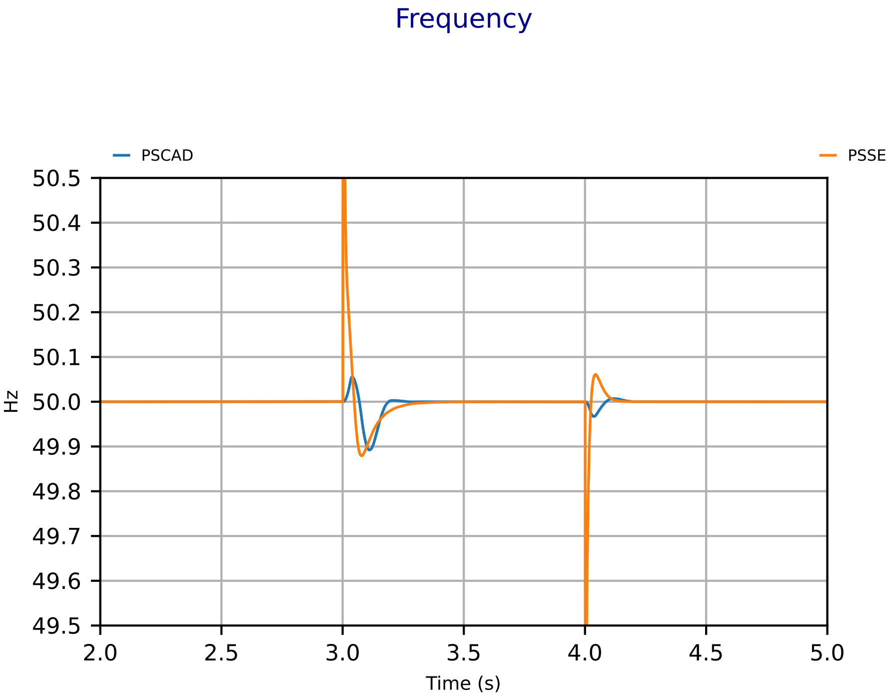
SCR = 3, X/R = 3

Test #6:

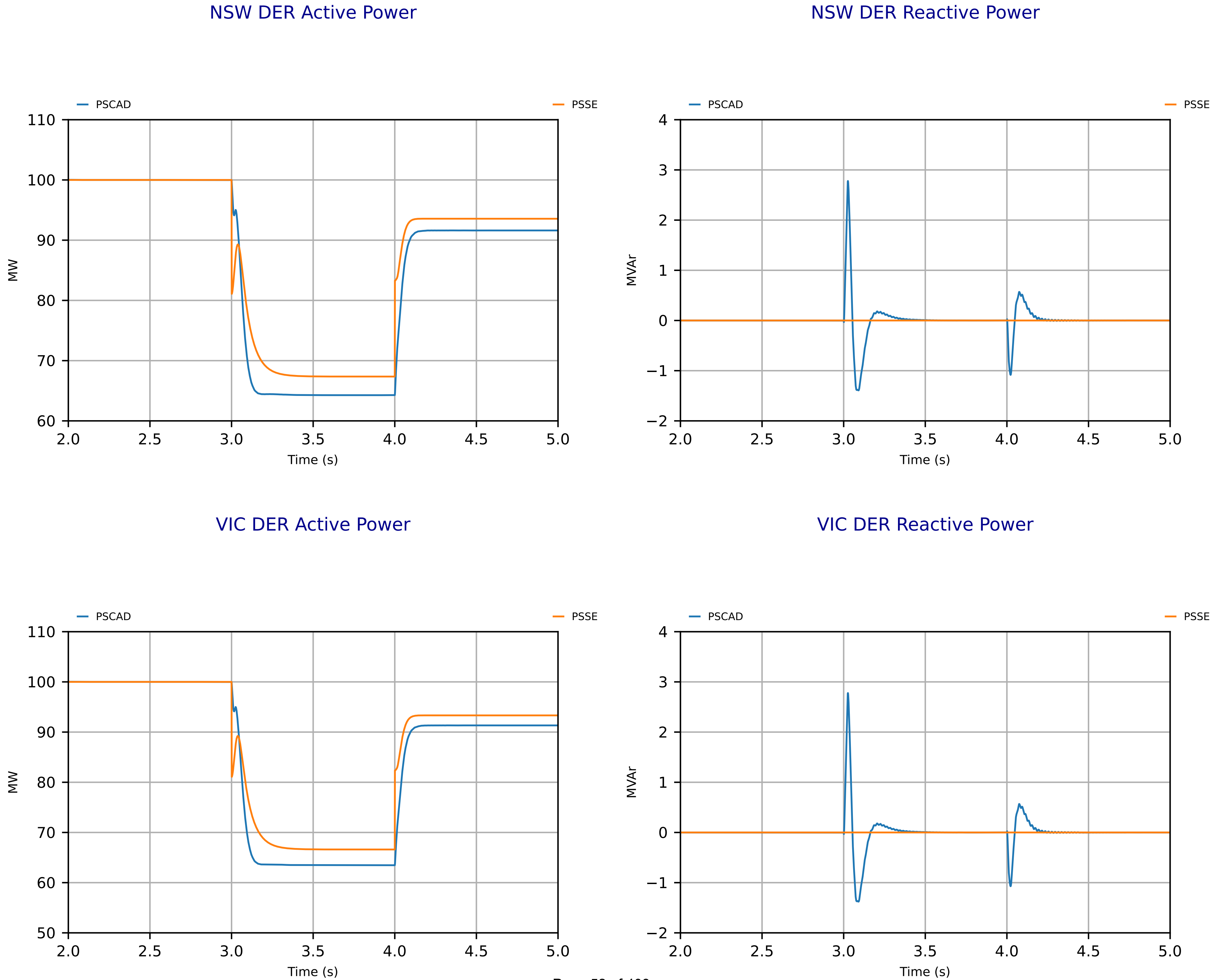
~80% Voltage disturbance for 1 sec

DER_SMIB_SCR_3_XR_3_T6_1



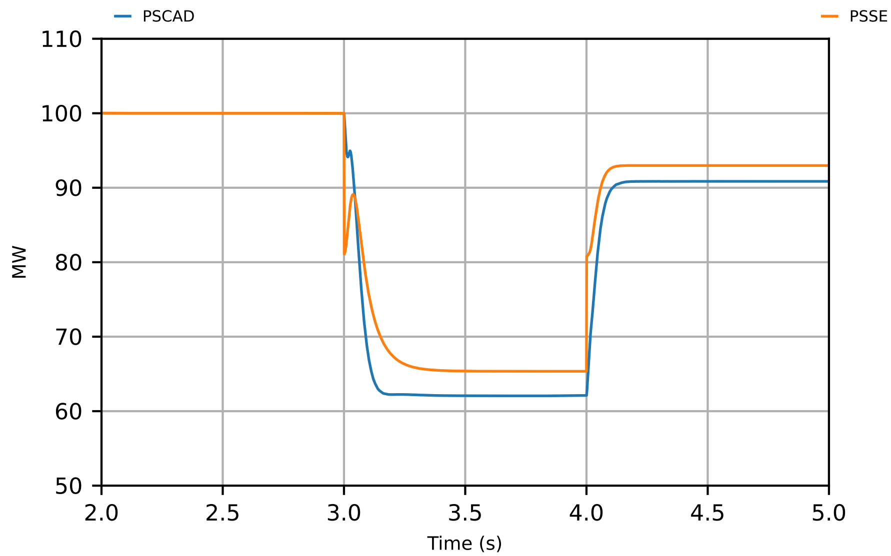


DER_SMIB_SCR_3_XR_3_T6_2

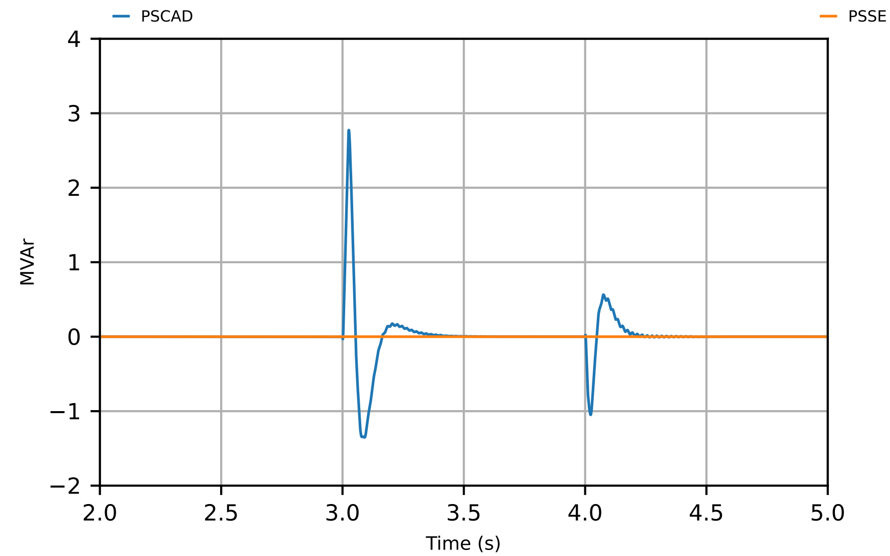


DER_SMIB_SCR_3_XR_3_T6_3

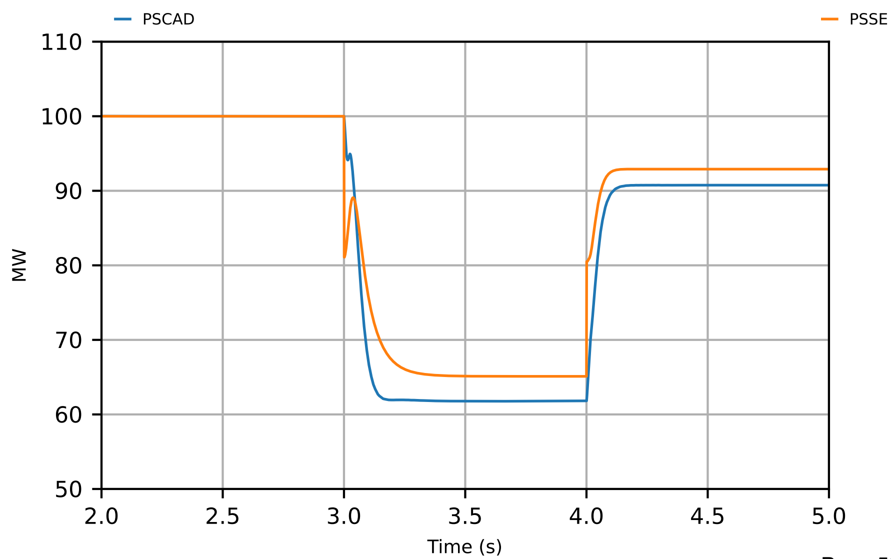
QLD DER Active Power



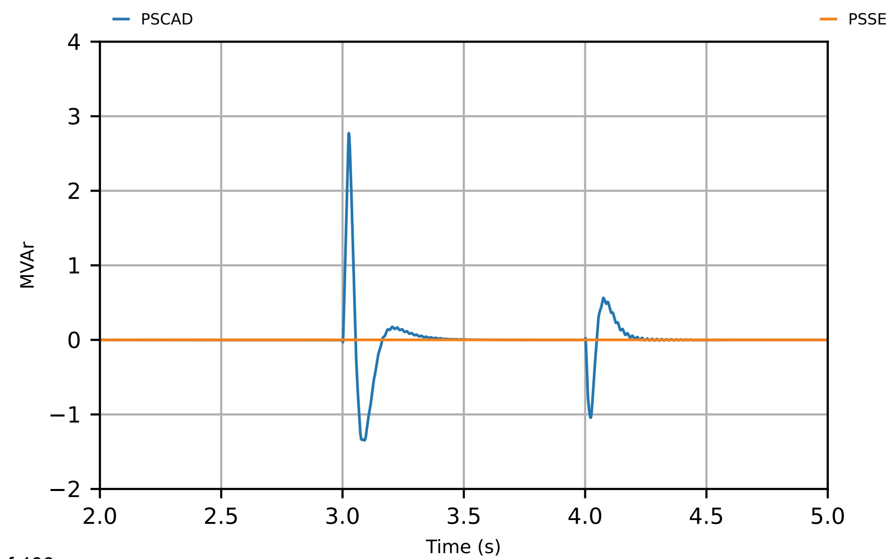
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



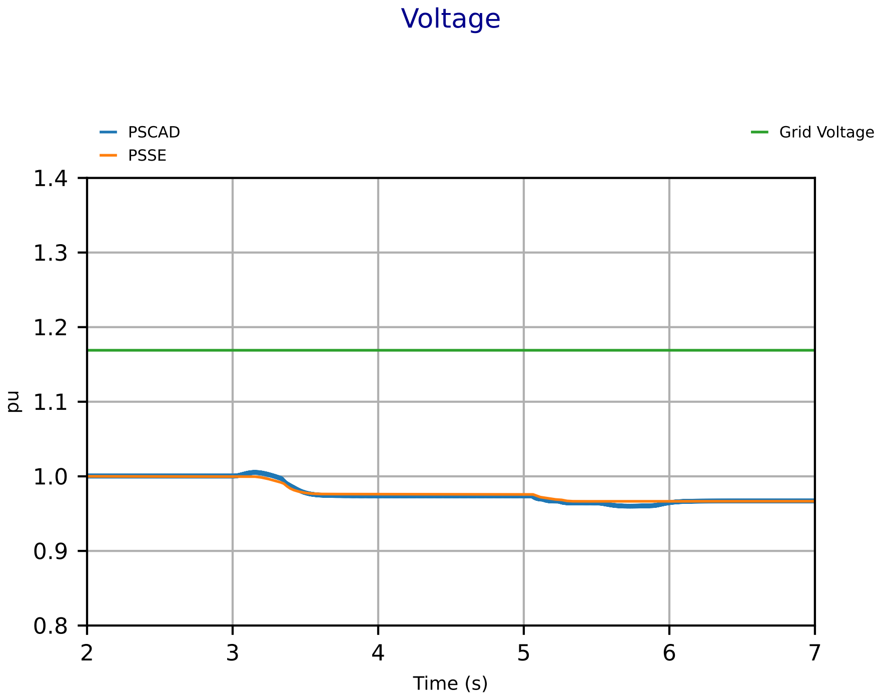
DER SMIB

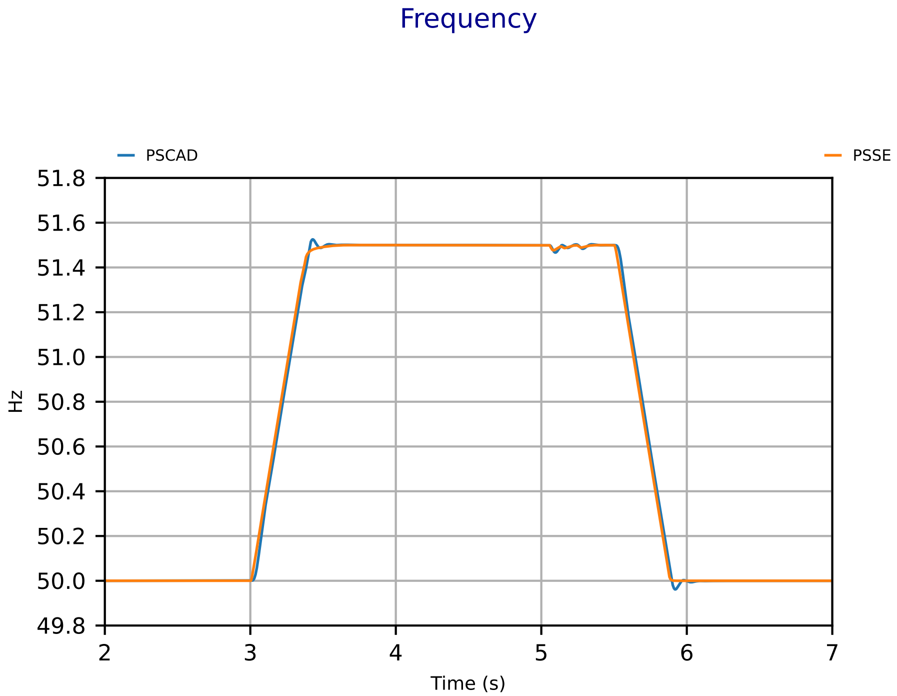
SCR = 3, X/R = 3

Test #7:

51.5 Hz frequency step for 2.5 sec (4 Hz/s)

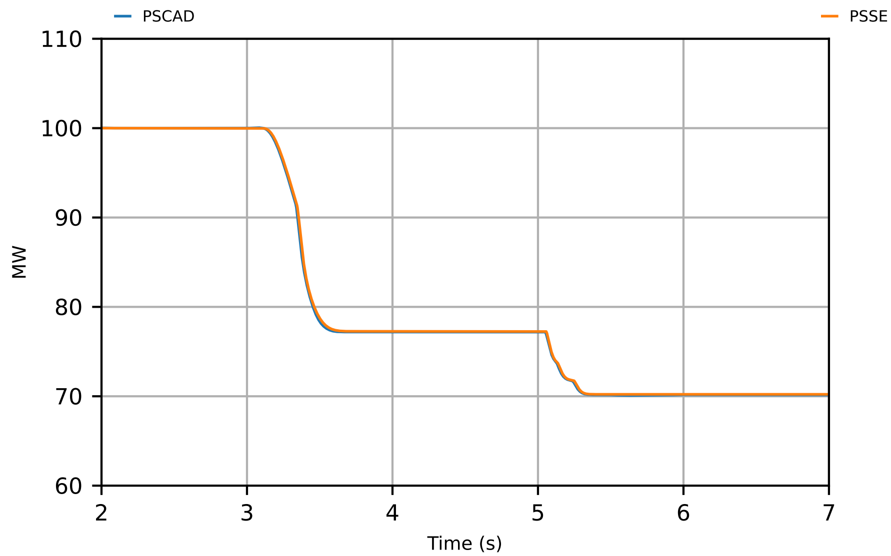
DER_SMIB_SCR_3_XR_3_T7_1



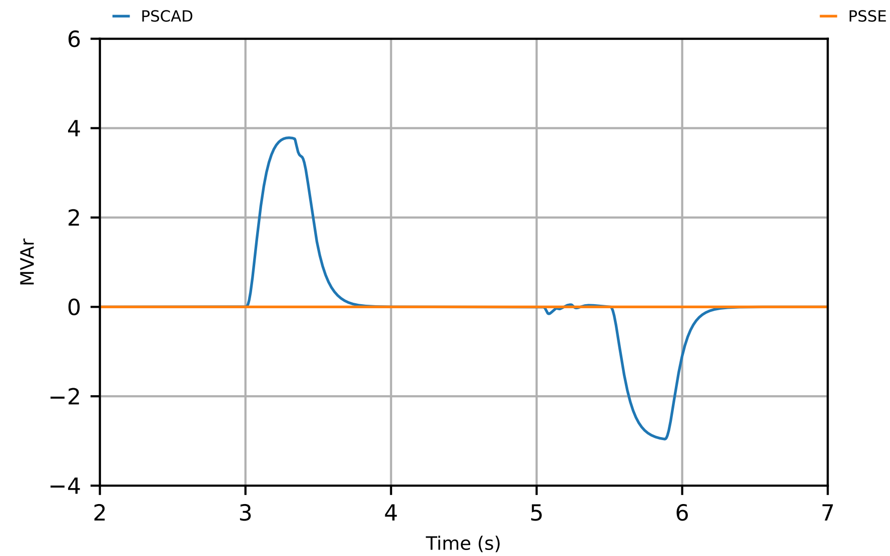


DER_SMIB_SCR_3_XR_3_T7_2

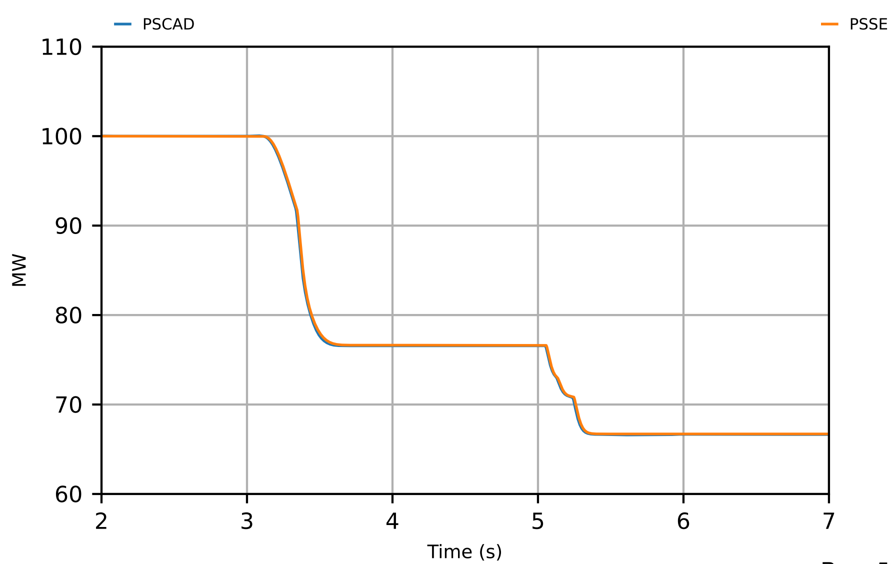
NSW DER Active Power



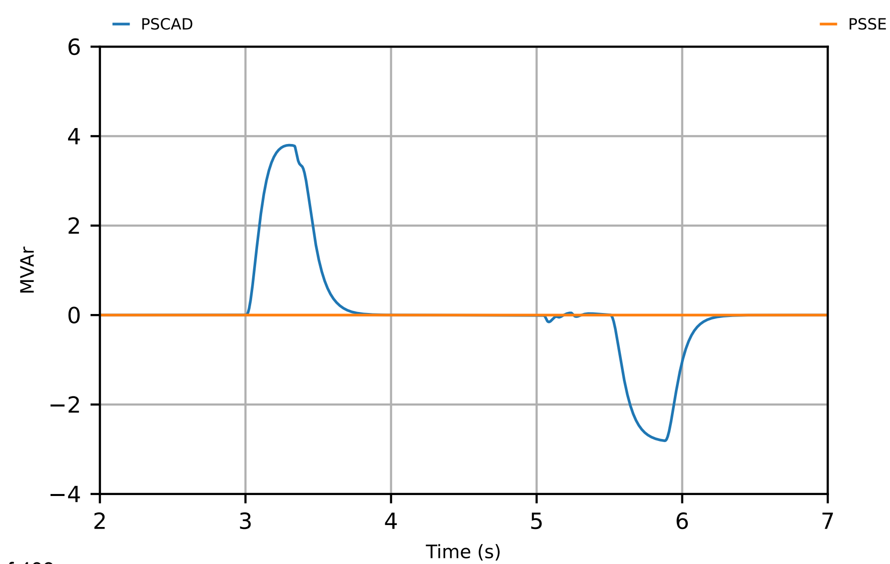
NSW DER Reactive Power



VIC DER Active Power

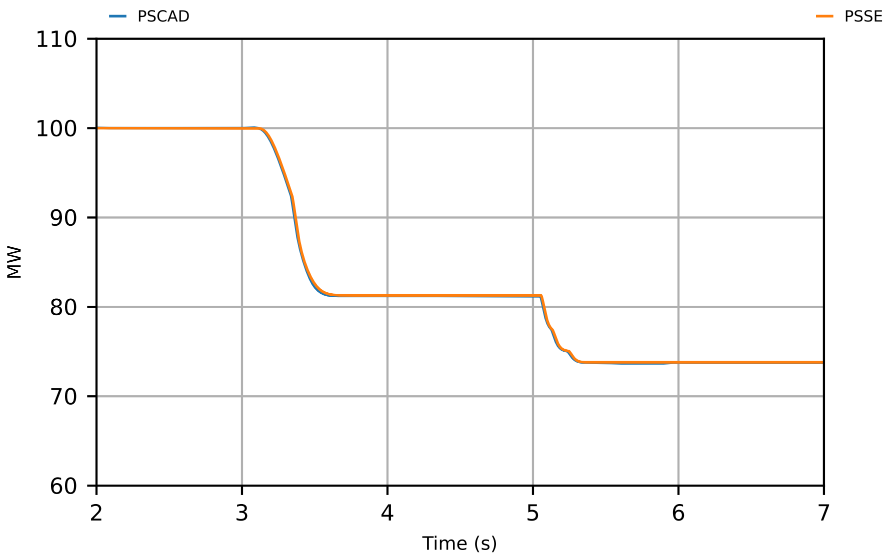


VIC DER Reactive Power

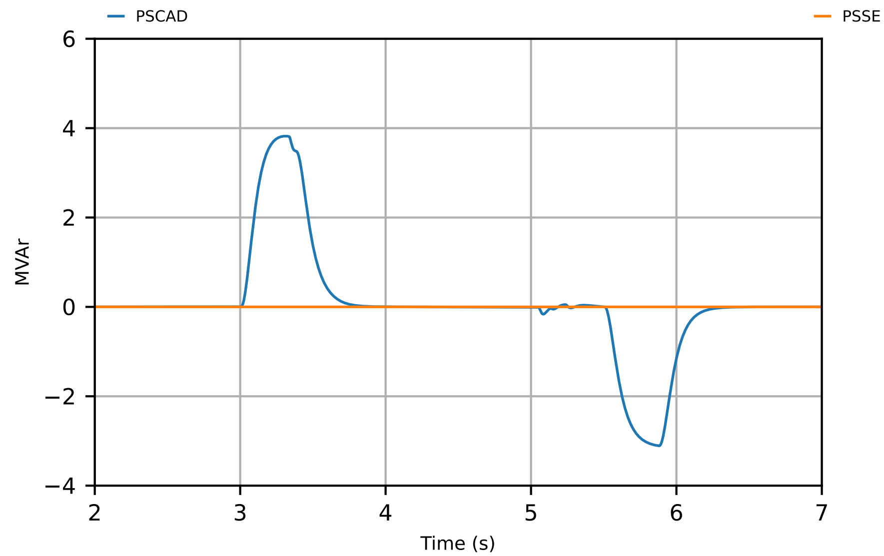


DER_SMIB_SCR_3_XR_3_T7_3

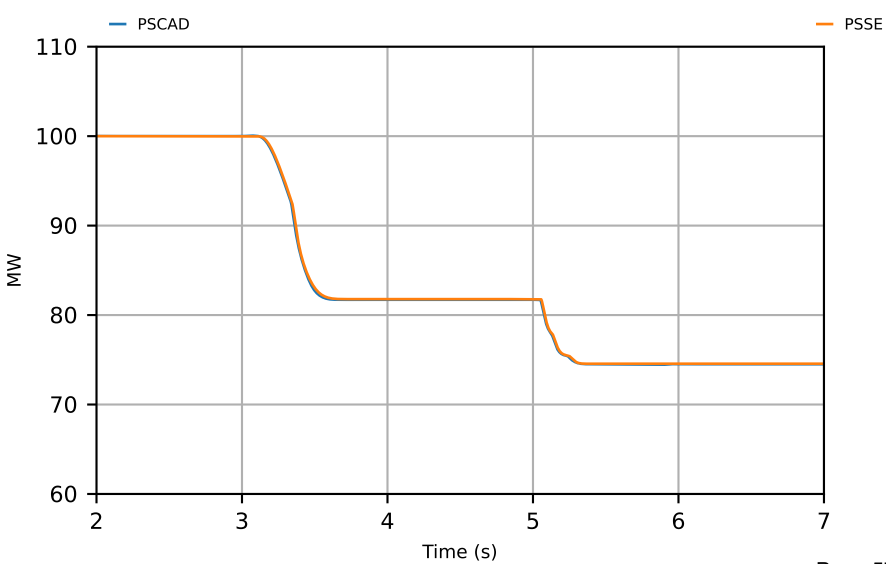
QLD DER Active Power



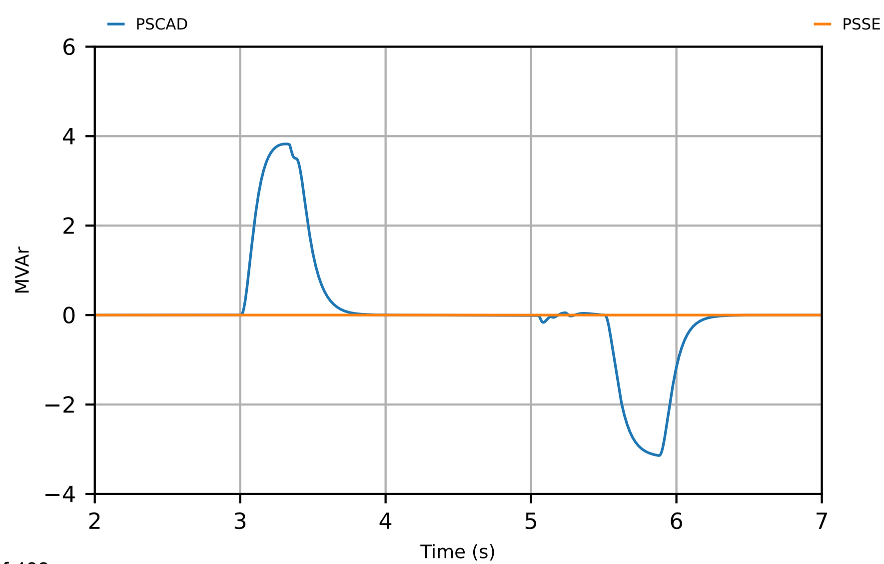
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



DER SMIB

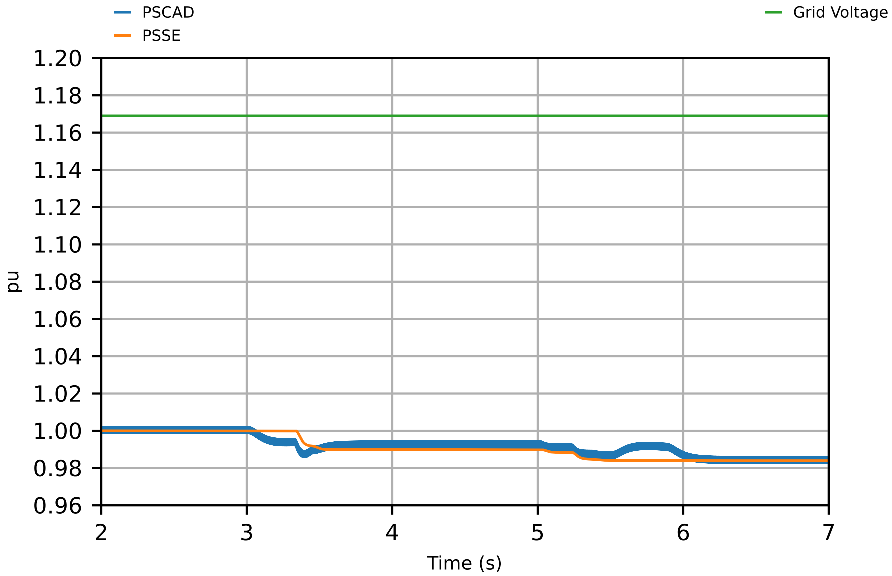
SCR = 3, X/R = 3

Test #8:

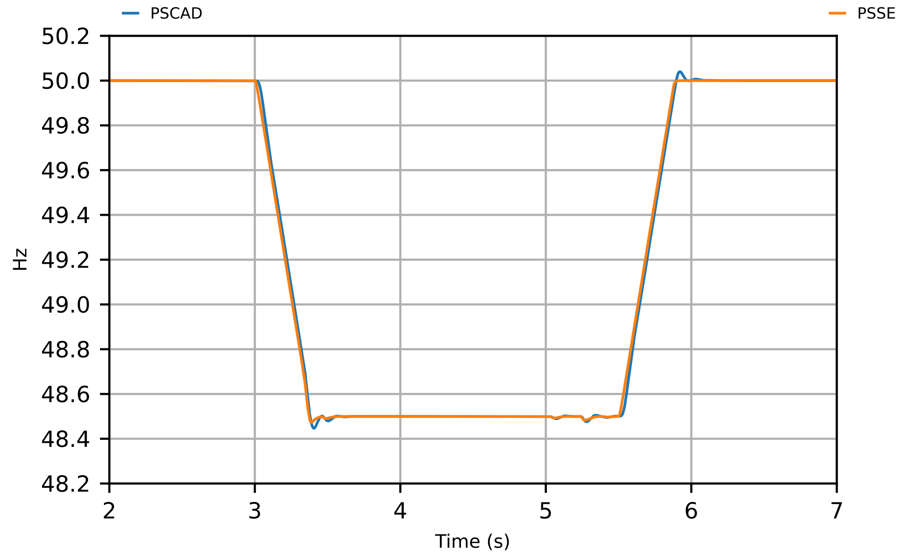
48.5 Hz frequency step for 2.5 sec (4 Hz/s)

DER_SMIB_SCR_3_XR_3_T8_1

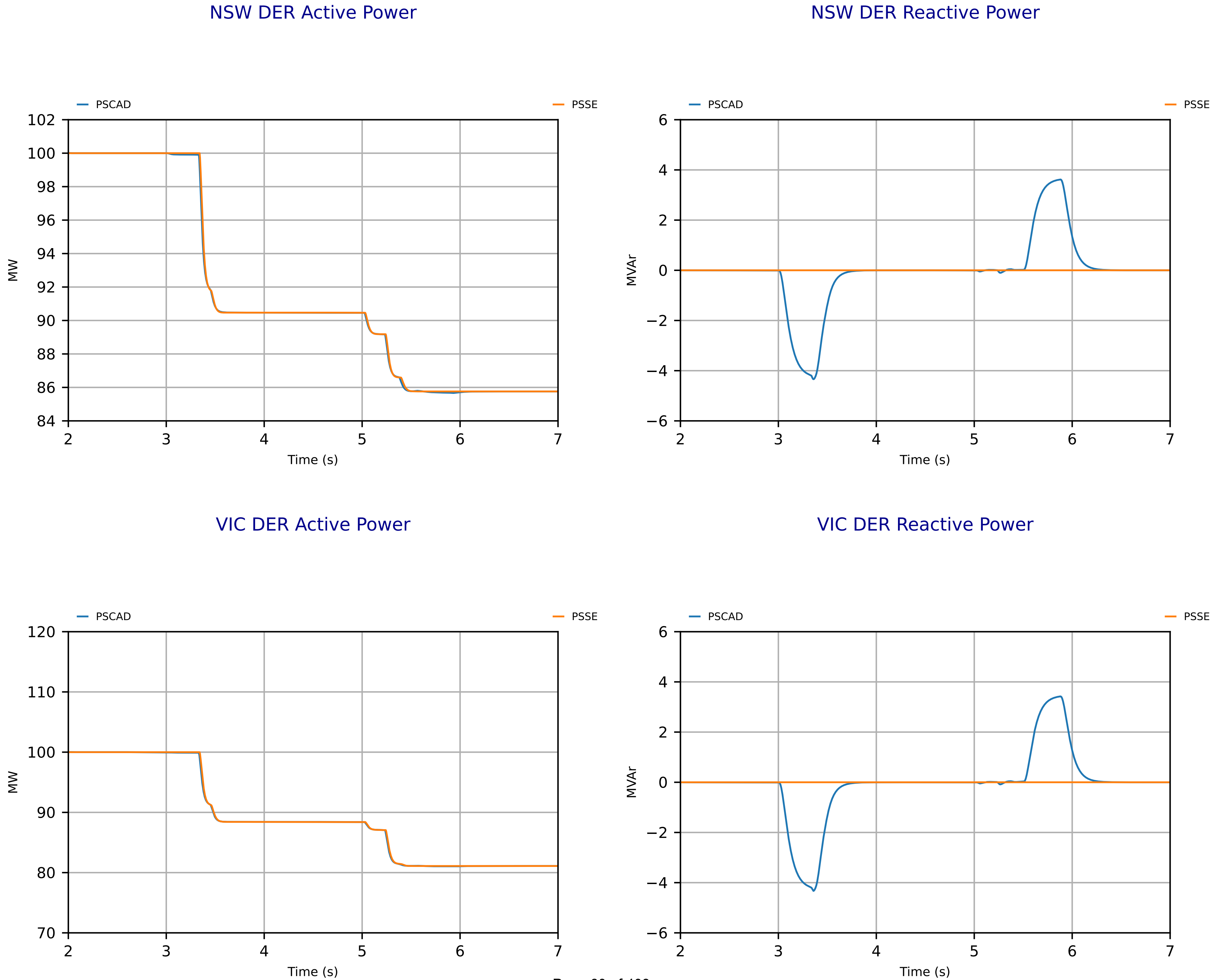
Voltage

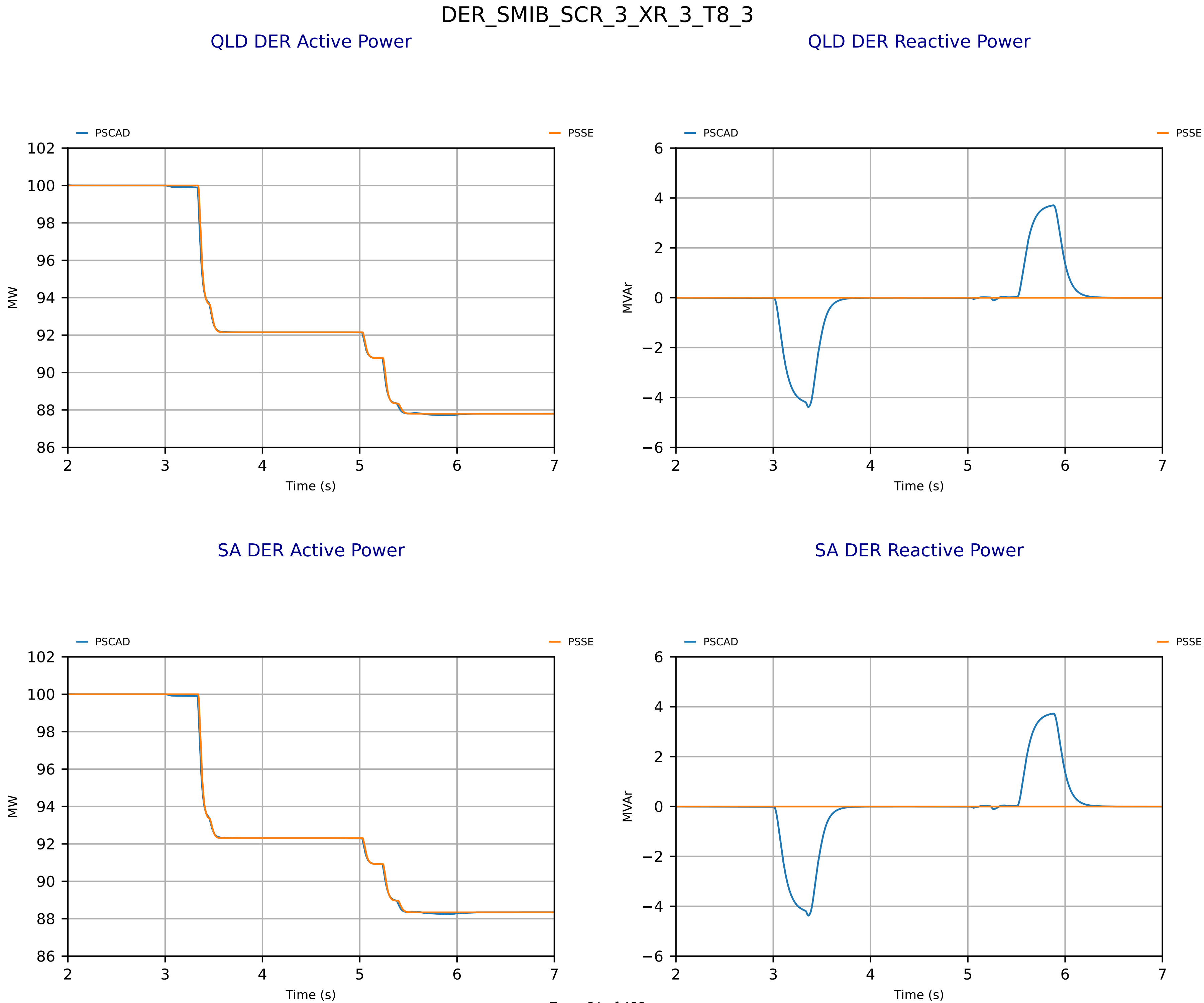


Frequency



DER_SMIB_SCR_3_XR_3_T8_2




DER_SMIB_SCR_3_XR_3_T8_3
QLD DER Active Power
QLD DER Reactive Power
SA DER Active Power
SA DER Reactive Power
PSCAD
PSSE
MW
MVAr
Time (s)

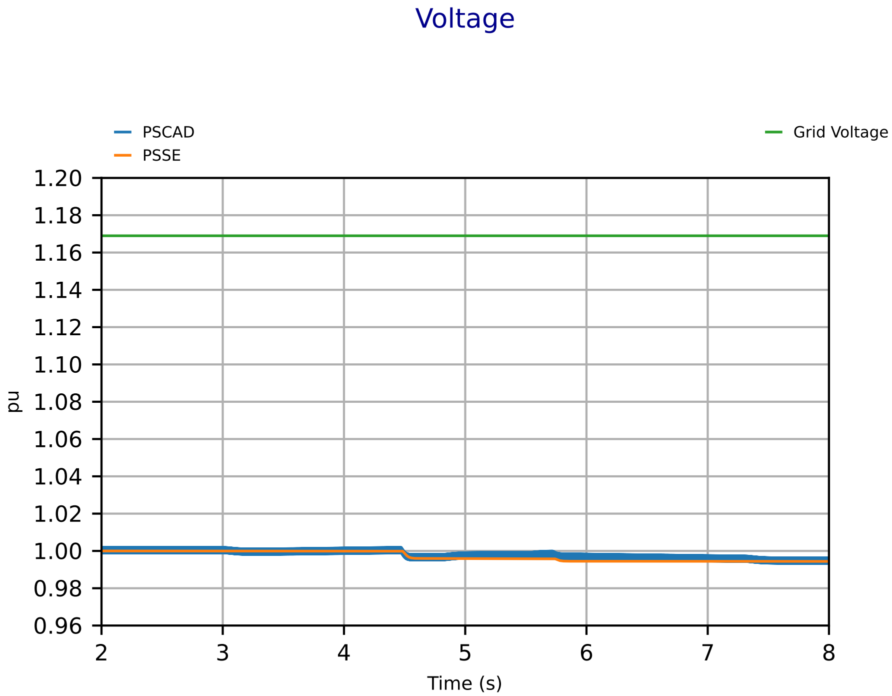
DER SMIB

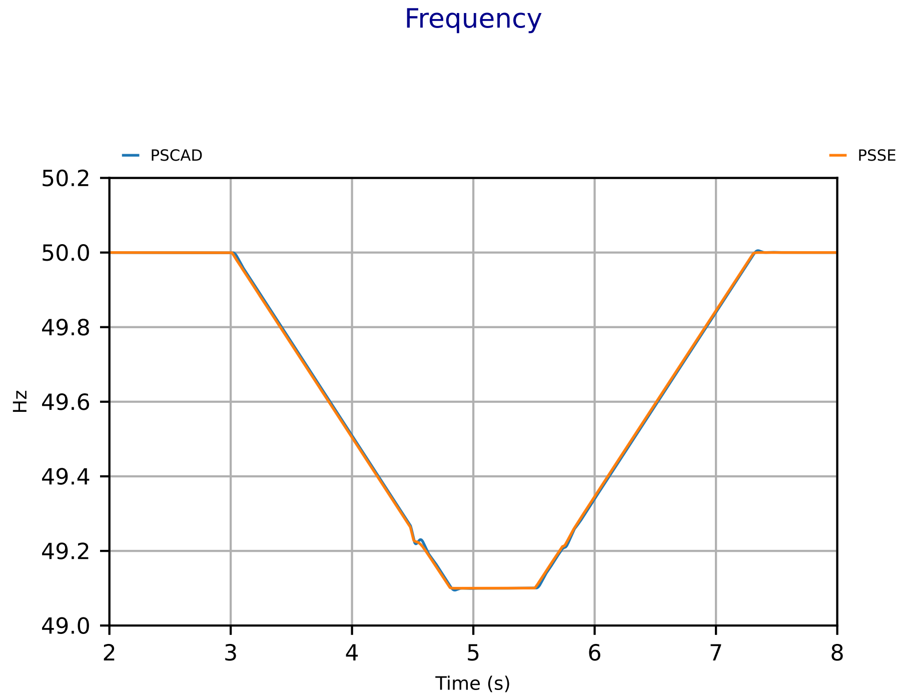
SCR = 3, X/R = 3

Test #9:

49.1 Hz slow frequency ramp (0.5 Hz/s)

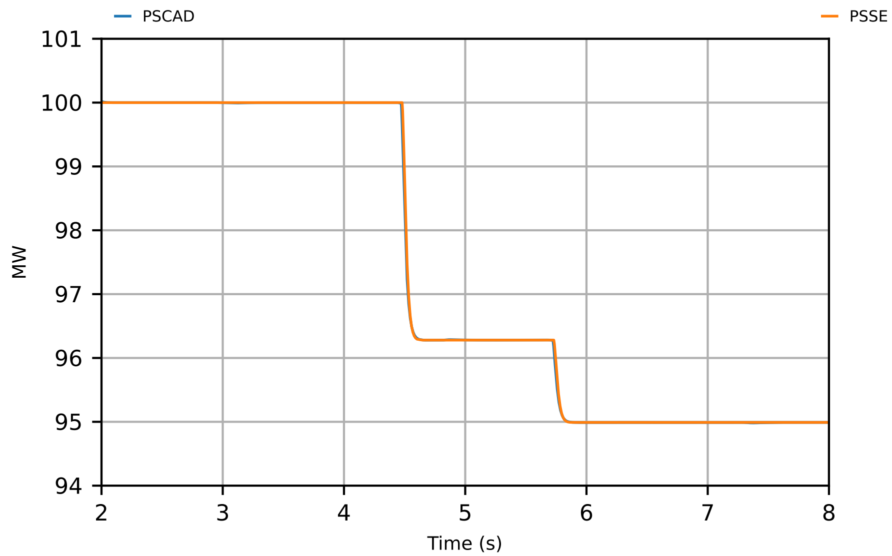
DER_SMIB_SCR_3_XR_3_T9_1



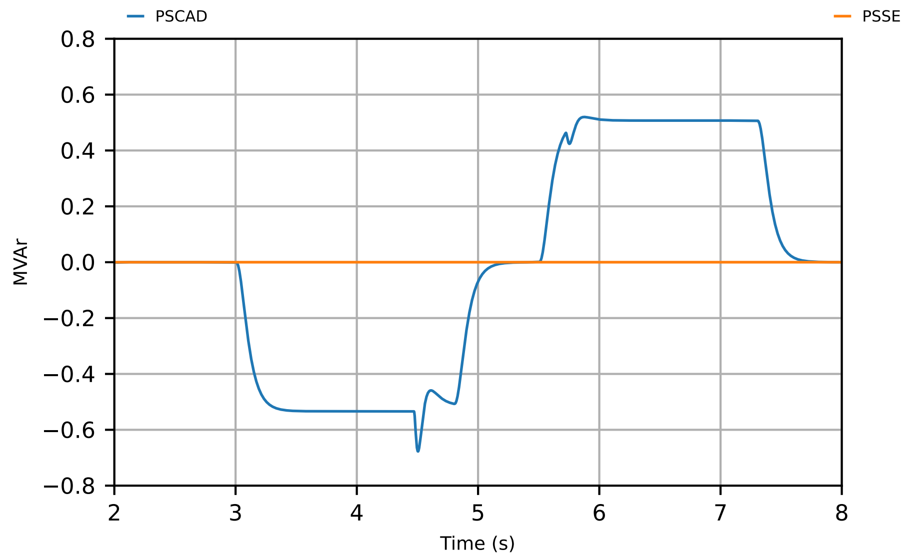


DER_SMIB_SCR_3_XR_3_T9_2

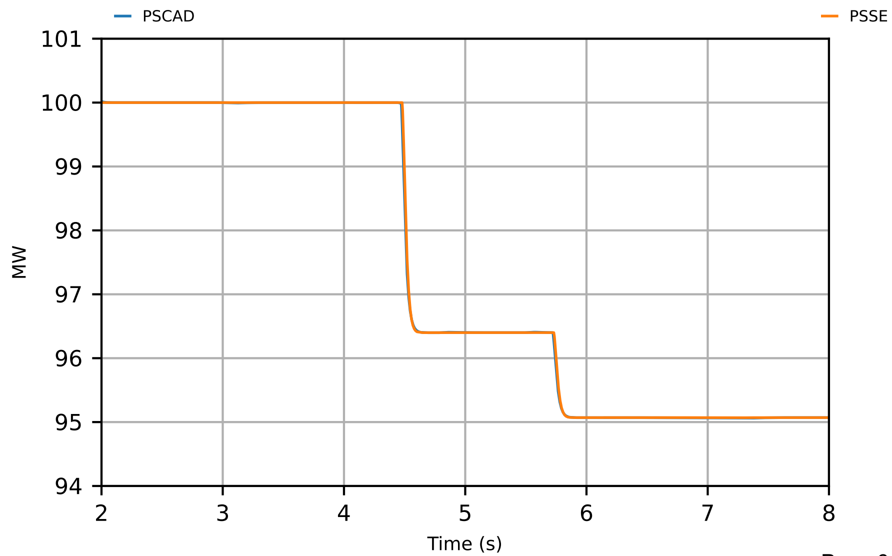
NSW DER Active Power



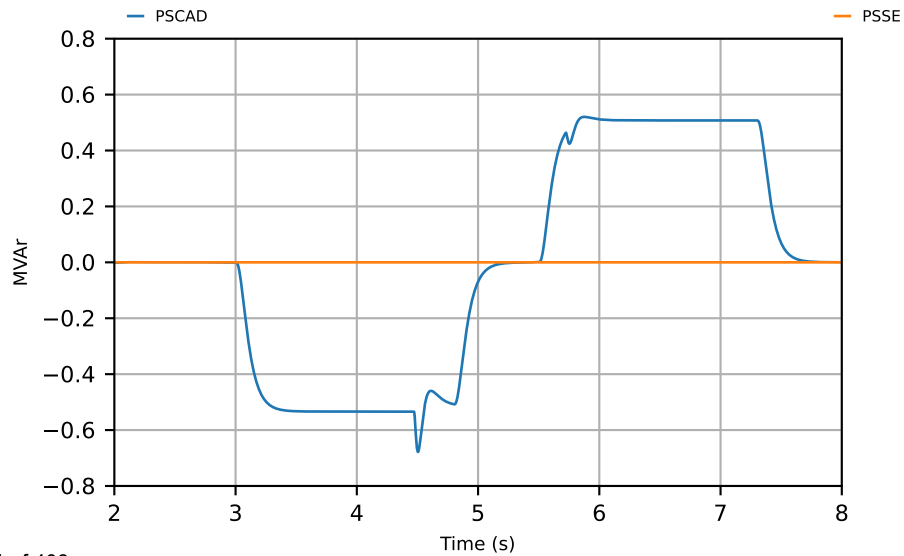
NSW DER Reactive Power



VIC DER Active Power

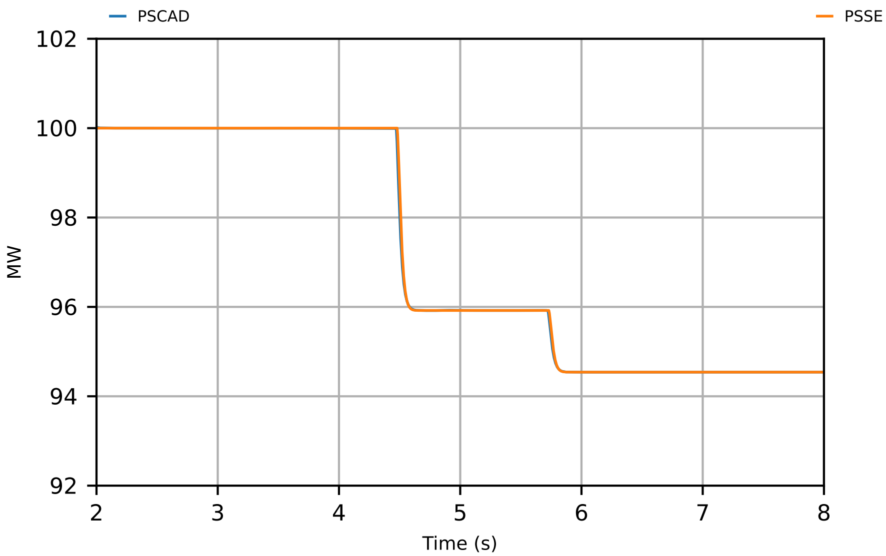


VIC DER Reactive Power

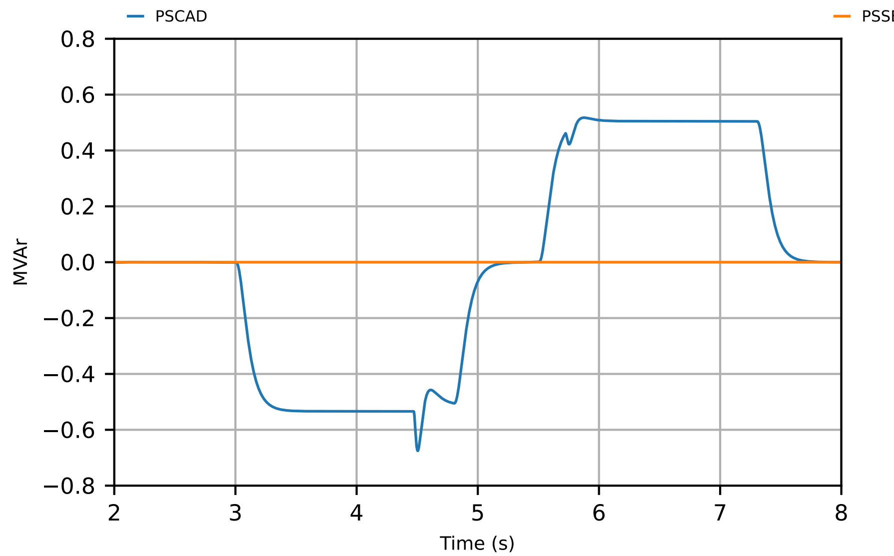


DER_SMIB_SCR_3_XR_3_T9_3

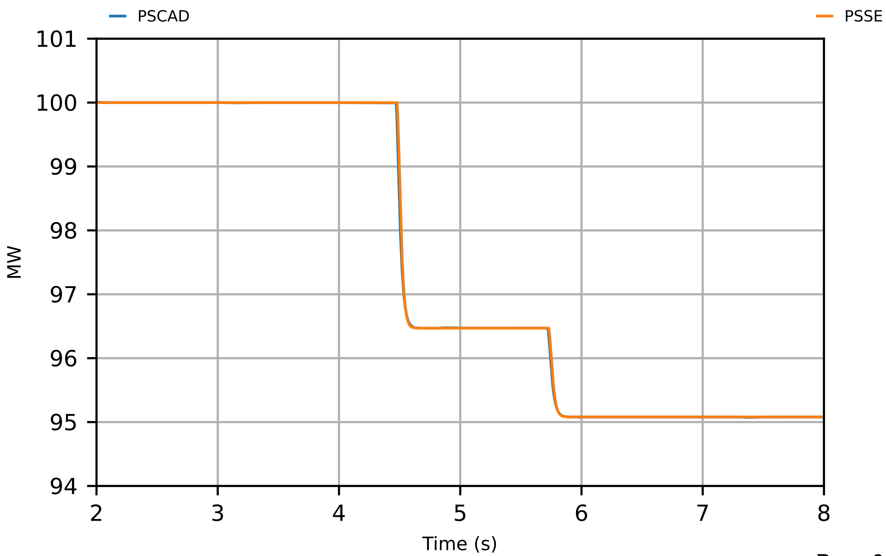
QLD DER Active Power



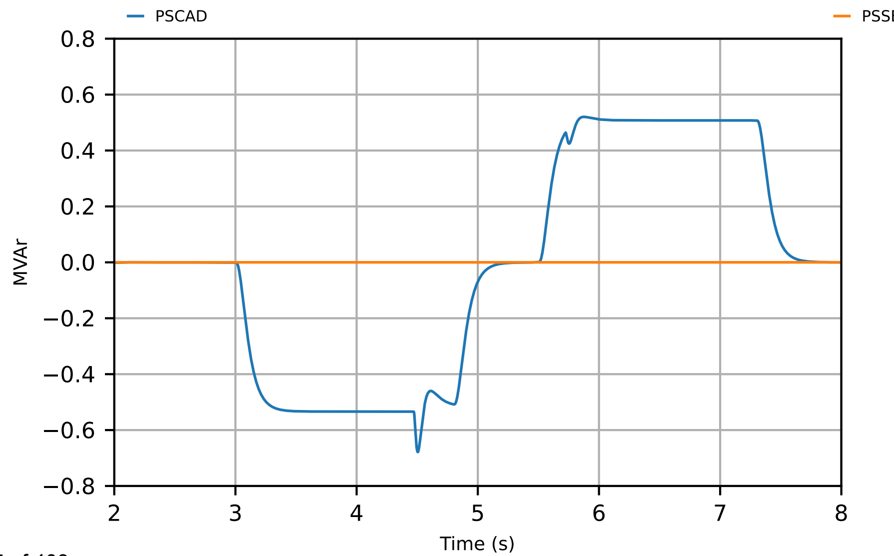
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power

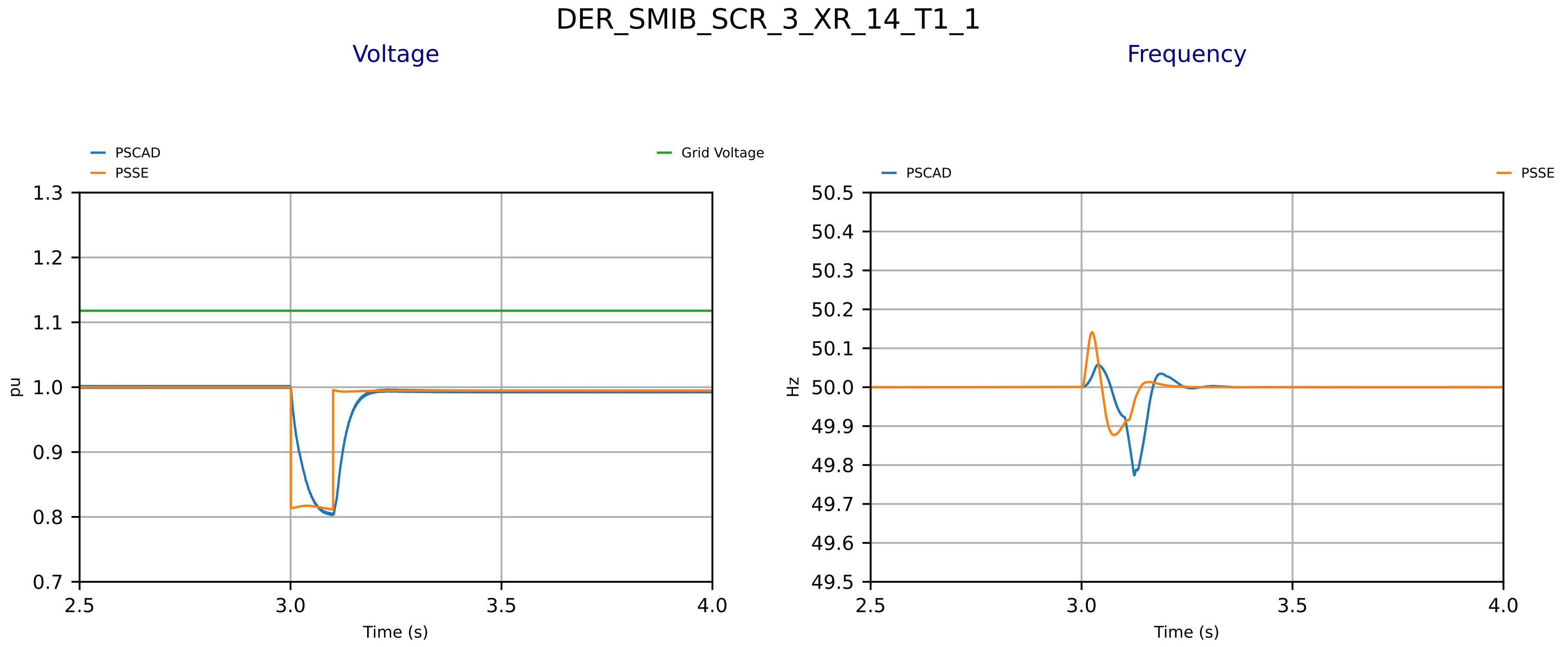


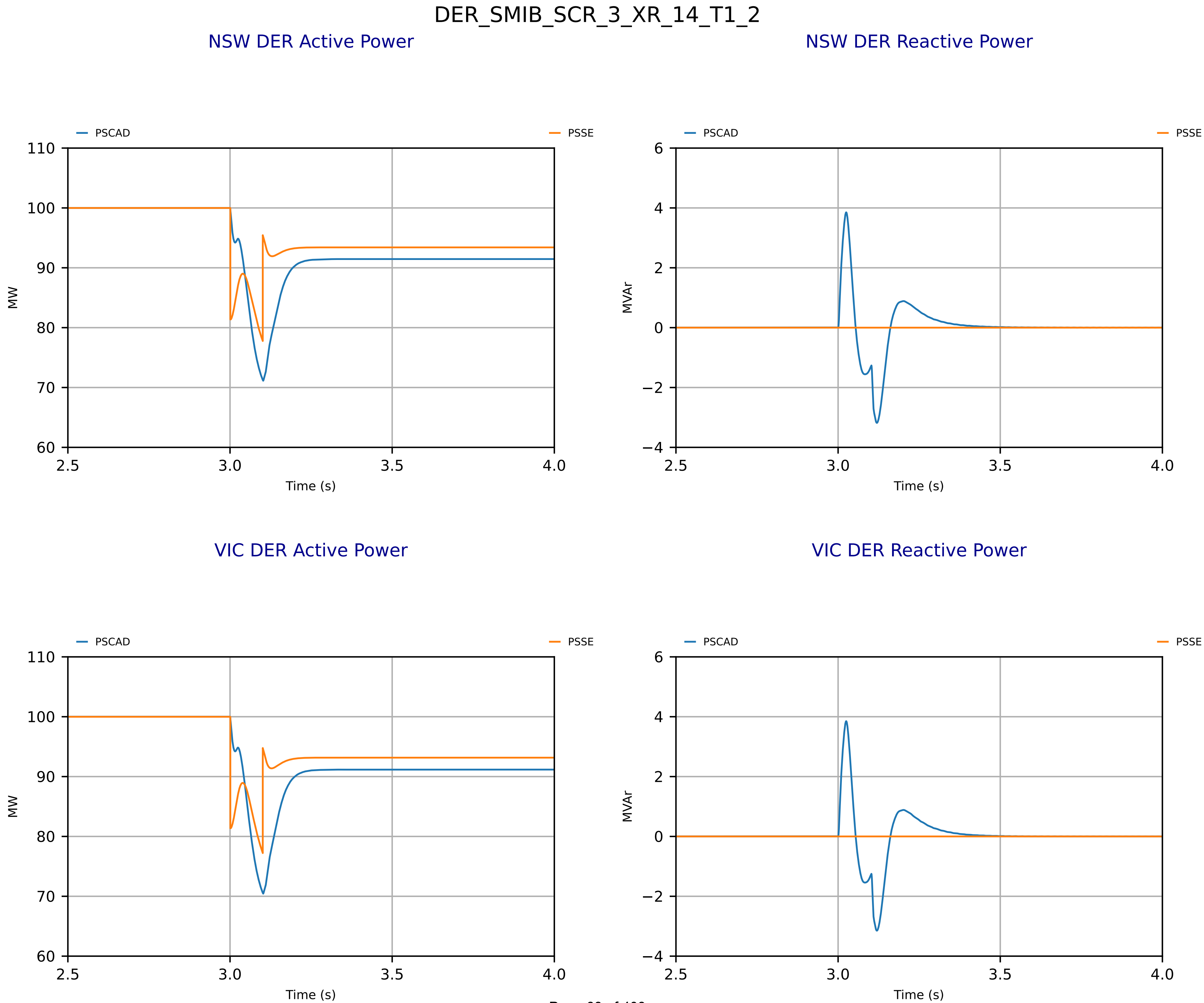
DER SMIB

SCR = 3, X/R = 14

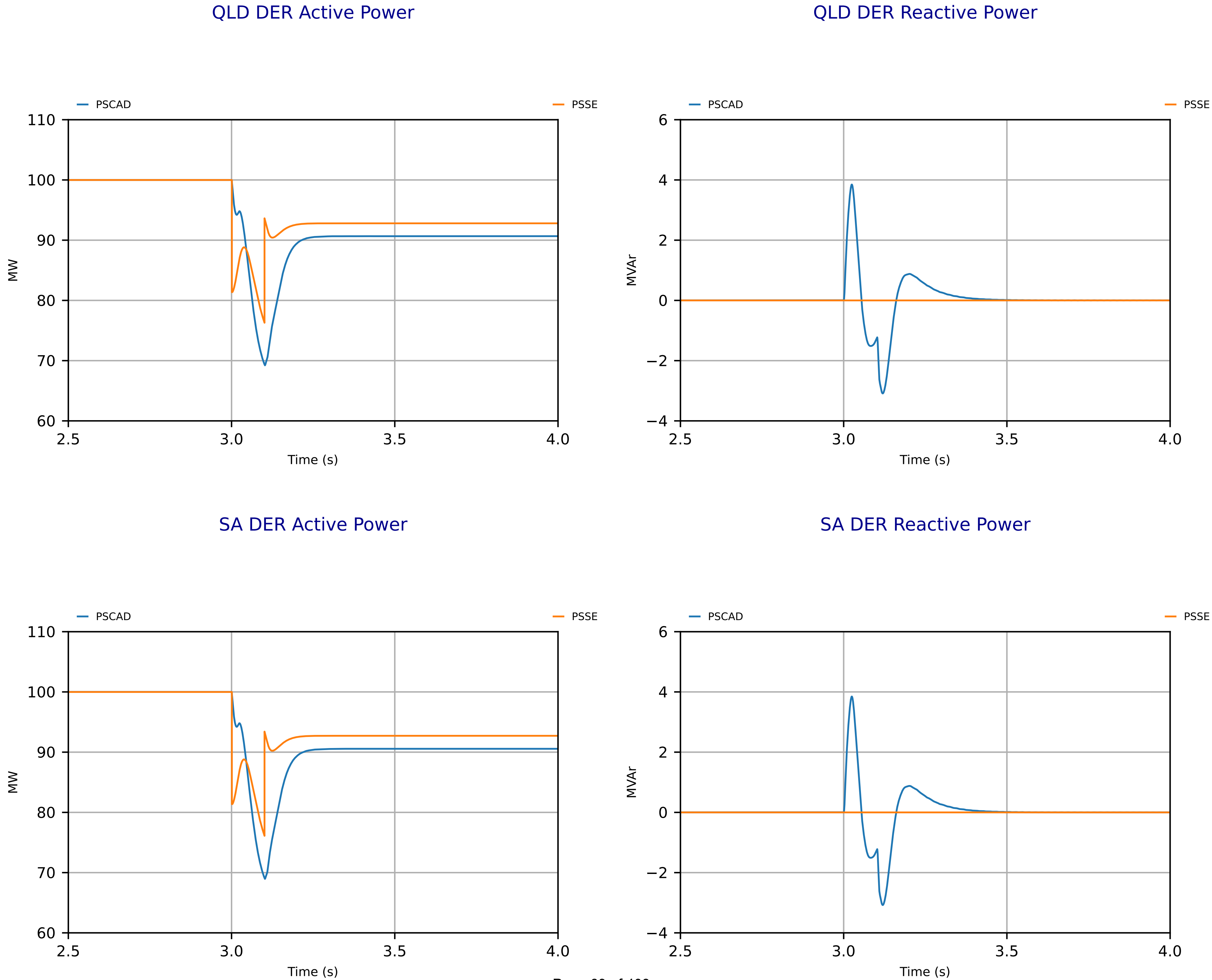
Test #1:

LG fault for 100 ms


DER_SMIB_SCR_3_XR_14_T1_1
Voltage
Frequency
PSCAD
PSSE
Grid Voltage
pu
Hz
Time (s)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
50.5
50.4
50.3
50.2
50.1
50.0
49.9
49.8
49.7
49.6
49.5
2.5
3.0
3.5
4.0


DER_SMIB_SCR_3_XR_14_T1_2
NSW DER Active Power
NSW DER Reactive Power
VIC DER Active Power
VIC DER Reactive Power
PSCAD
PSSE
MW
MVAr
Time (s)
110
100
90
80
70
60
6
4
2
0
−2
−4
2.5
3.0
3.5
4.0

DER_SMIB_SCR_3_XR_14_T1_3



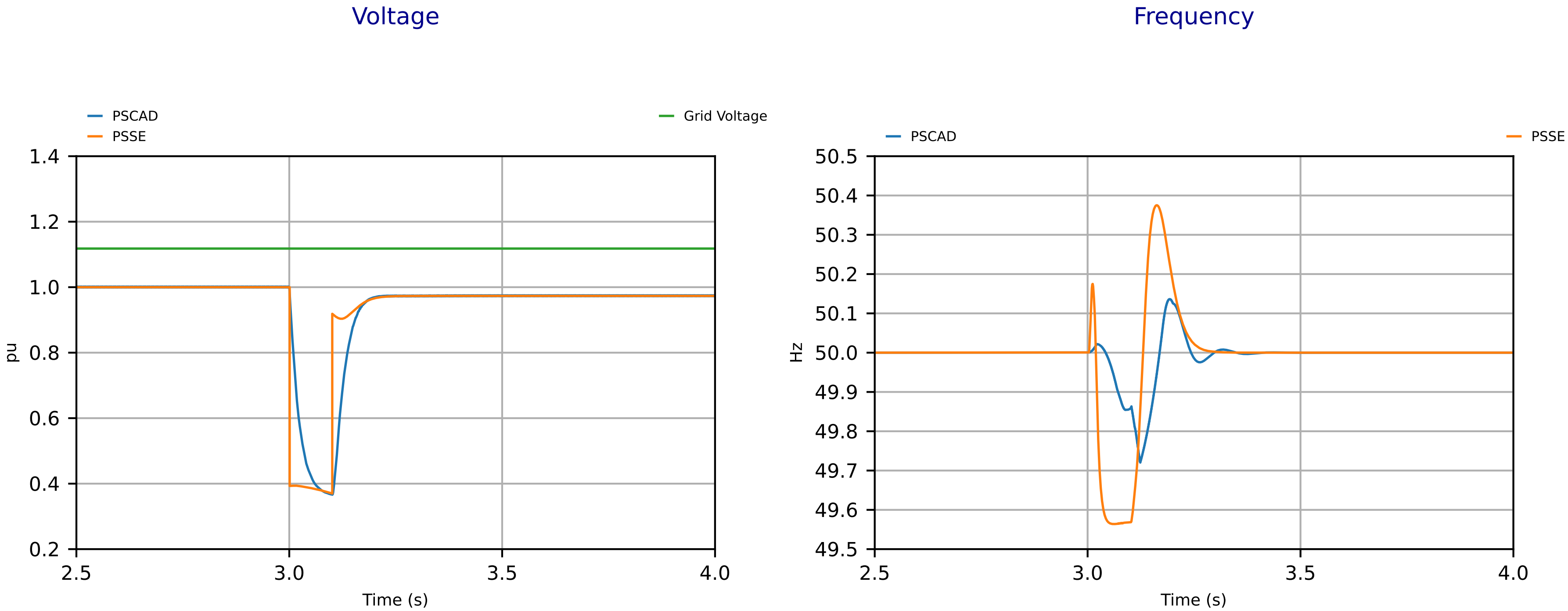
DER SMIB

SCR = 3, X/R = 14

Test #2:

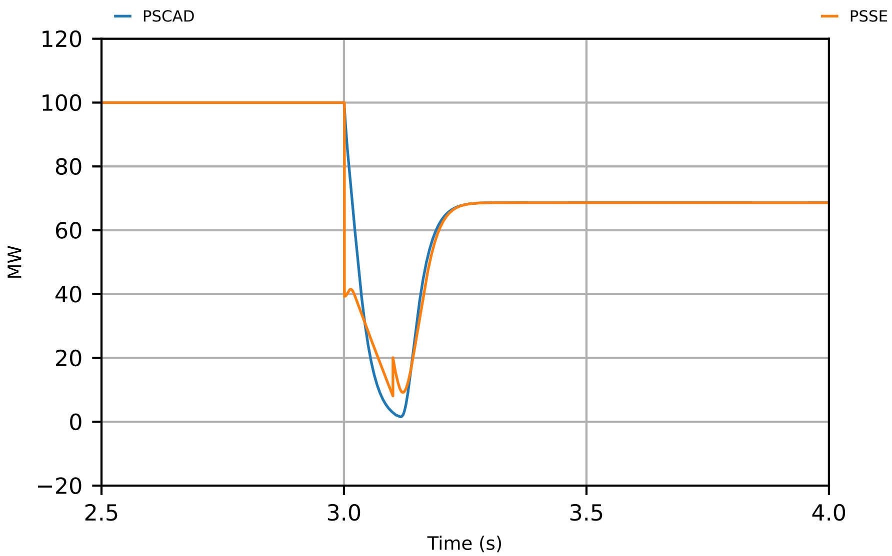
LLG fault for 100 ms

DER_SMIB_SCR_3_XR_14_T2_1

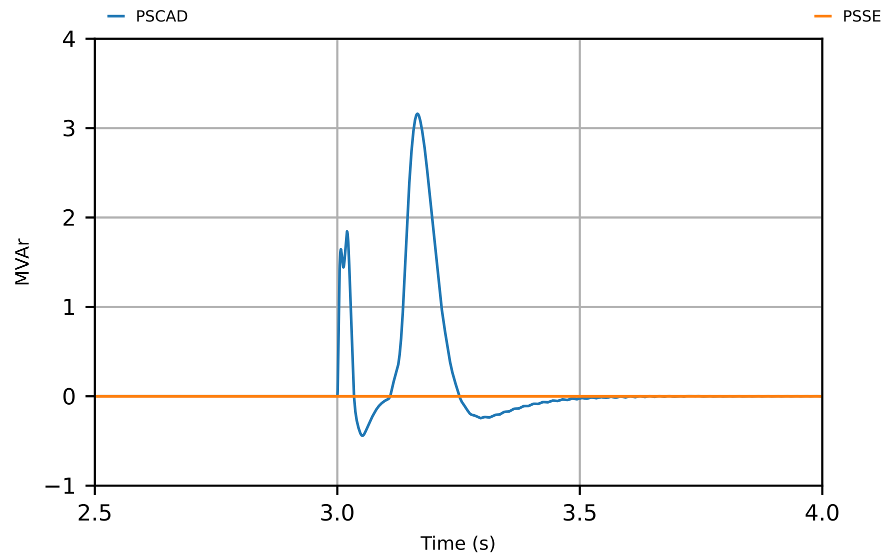


DER_SMIB_SCR_3_XR_14_T2_2

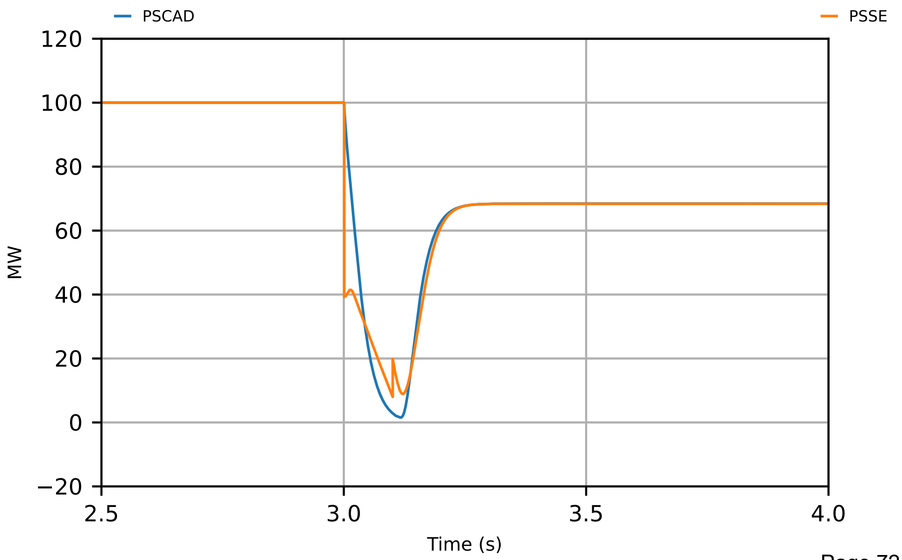
NSW DER Active Power



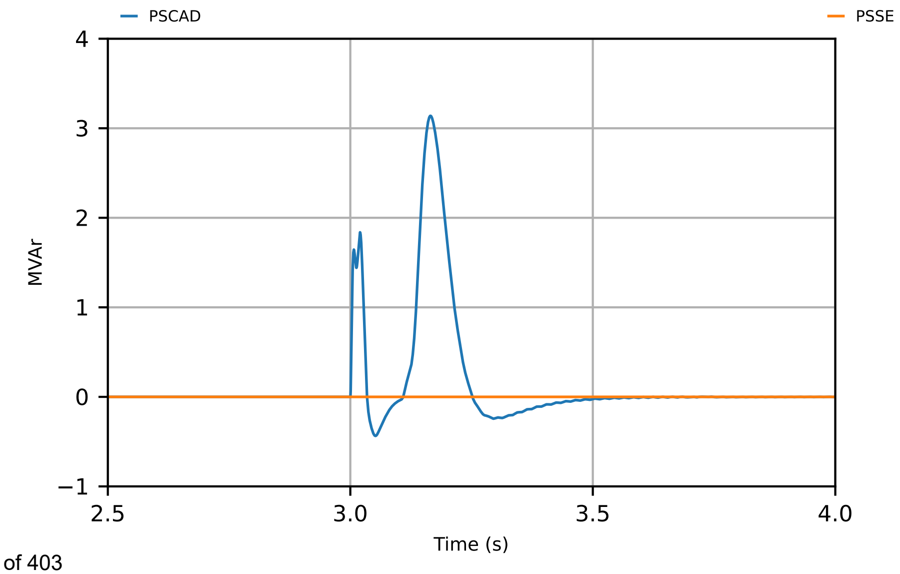
NSW DER Reactive Power



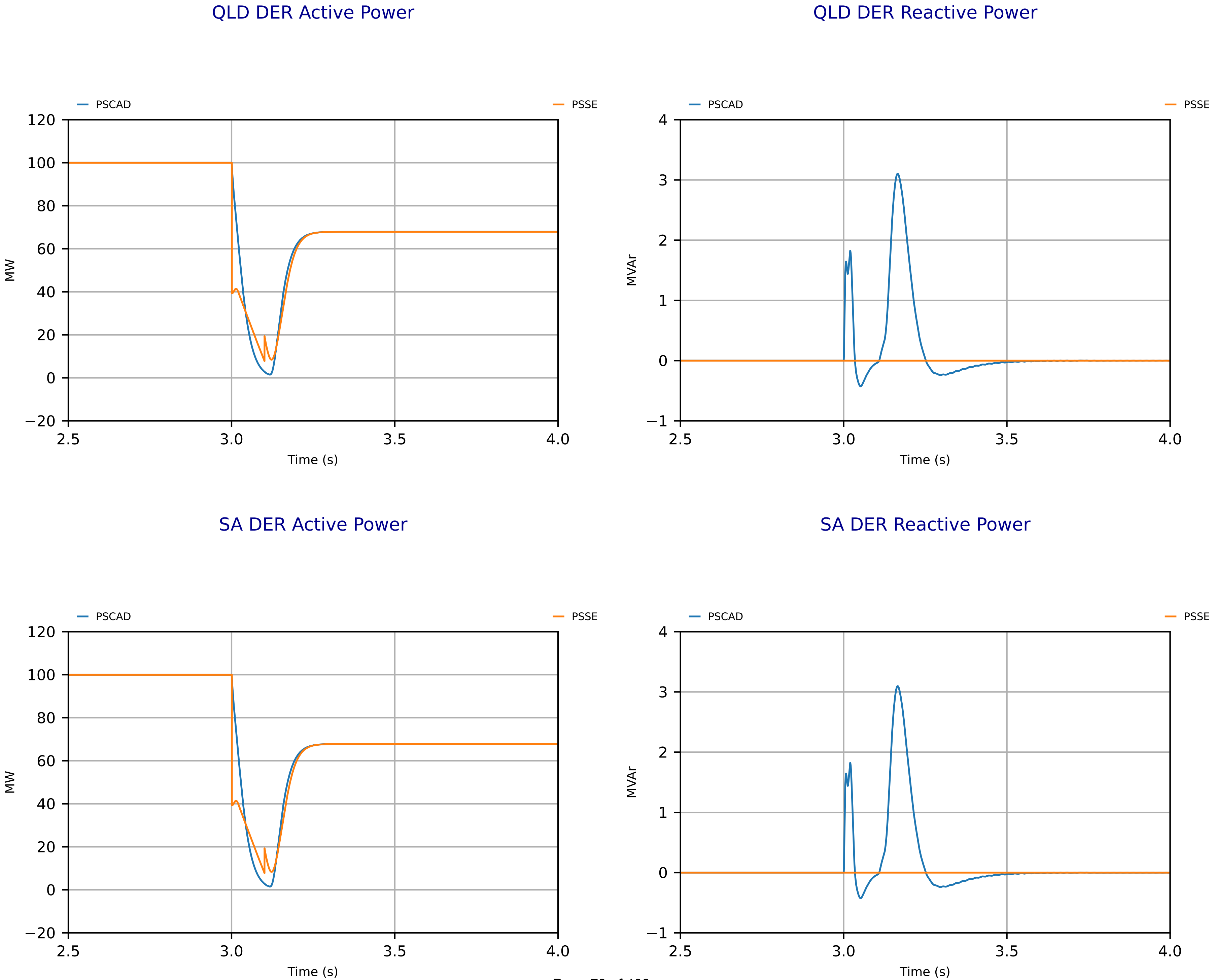
VIC DER Active Power



VIC DER Reactive Power



DER_SMIB_SCR_3_XR_14_T2_3

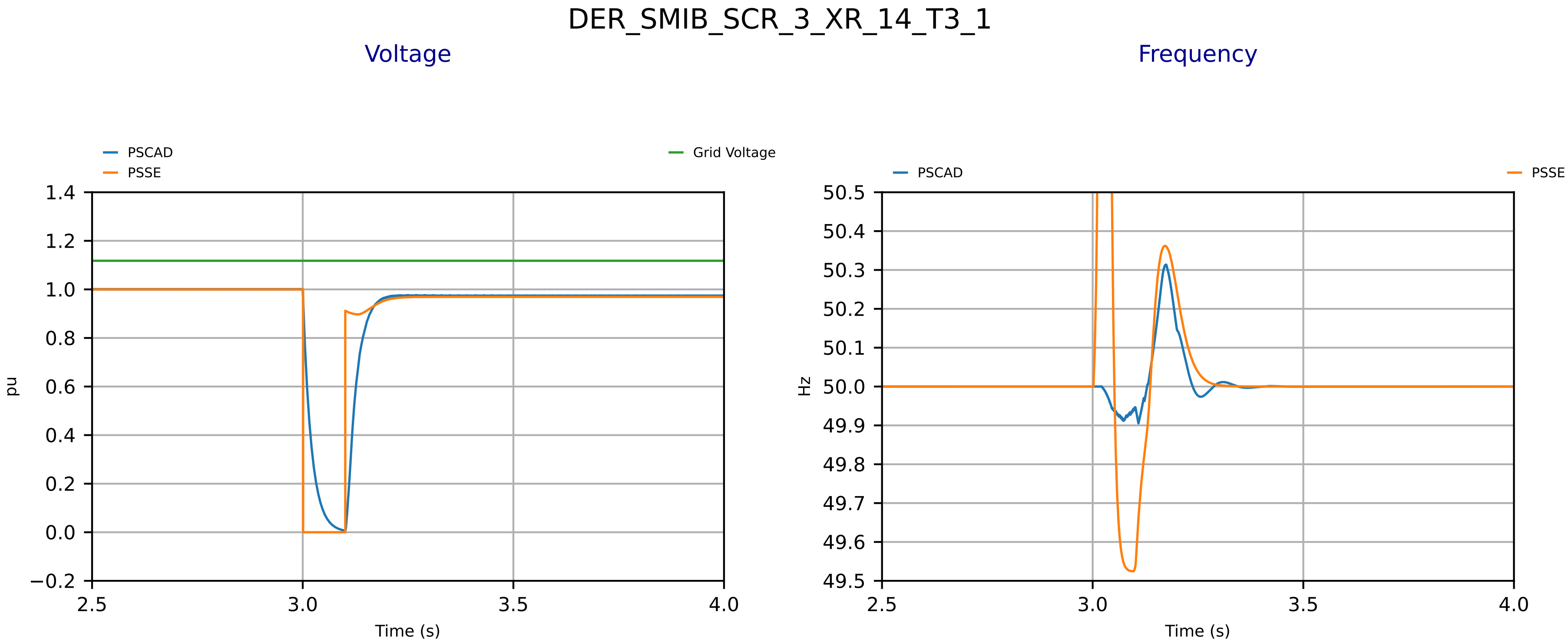


DER SMIB

SCR = 3, X/R = 14

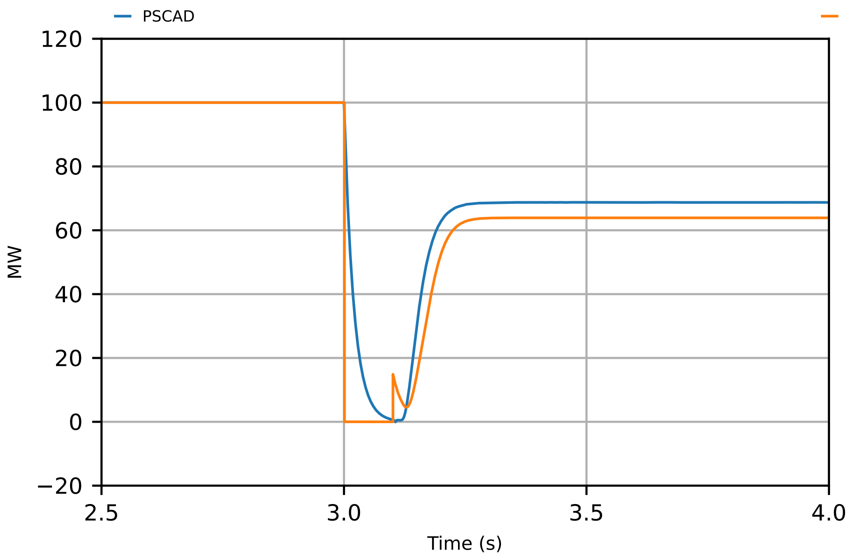
Test #3:

3PH-G fault for 100 ms

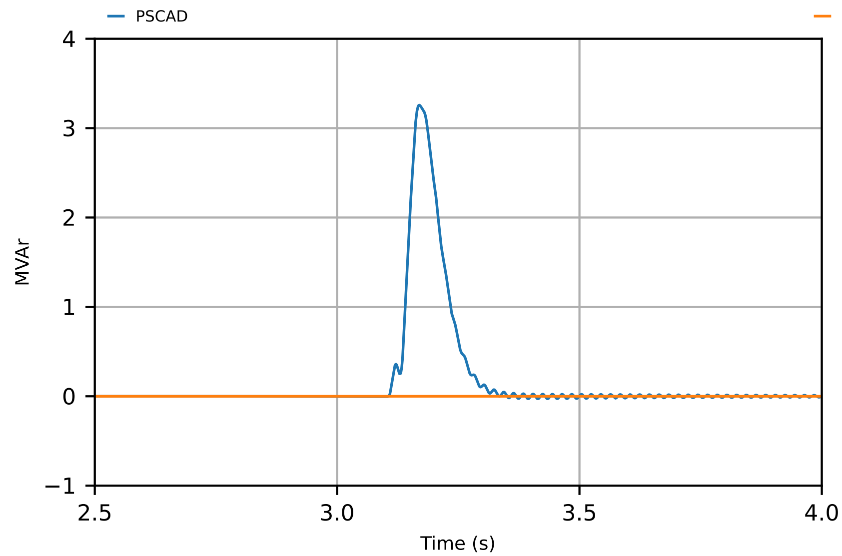

DER_SMIB_SCR_3_XR_14_T3_1
Voltage
Frequency
PSCAD
PSSE
Grid Voltage
pu
Hz
Time (s)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
−0.2
50.5
50.4
50.3
50.2
50.1
50.0
49.9
49.8
49.7
49.6
49.5
2.5
3.0
3.5
4.0

DER_SMIB_SCR_3_XR_14_T3_2

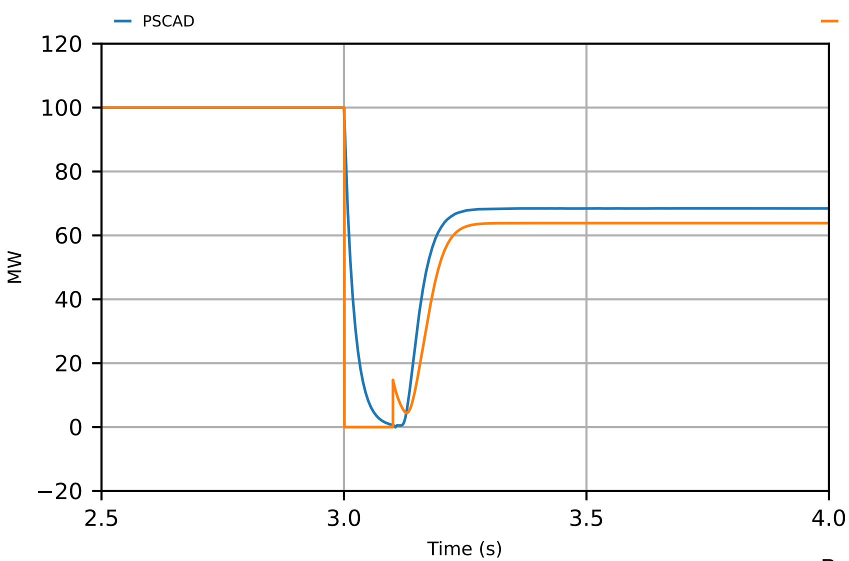
NSW DER Active Power



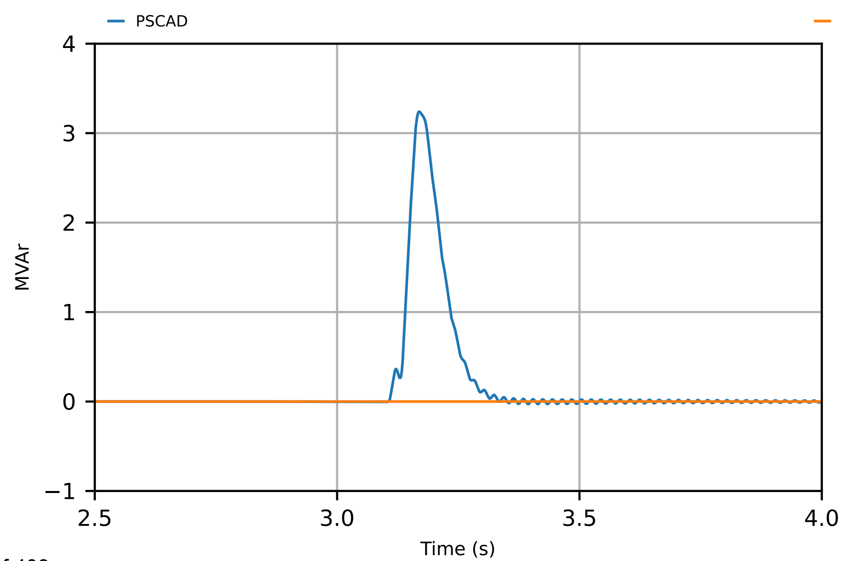
NSW DER Reactive Power



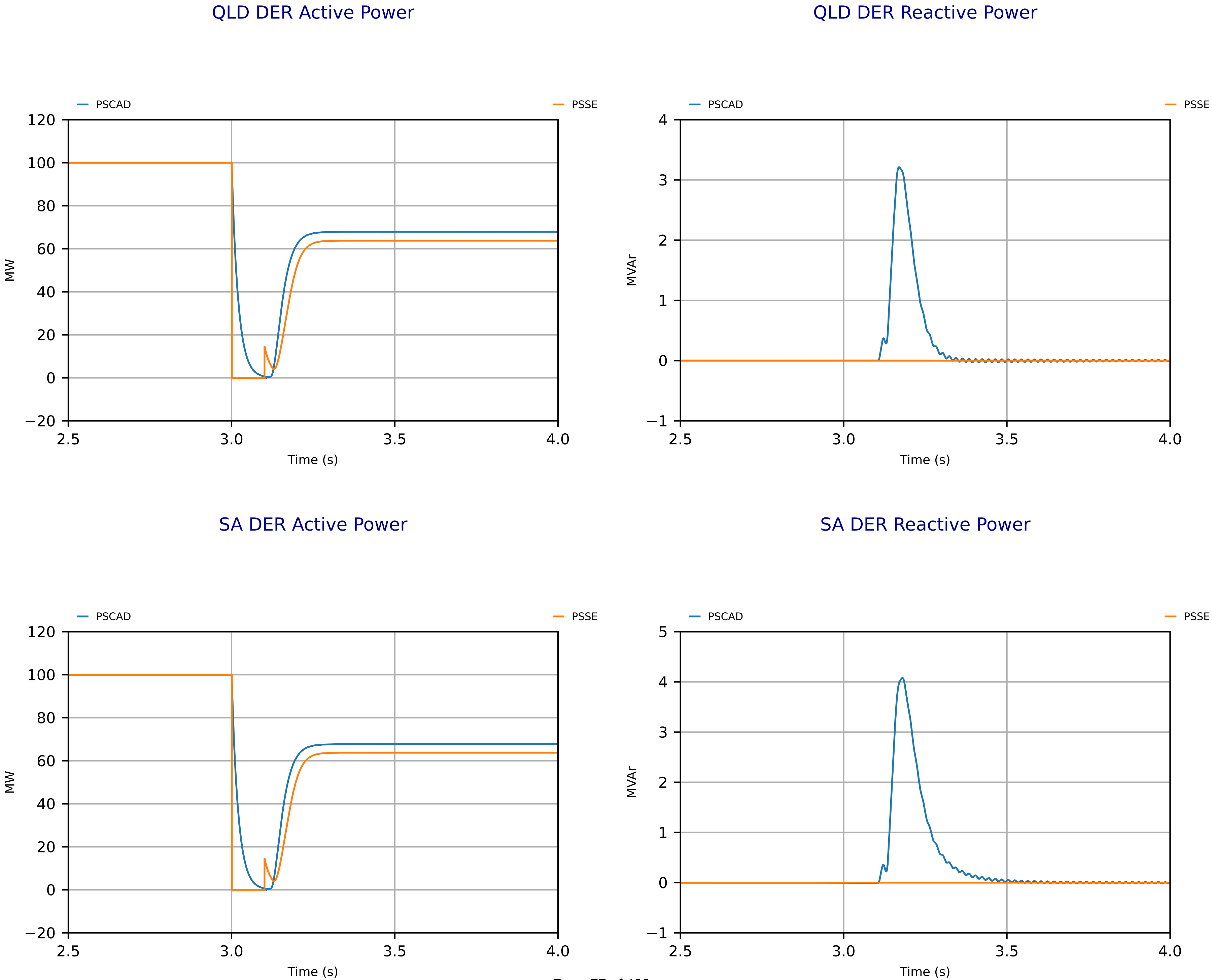
VIC DER Active Power



VIC DER Reactive Power



DER_SMIB_SCR_3_XR_14_T3_3



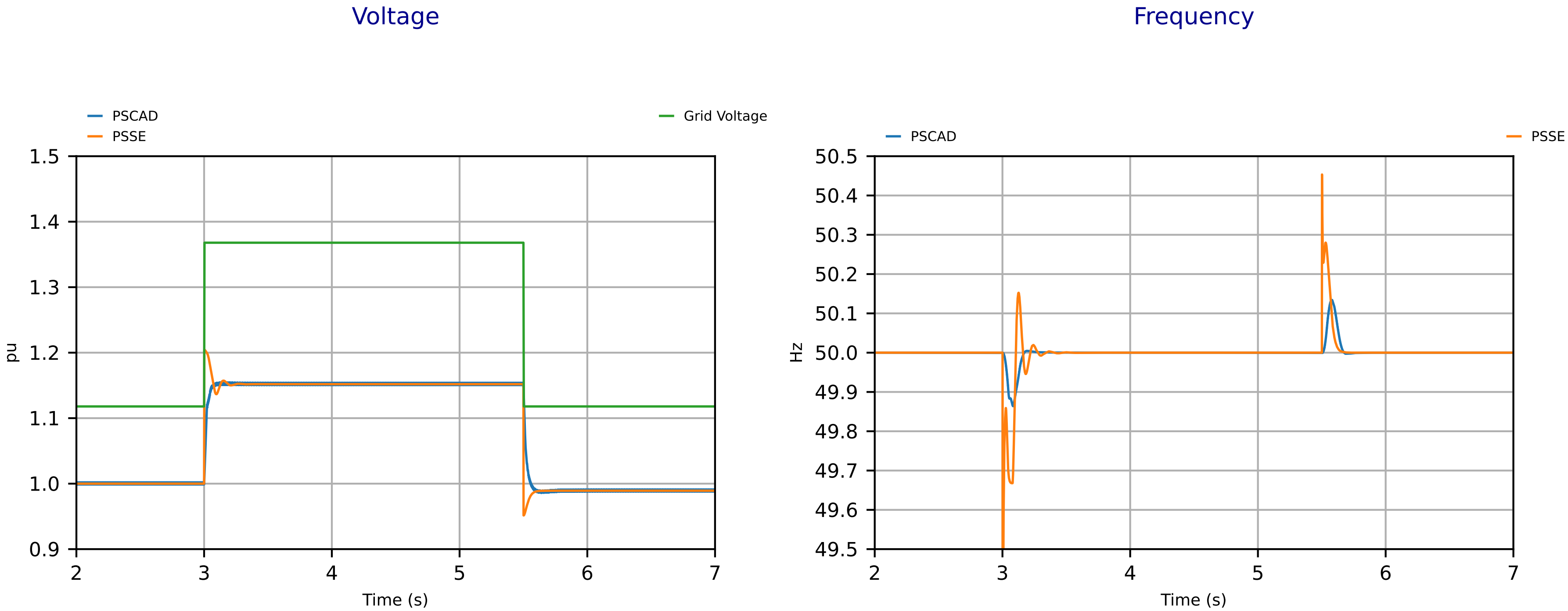
DER SMIB

SCR = 3, X/R = 14

Test #4:

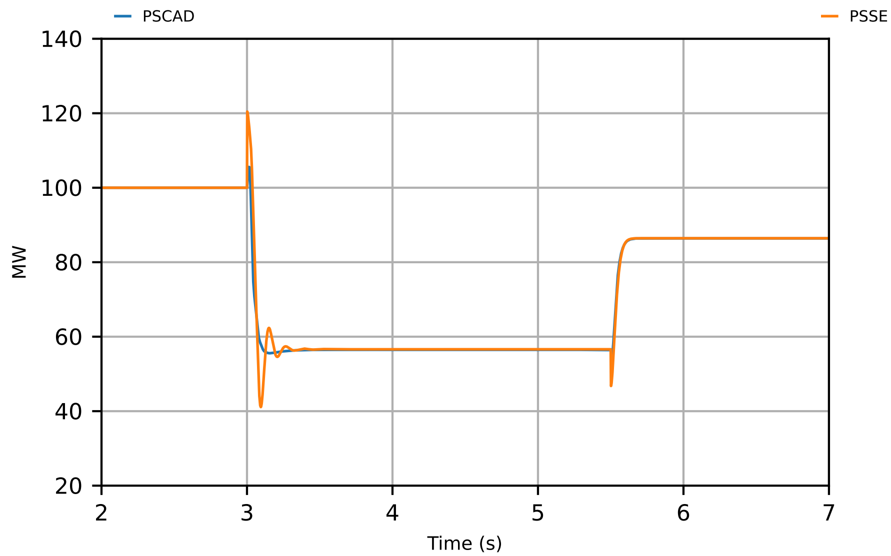
~115% Voltage disturbance for 2.5 s

DER_SMIB_SCR_3_XR_14_T4_1

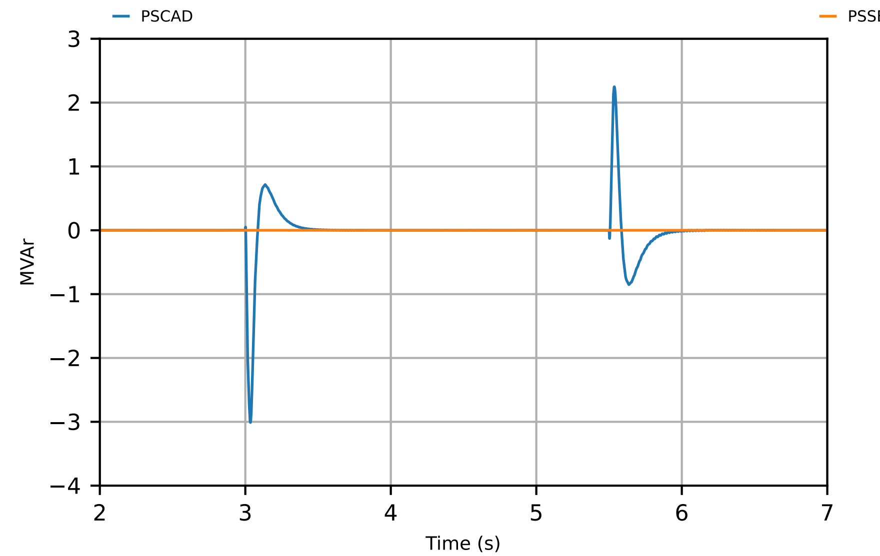


DER_SMIB_SCR_3_XR_14_T4_2

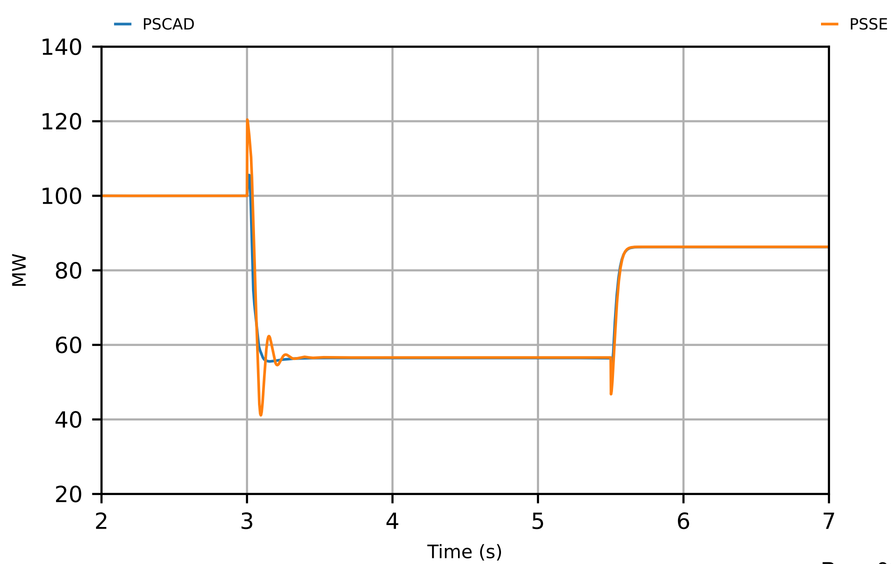
NSW DER Active Power



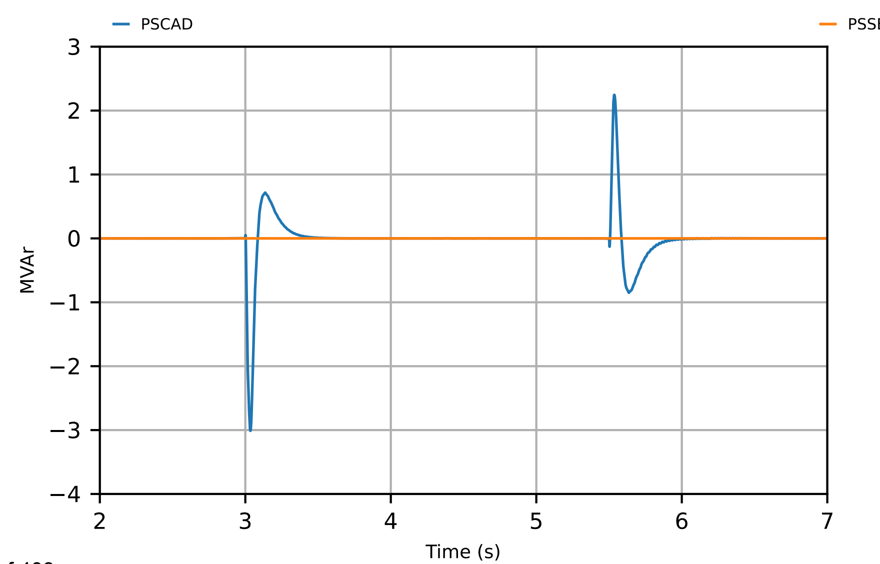
NSW DER Reactive Power



VIC DER Active Power

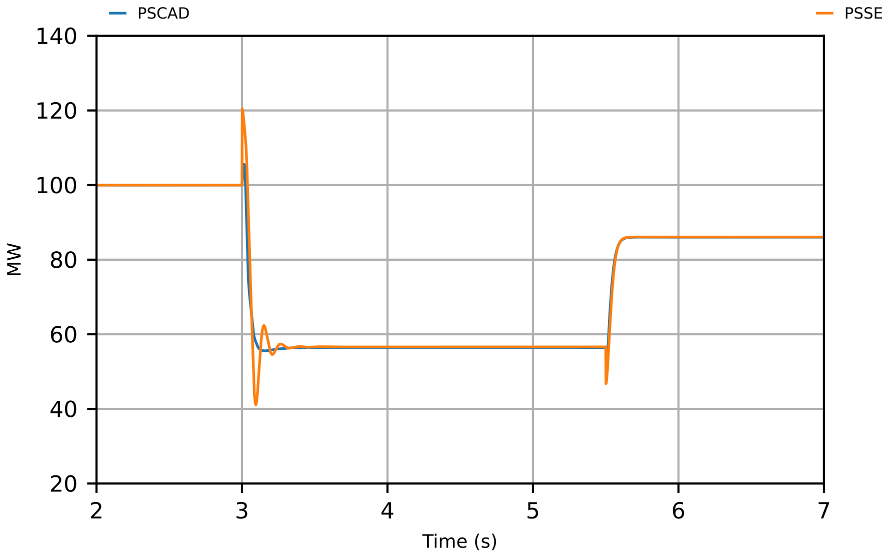


VIC DER Reactive Power

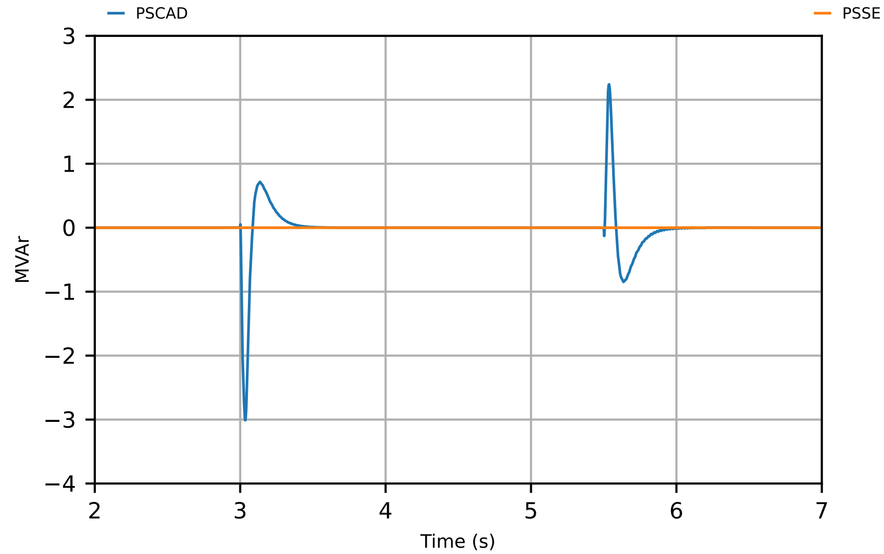


DER_SMIB_SCR_3_XR_14_T4_3

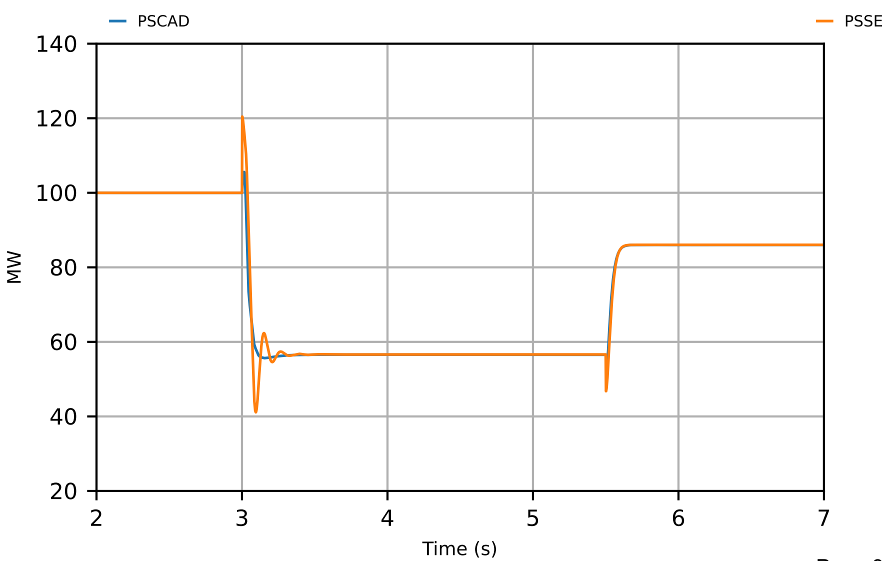
QLD DER Active Power



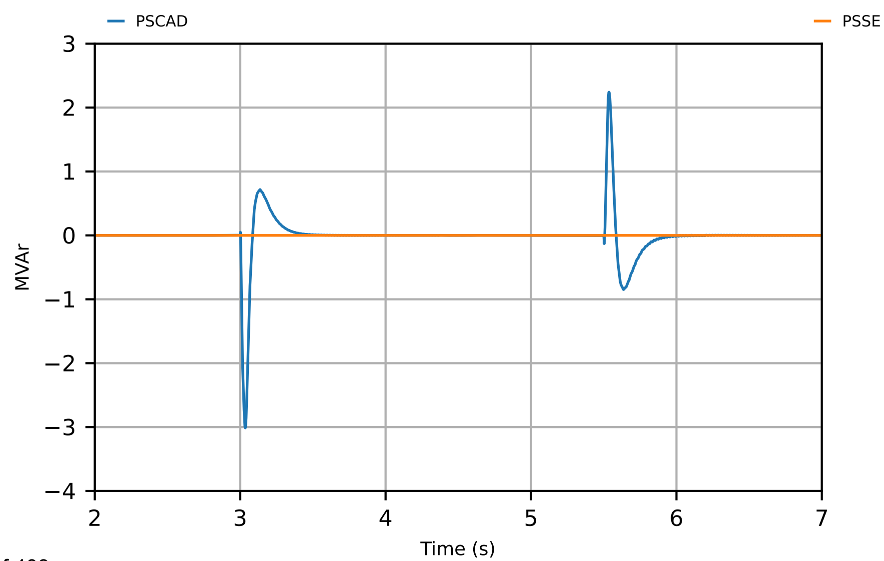
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



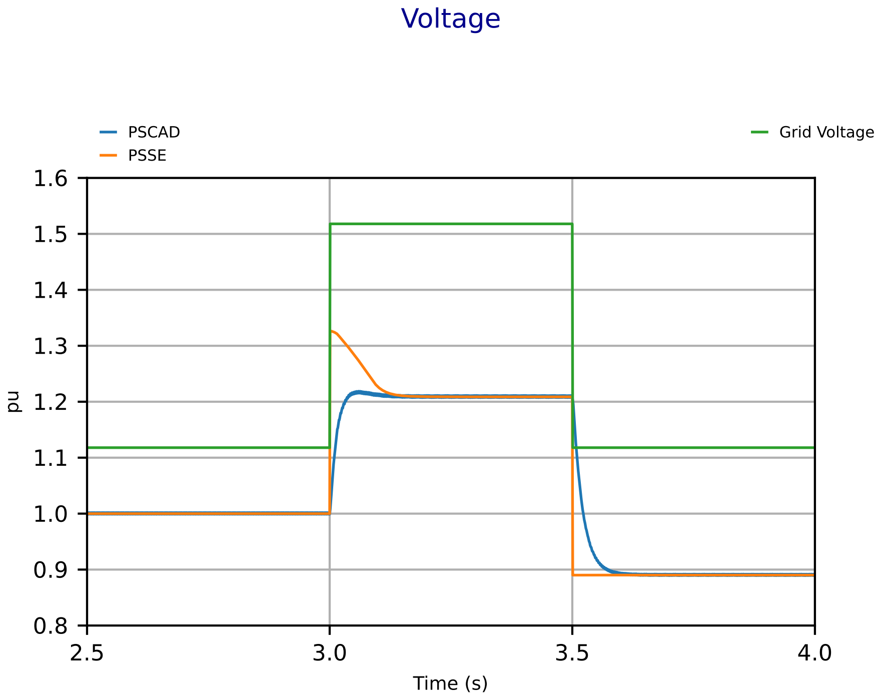
DER SMIB

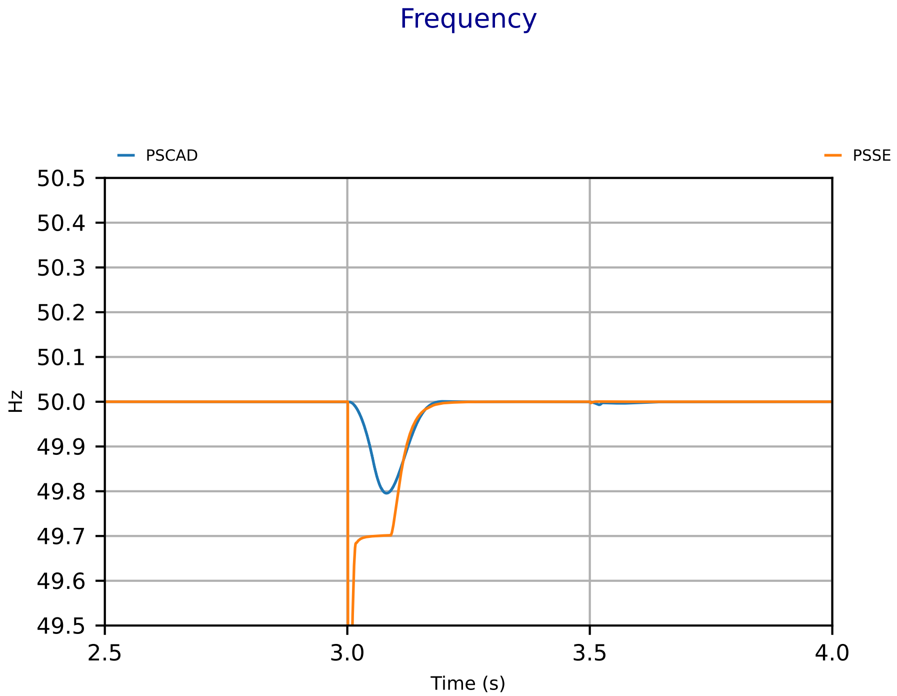
SCR = 3, X/R = 14

Test #5:

~120% Voltage disturbance for 500 ms

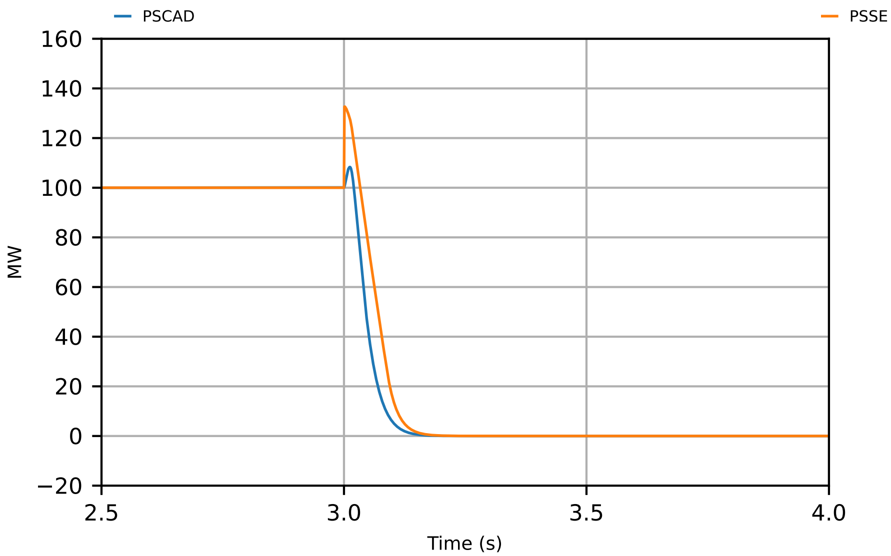
DER_SMIB_SCR_3_XR_14_T5_1



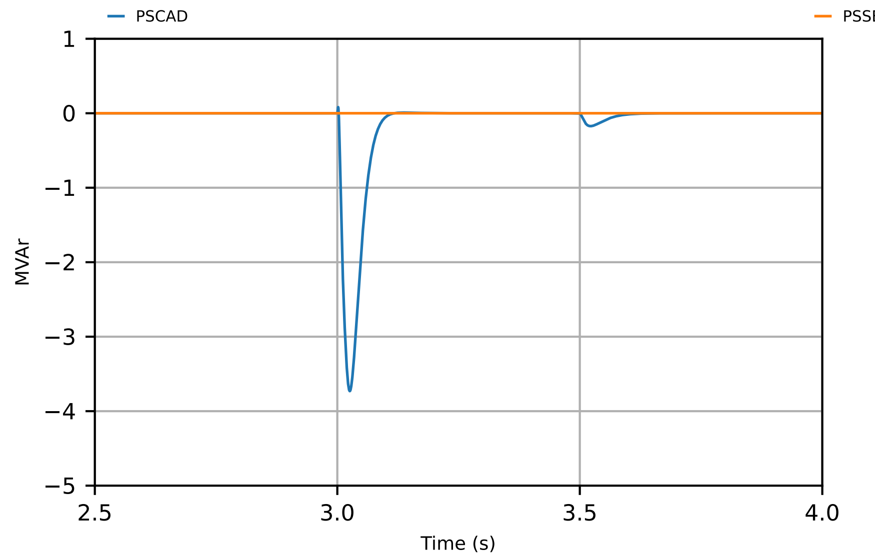


DER_SMIB_SCR_3_XR_14_T5_2

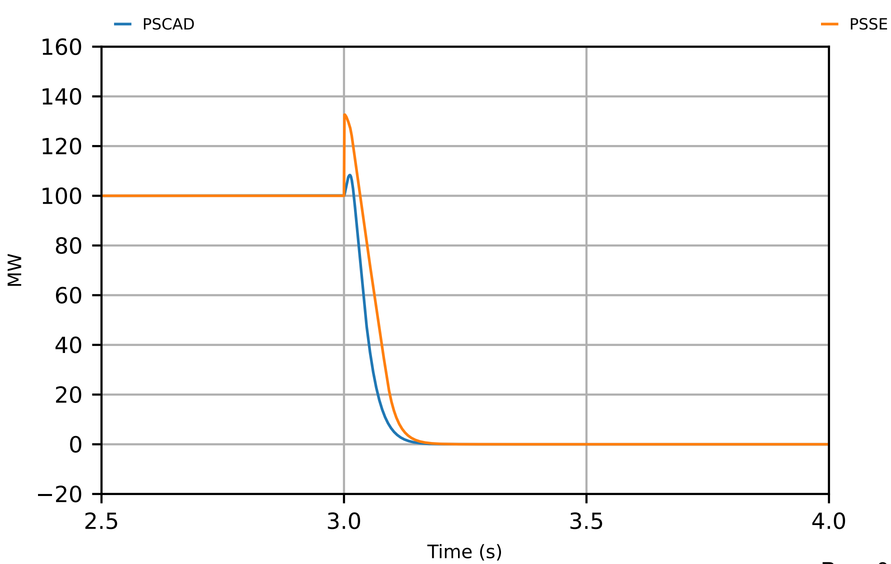
NSW DER Active Power



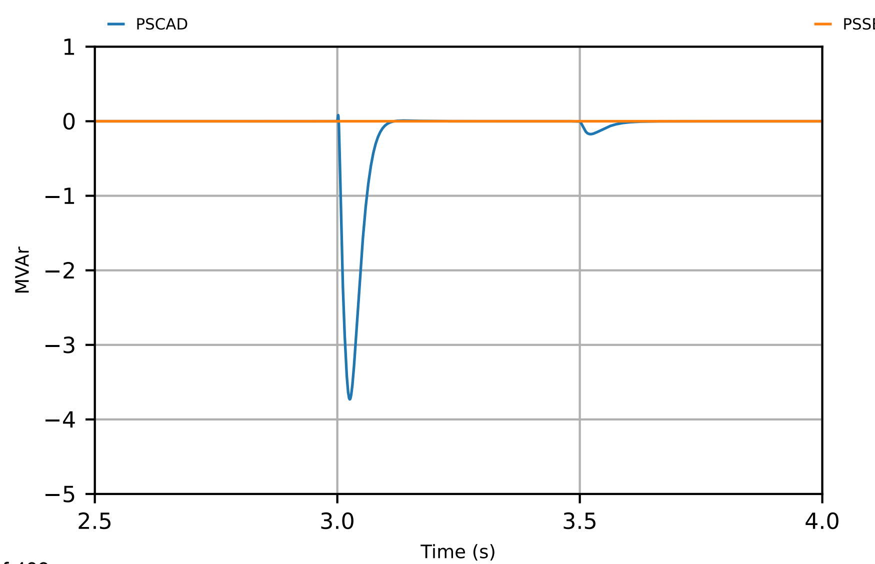
NSW DER Reactive Power



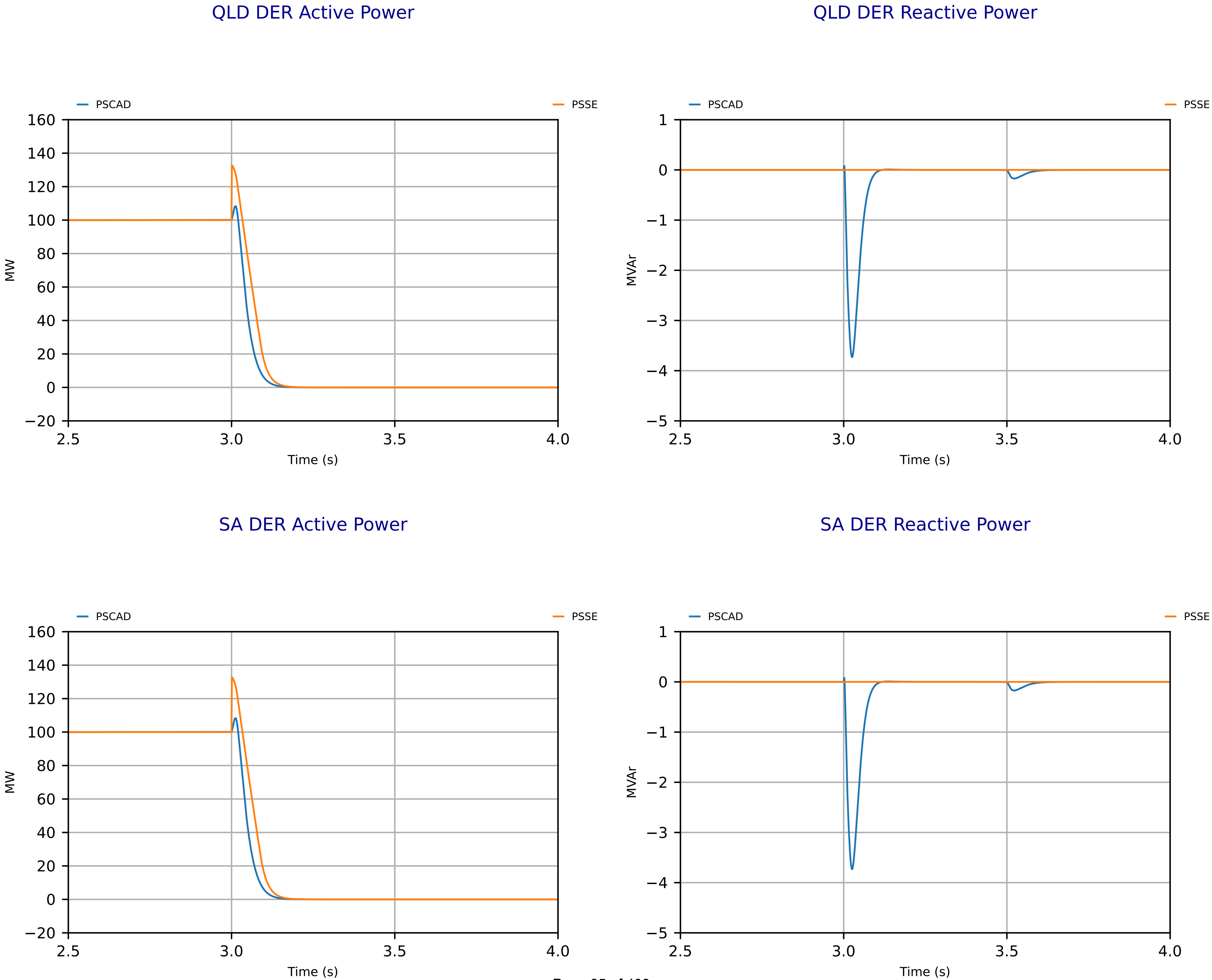
VIC DER Active Power



VIC DER Reactive Power



DER_SMIB_SCR_3_XR_14_T5_3



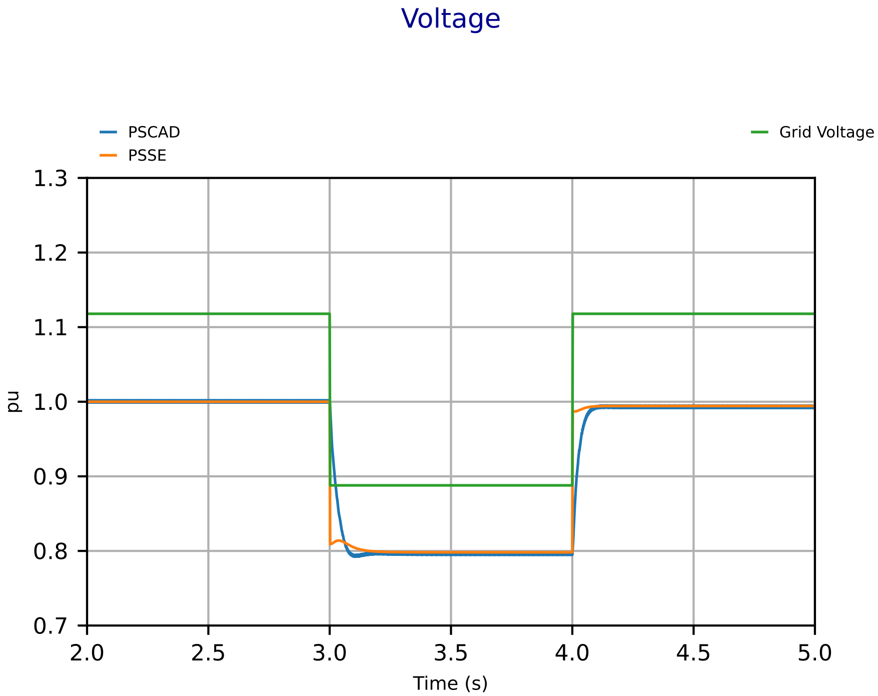
DER SMIB

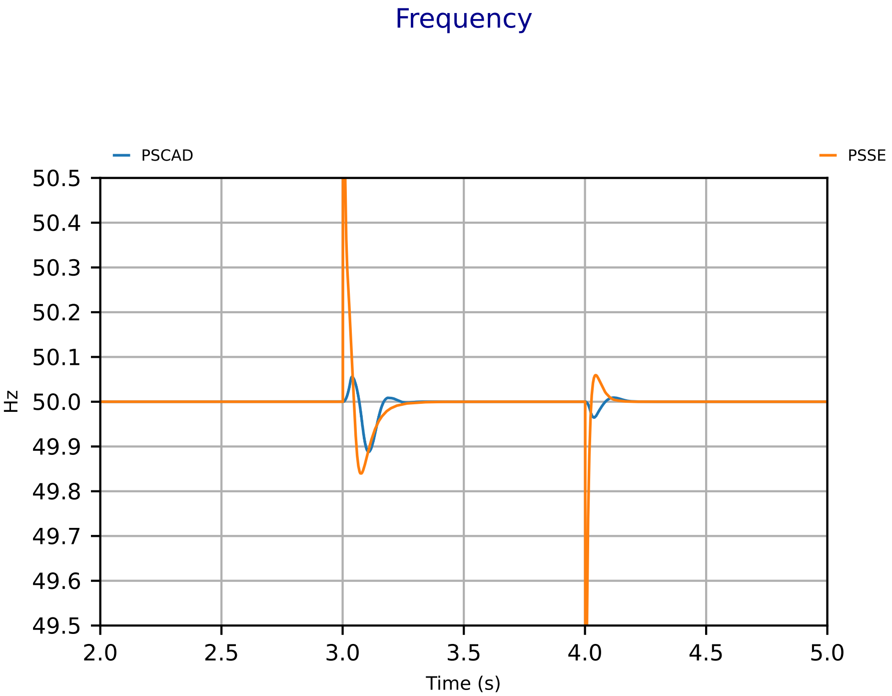
SCR = 3, X/R = 14

Test #6:

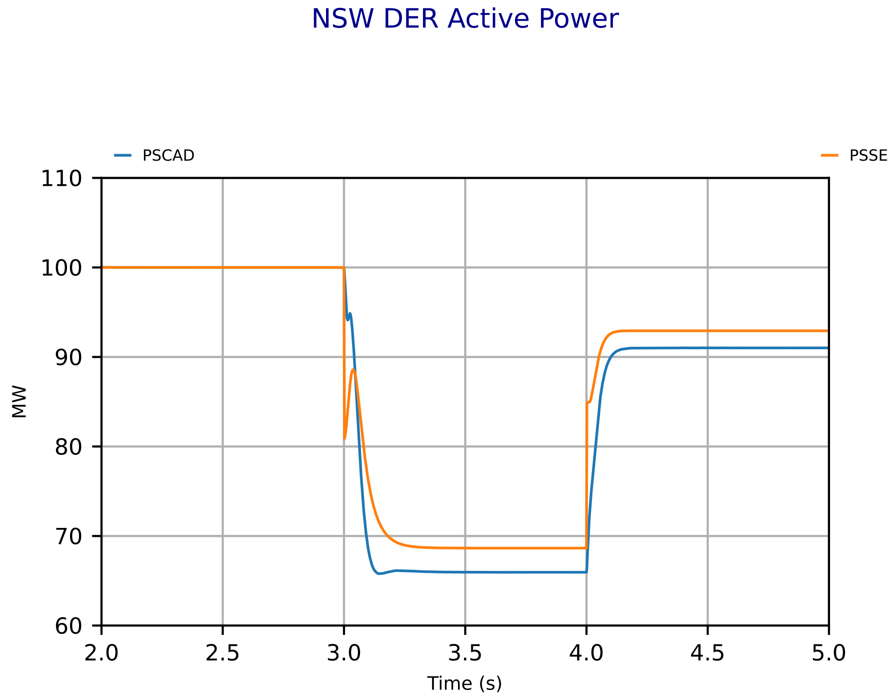
~80% Voltage disturbance for 1 sec

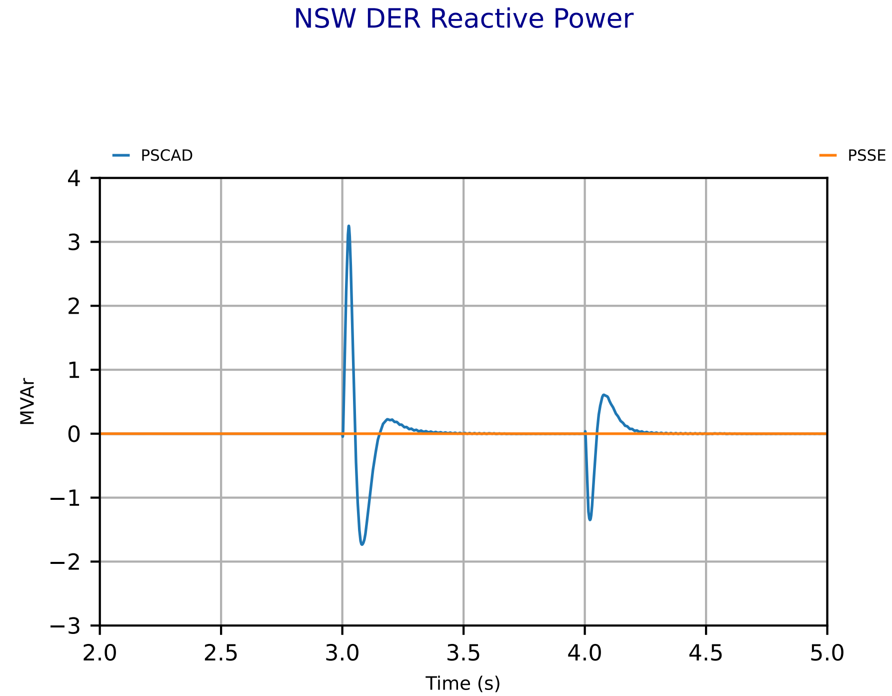
DER_SMIB_SCR_3_XR_14_T6_1

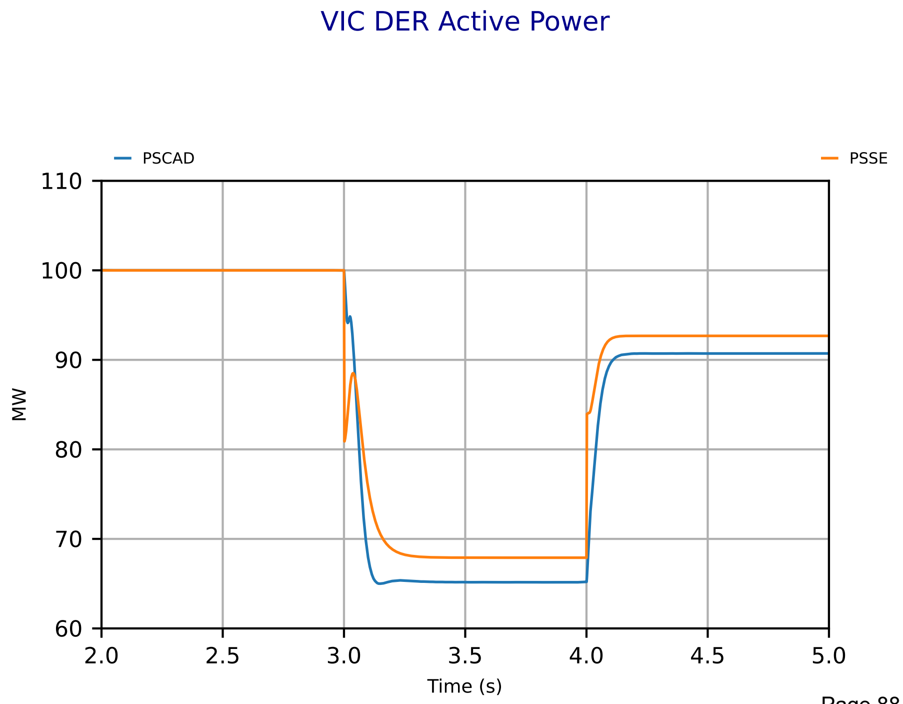


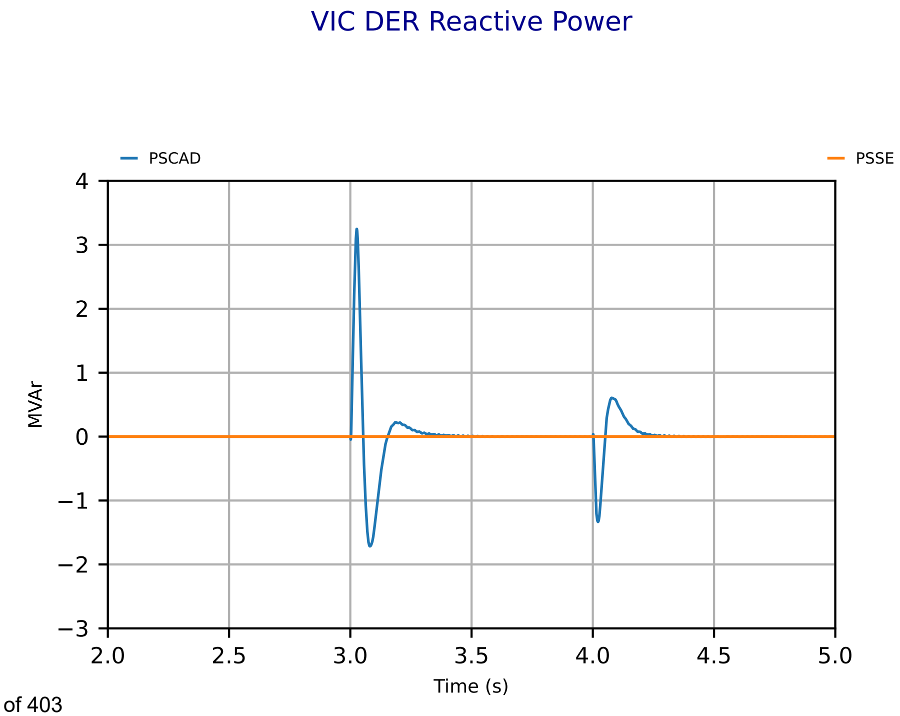


DER_SMIB_SCR_3_XR_14_T6_2

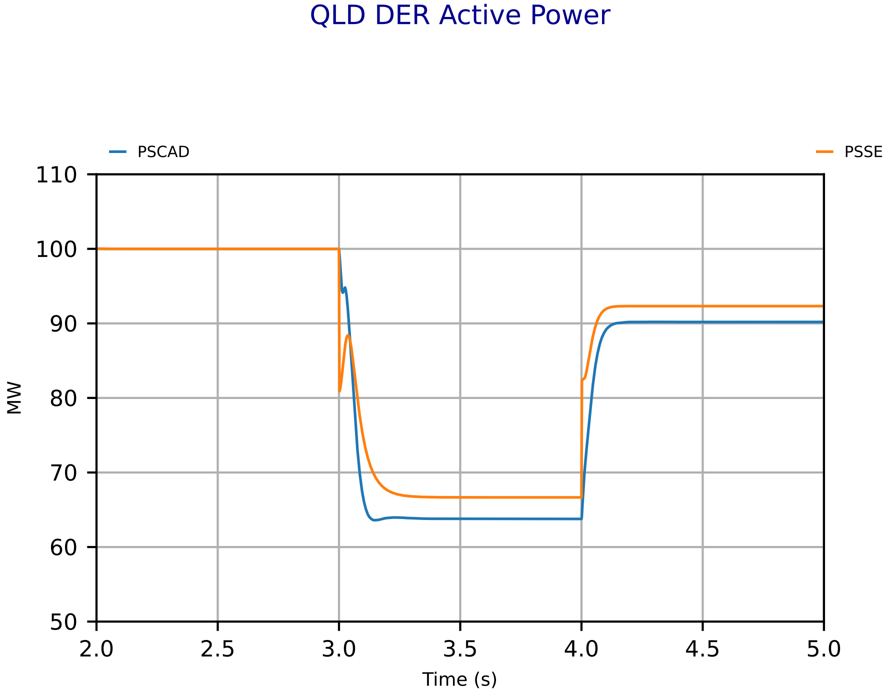


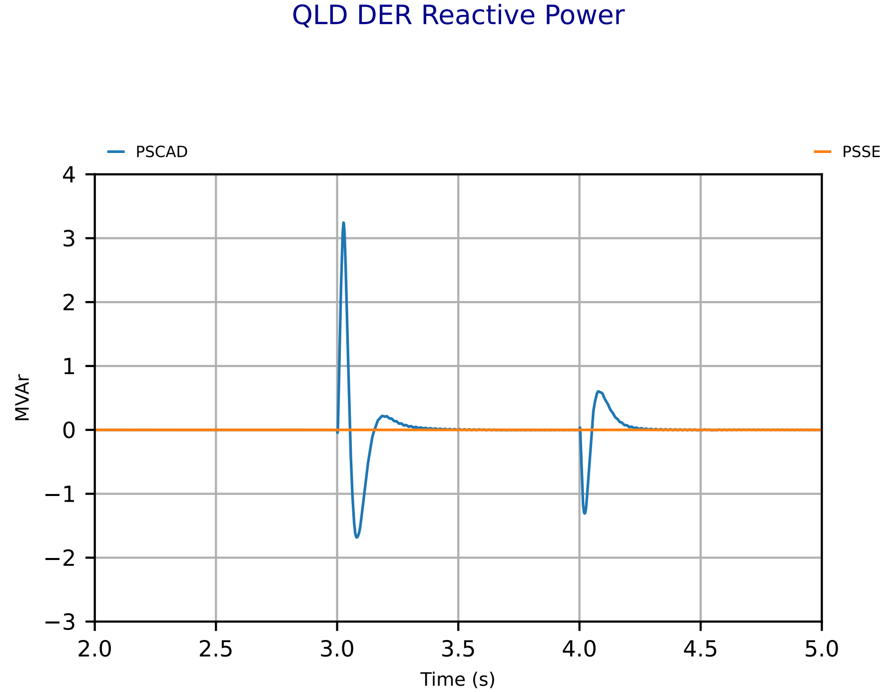


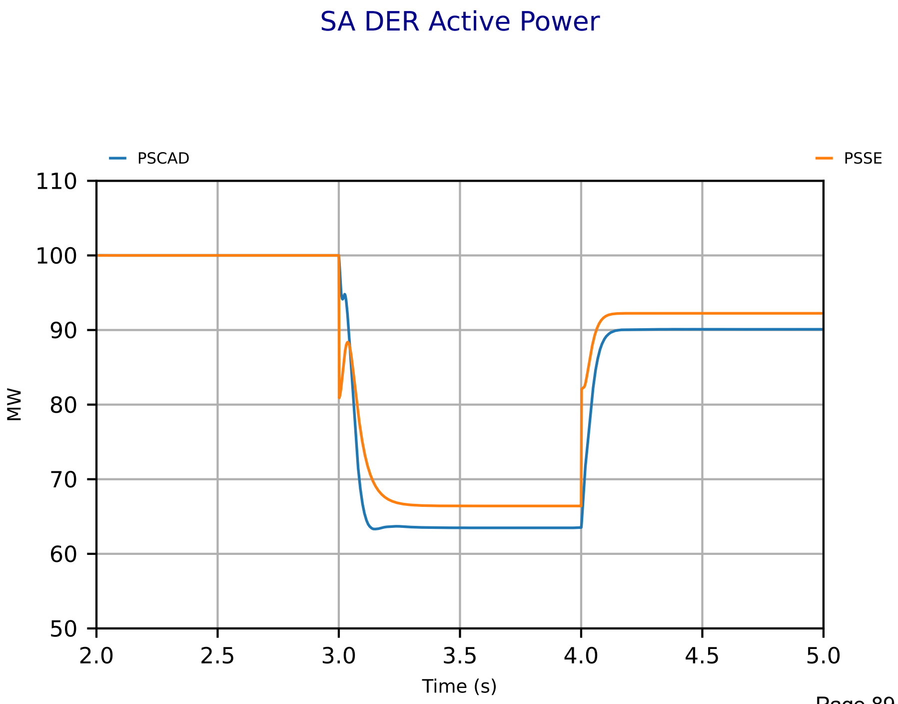


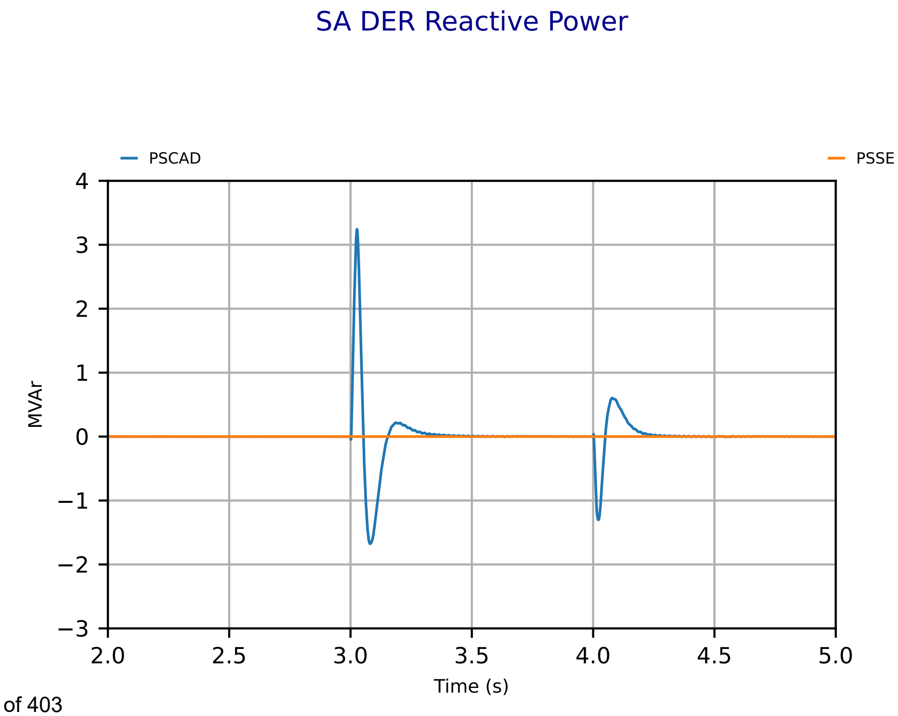


DER_SMIB_SCR_3_XR_14_T6_3









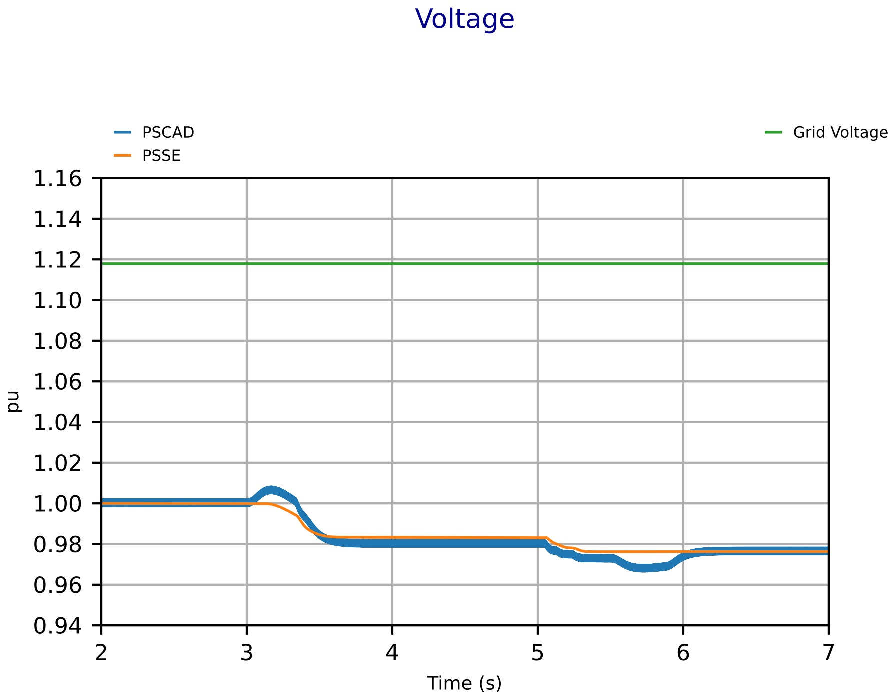
DER SMIB

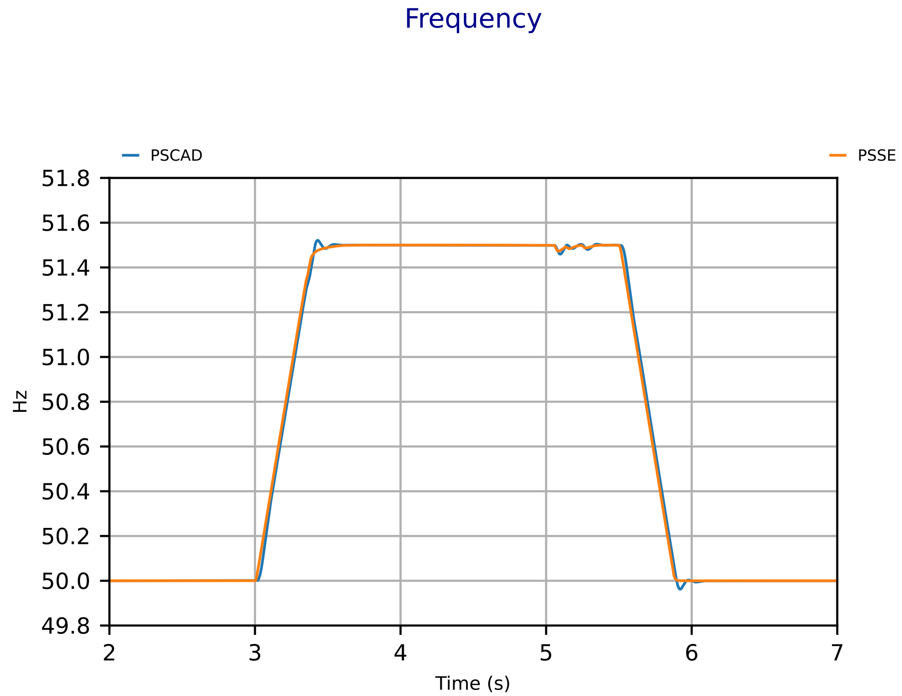
SCR = 3, X/R = 14

Test #7:

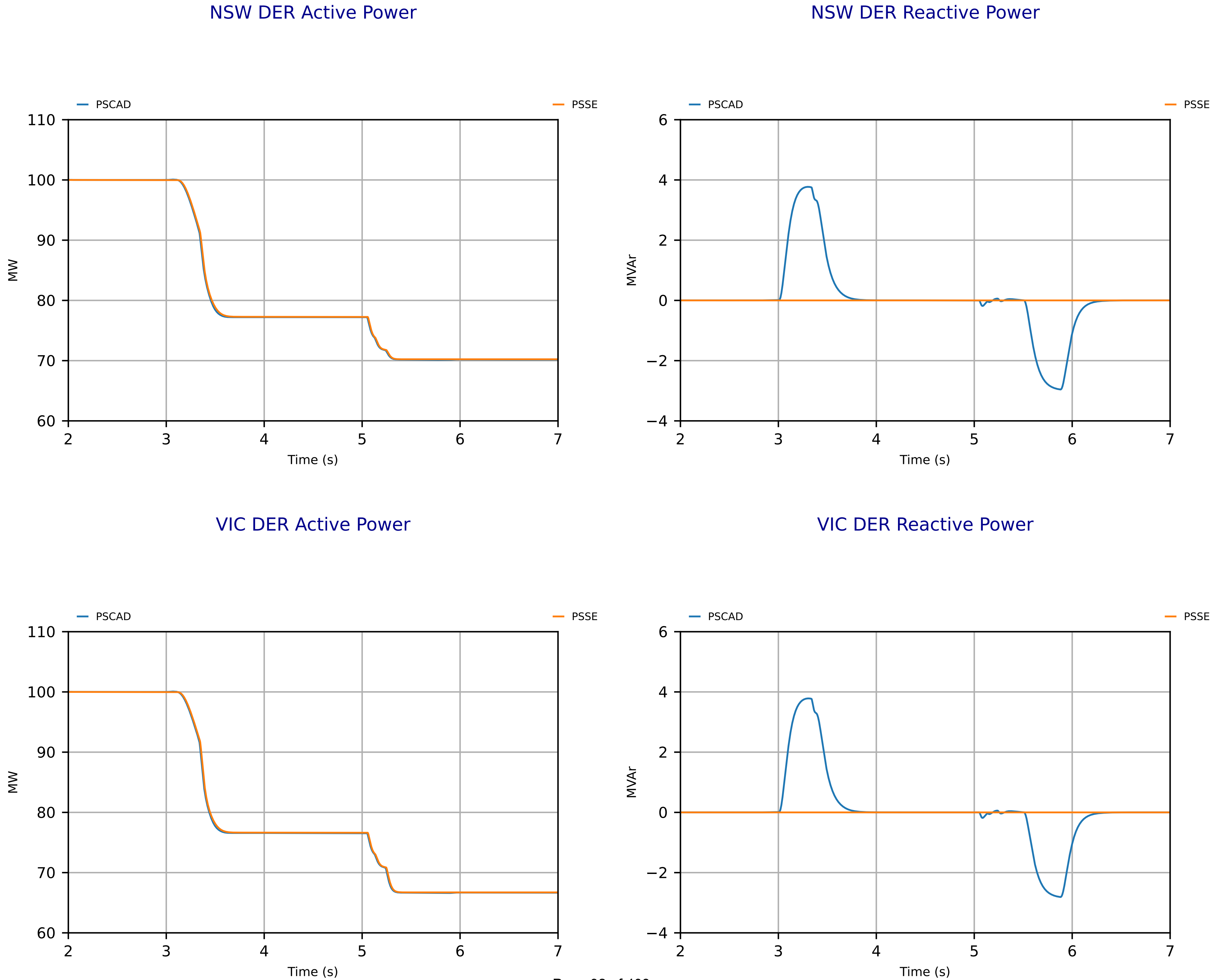
51.5 Hz frequency step for 2.5 sec (4 Hz/s)

DER_SMIB_SCR_3_XR_14_T7_1

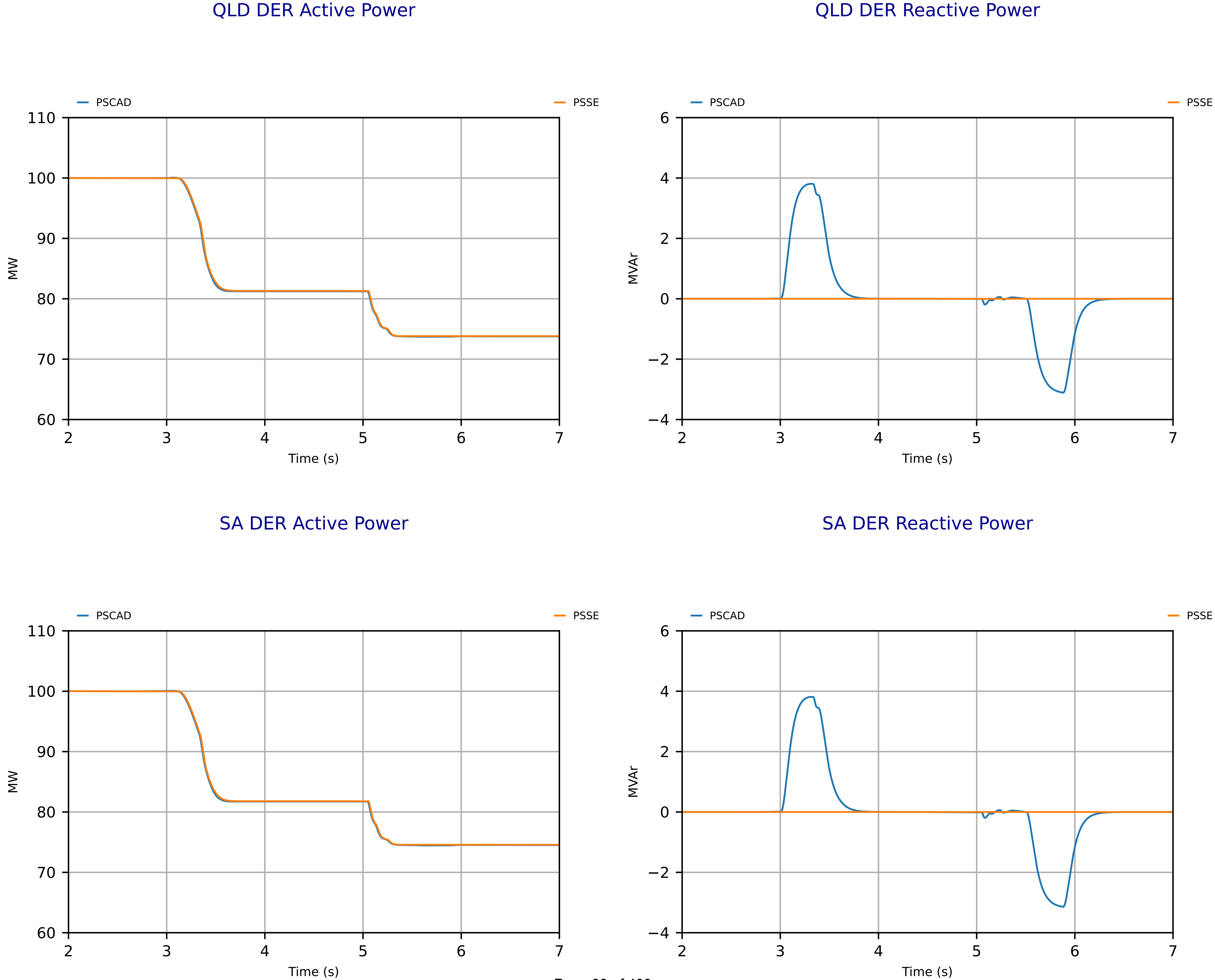




DER_SMIB_SCR_3_XR_14_T7_2



DER_SMIB_SCR_3_XR_14_T7_3



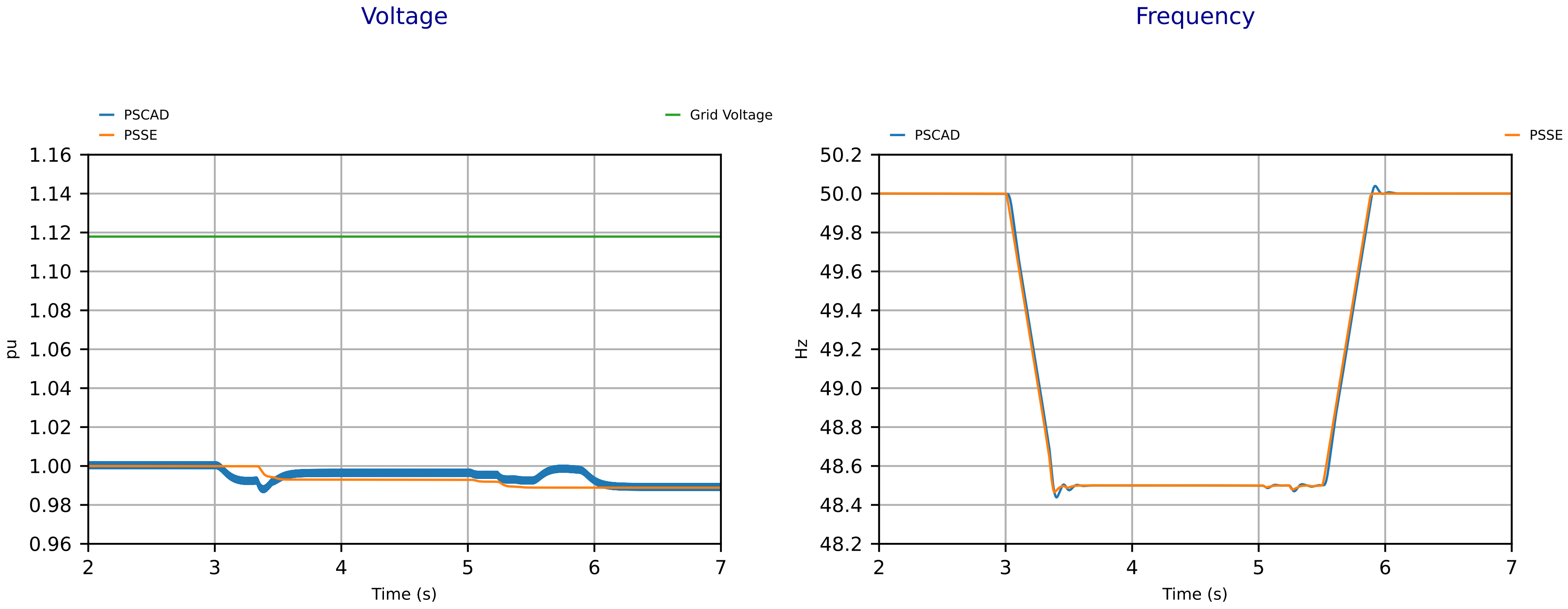
DER SMIB

SCR = 3, X/R = 14

Test #8:

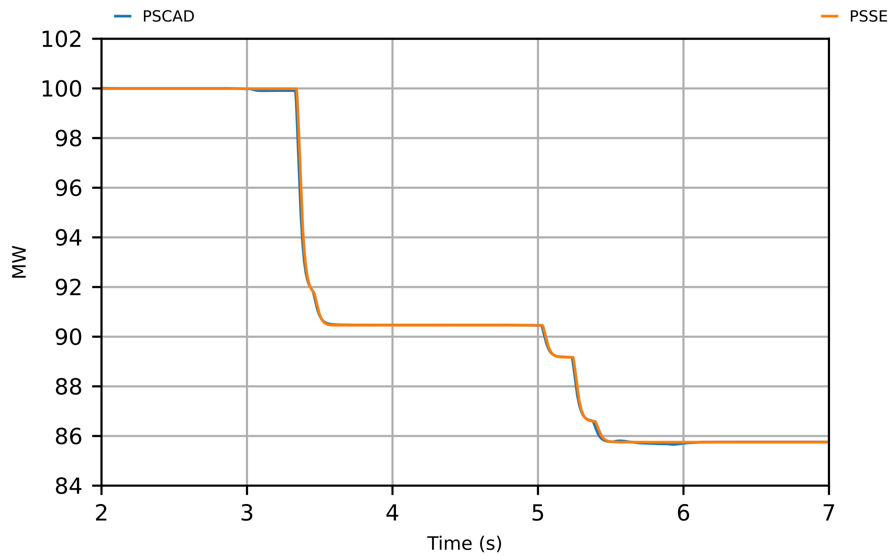
48.5 Hz frequency step for 2.5 sec (4 Hz/s)

DER_SMIB_SCR_3_XR_14_T8_1

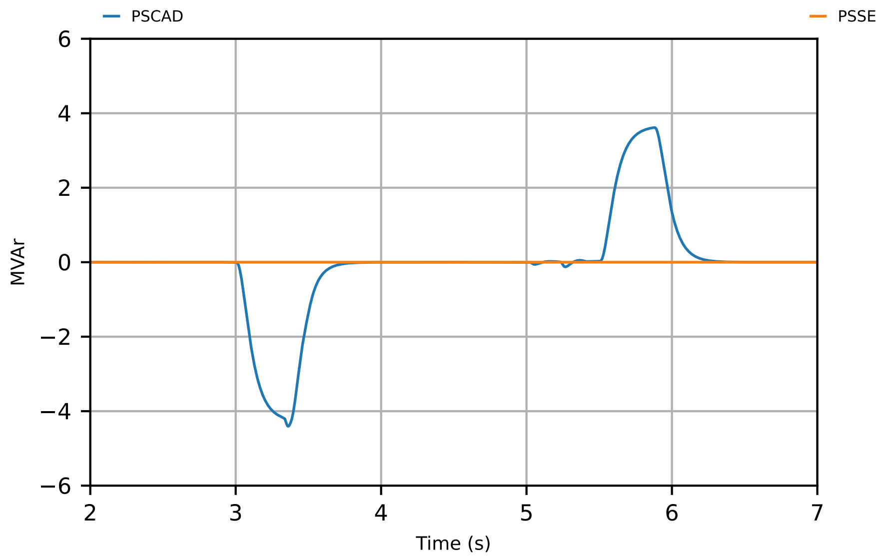


DER_SMIB_SCR_3_XR_14_T8_2

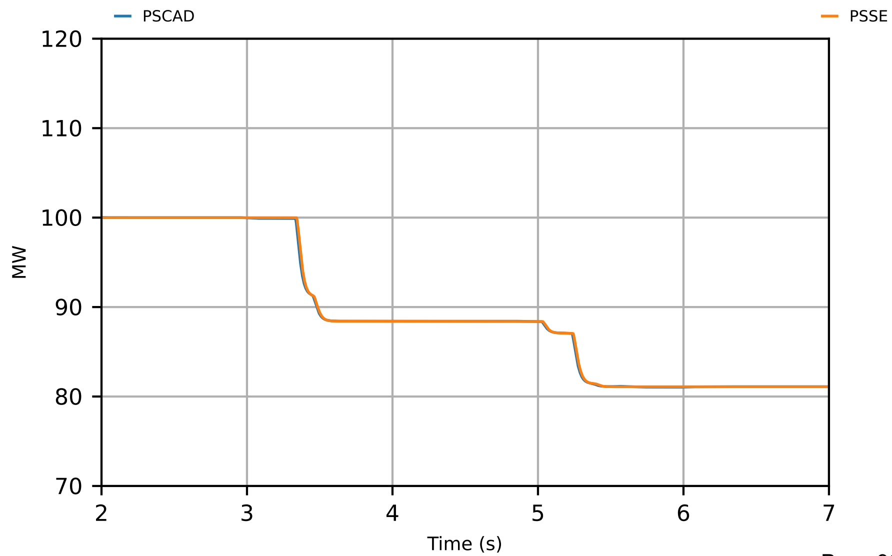
NSW DER Active Power



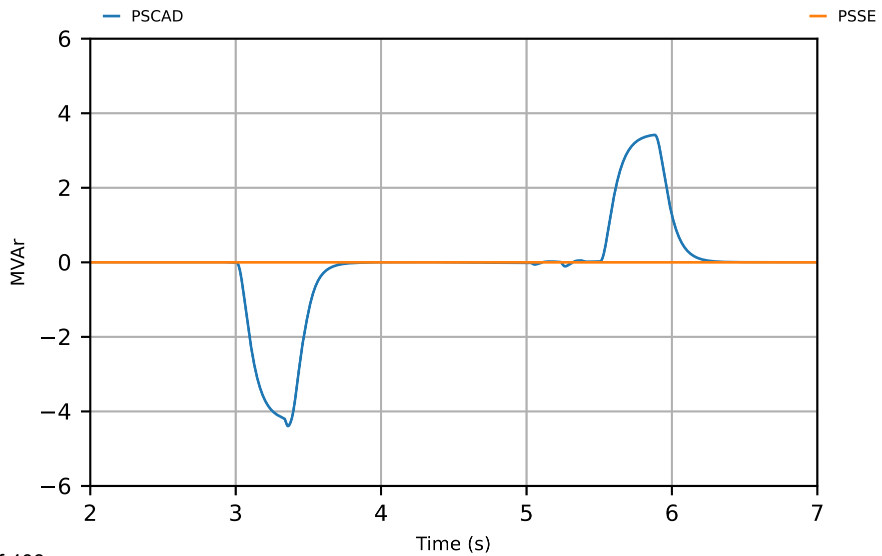
NSW DER Reactive Power



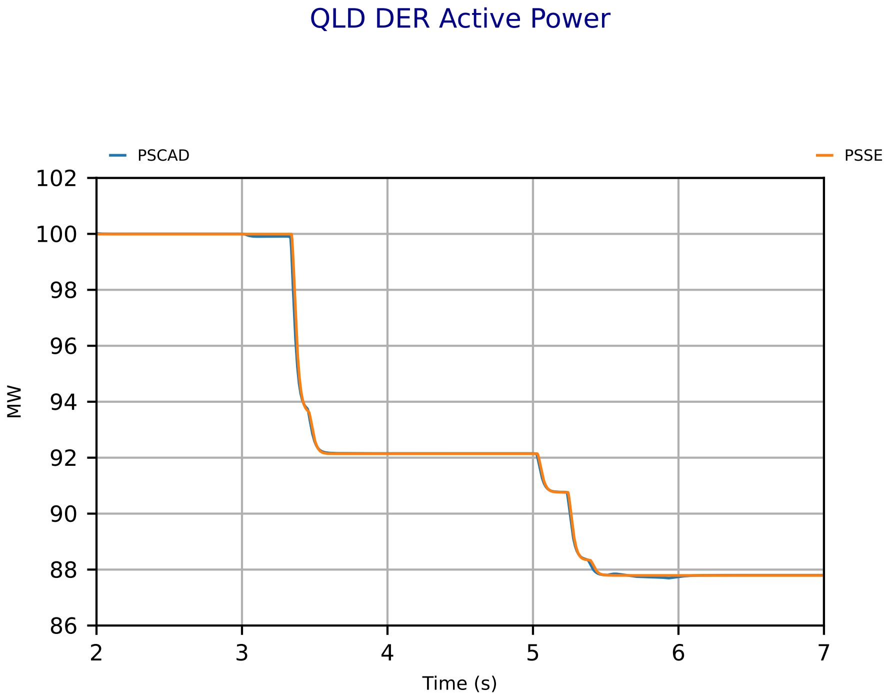
VIC DER Active Power

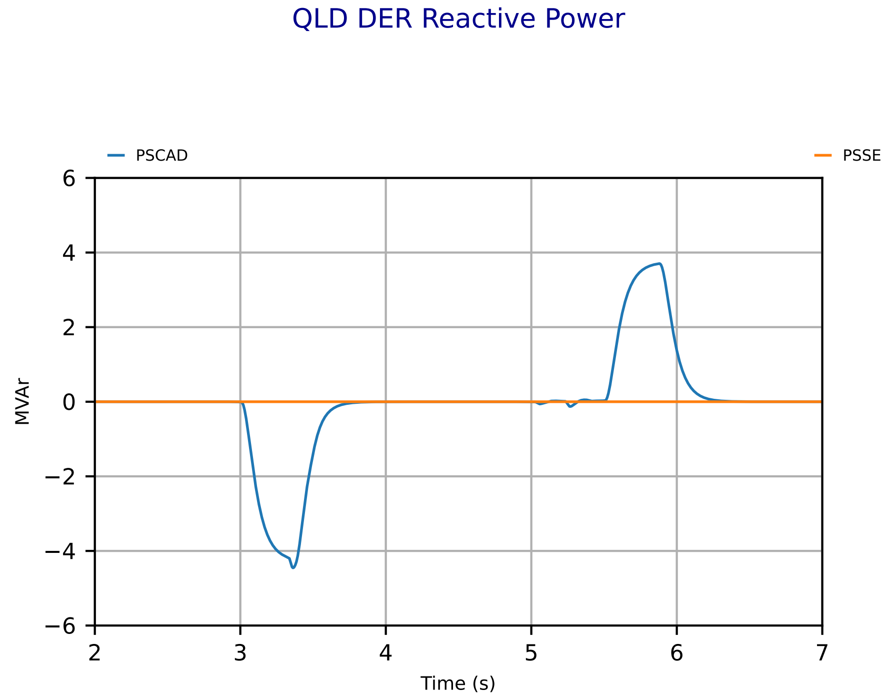


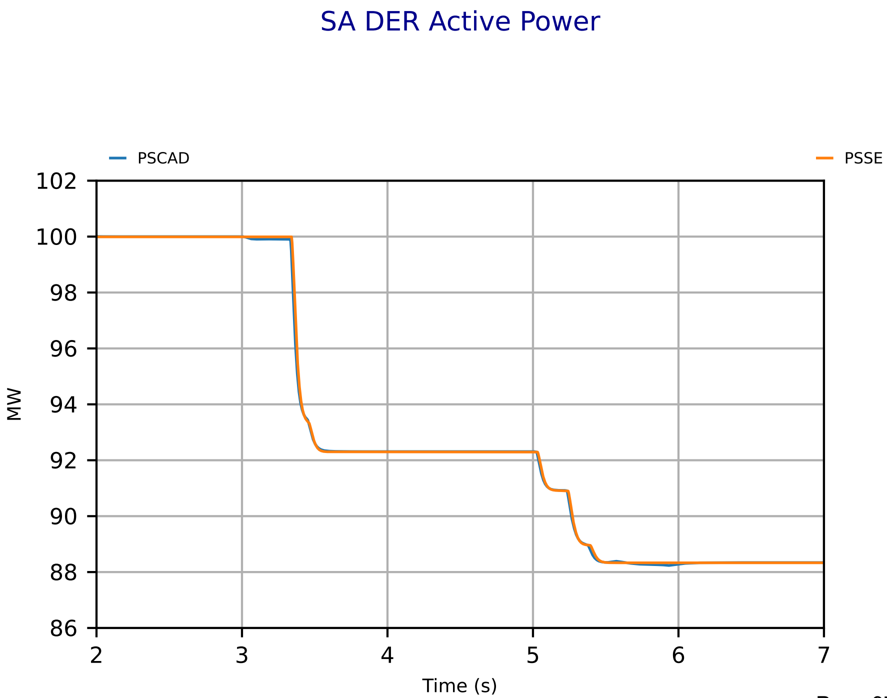
VIC DER Reactive Power

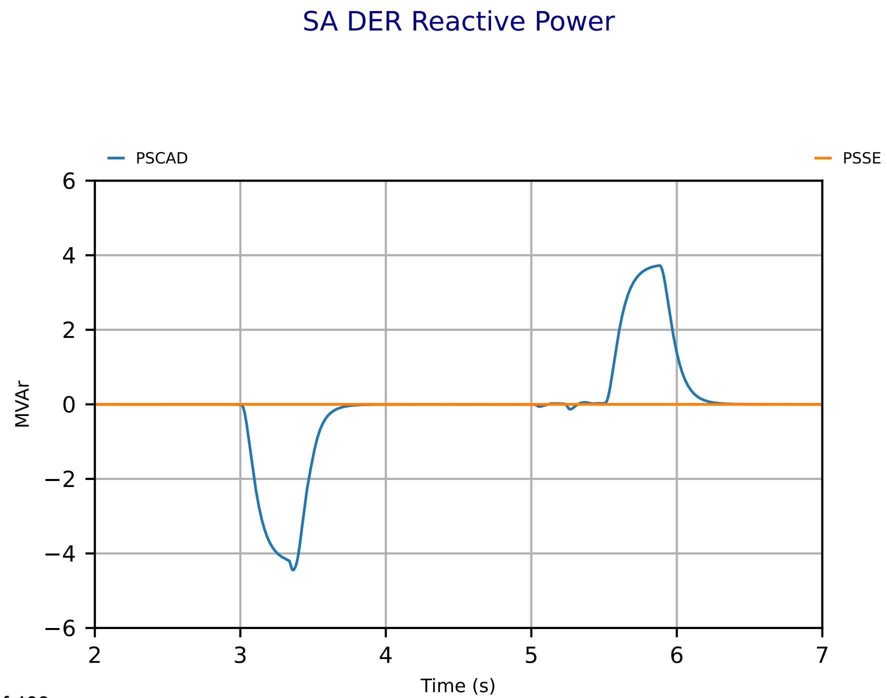


DER_SMIB_SCR_3_XR_14_T8_3









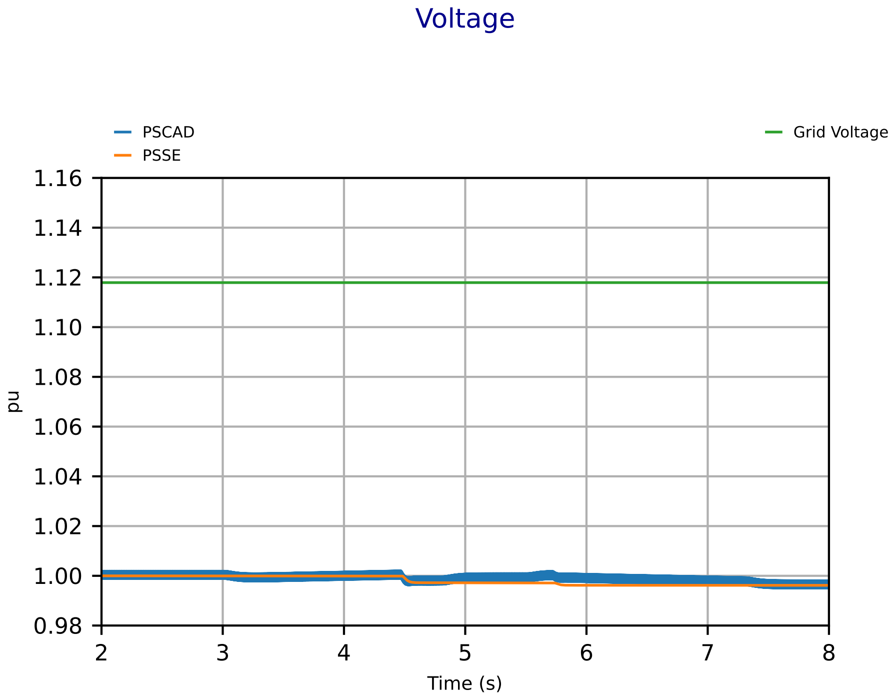
DER SMIB

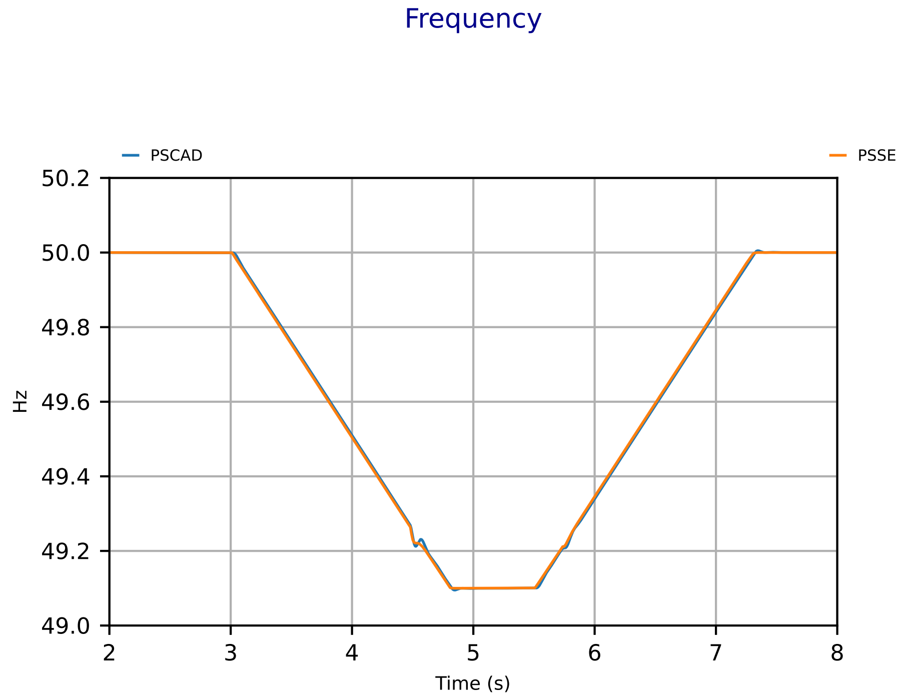
SCR = 3, X/R = 14

Test #9:

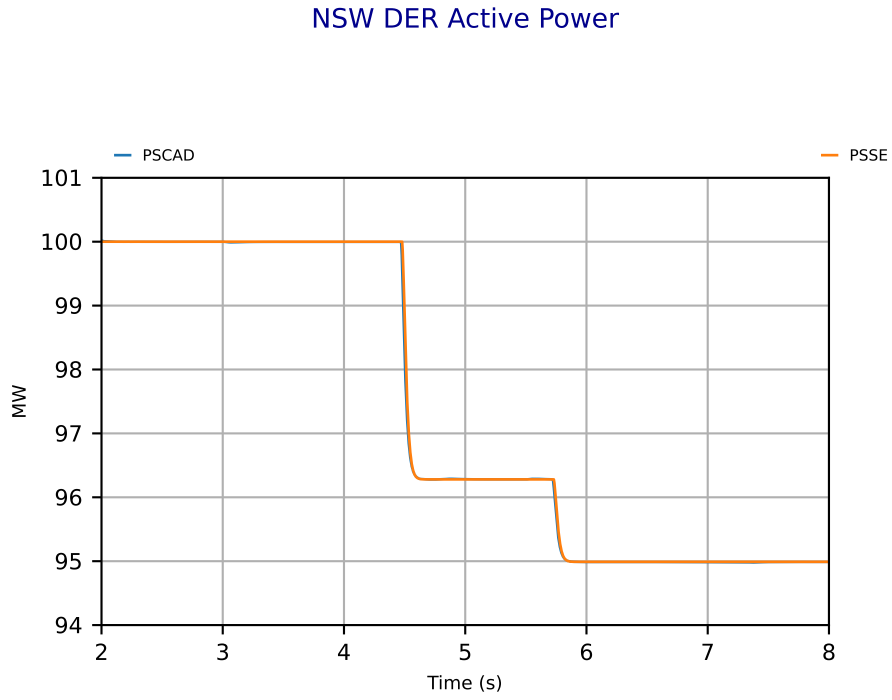
49.1 Hz slow frequency ramp (0.5 Hz/s)

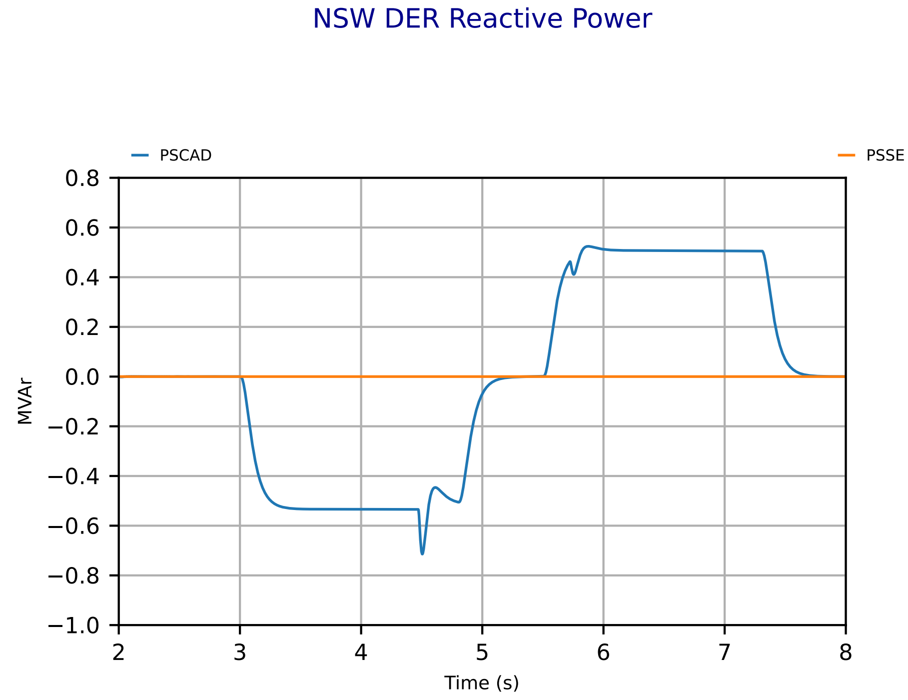
DER_SMIB_SCR_3_XR_14_T9_1

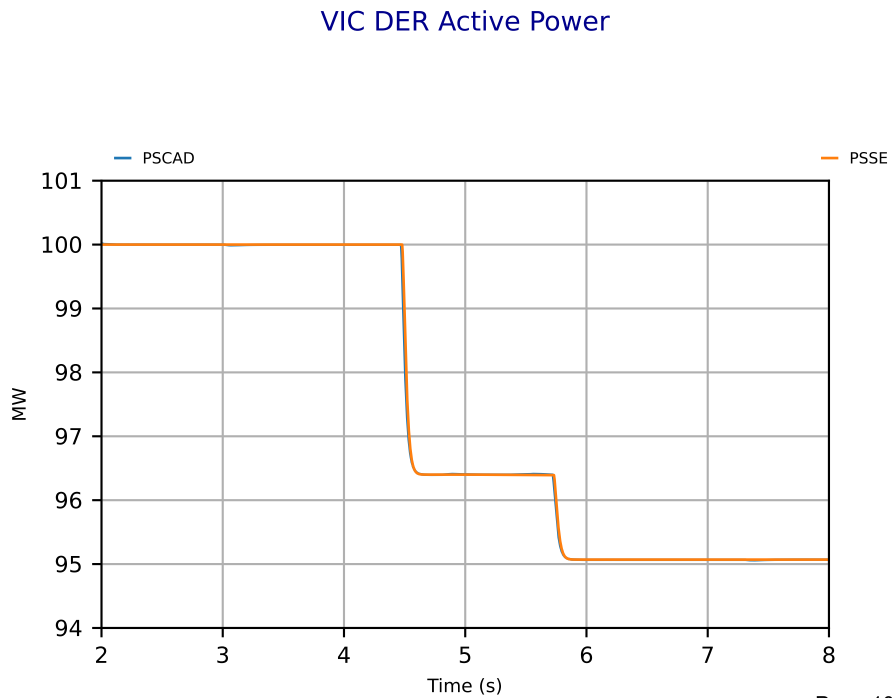


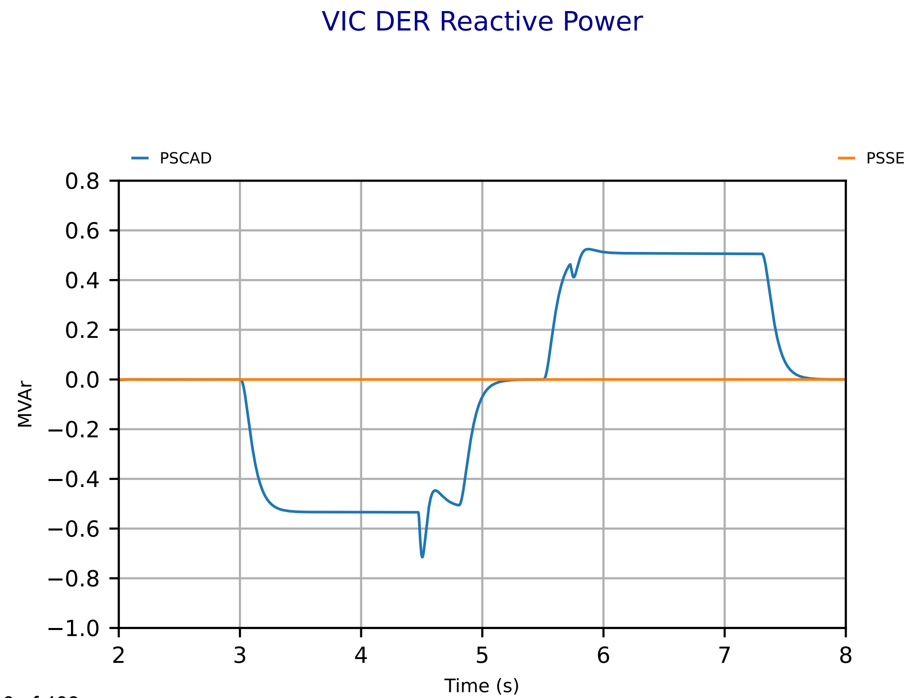


DER_SMIB_SCR_3_XR_14_T9_2

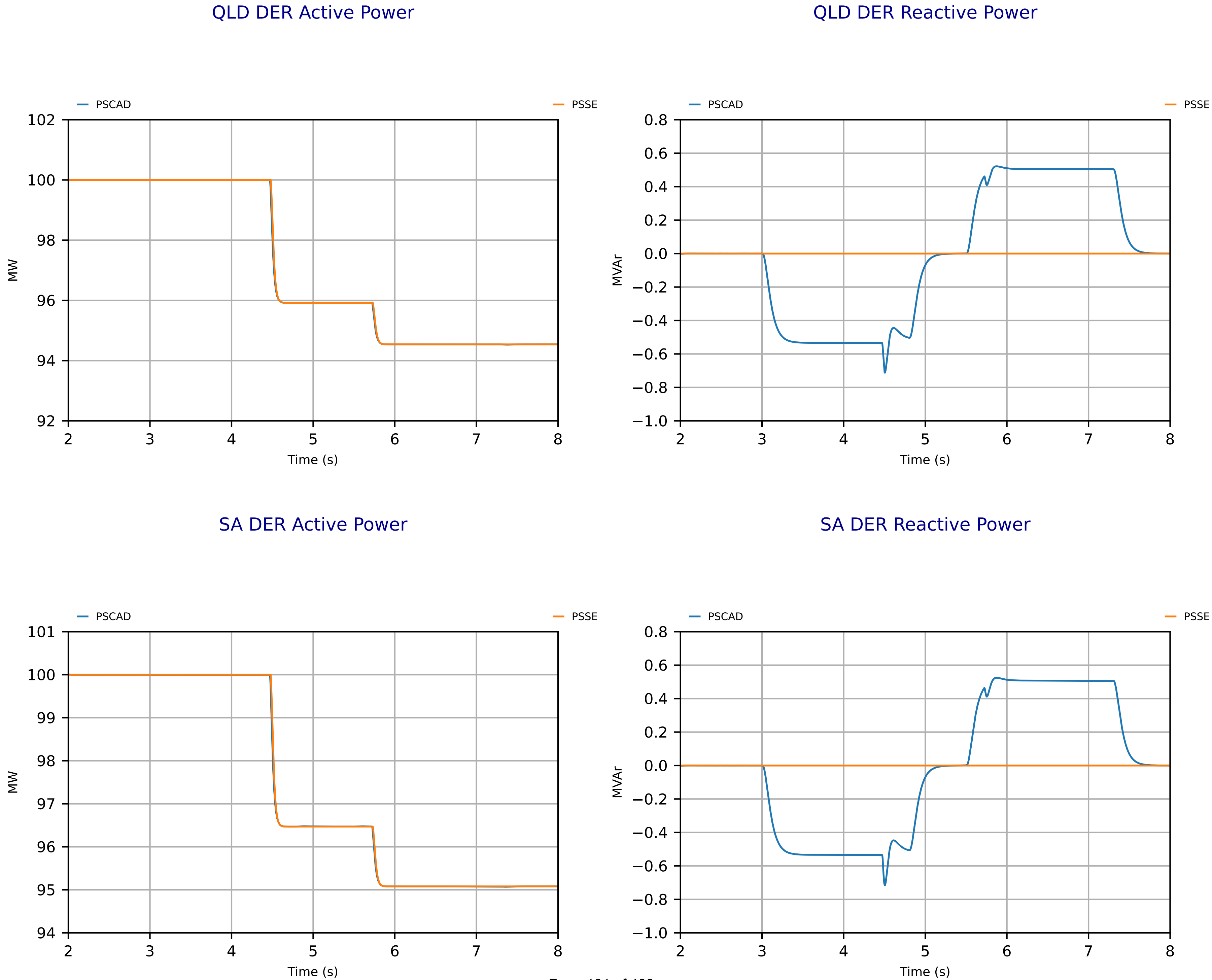








DER_SMIB_SCR_3_XR_14_T9_3

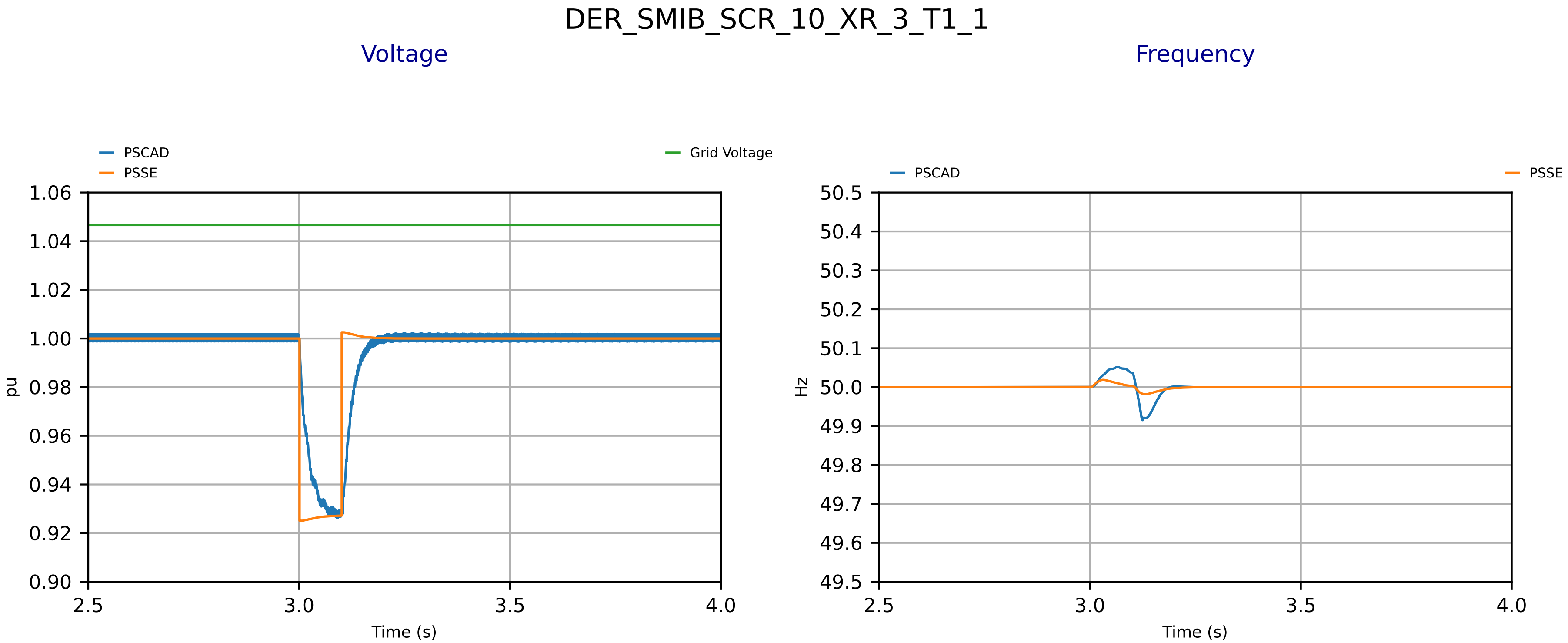


DER SMIB

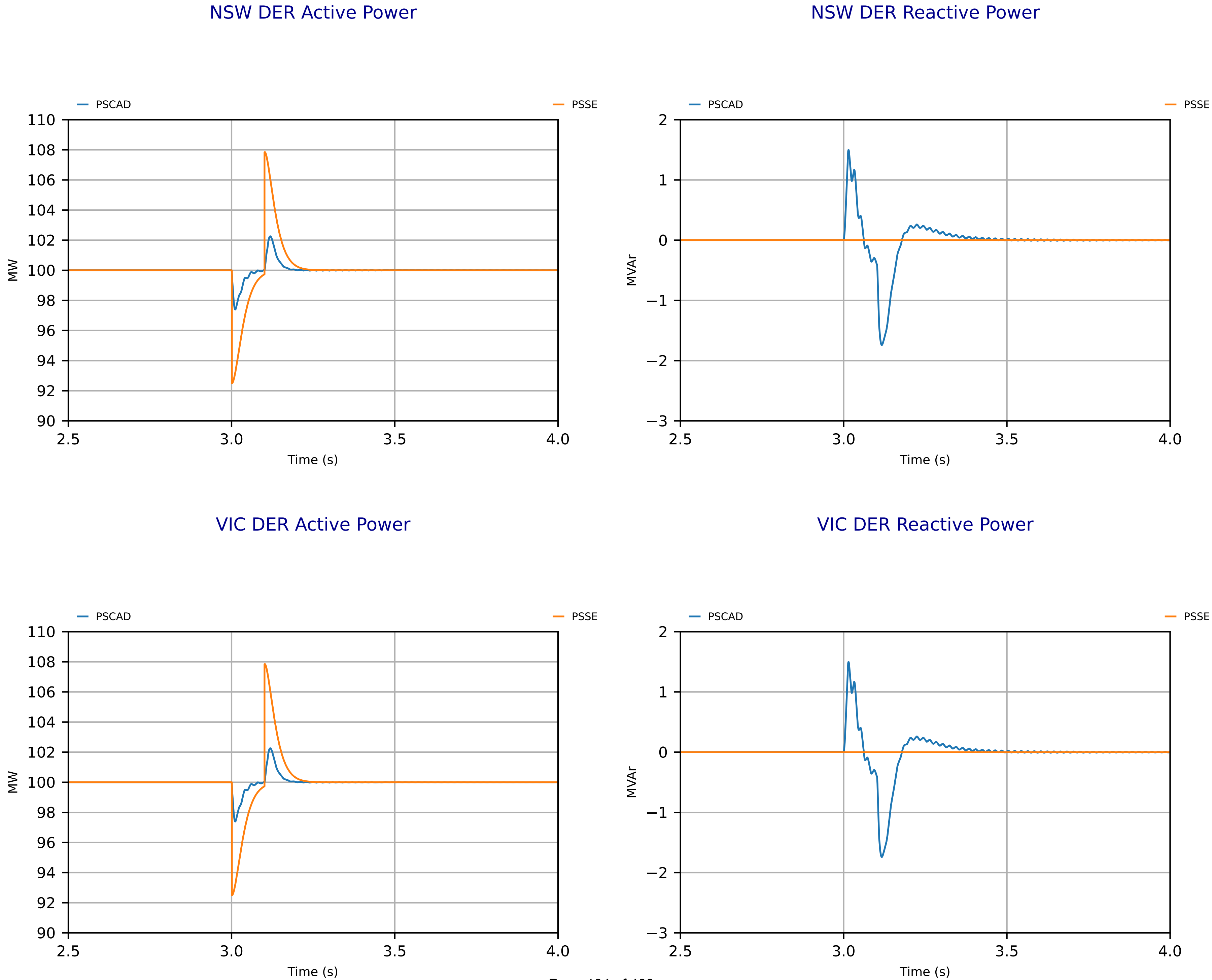
SCR = 10, X/R = 3

Test #1:

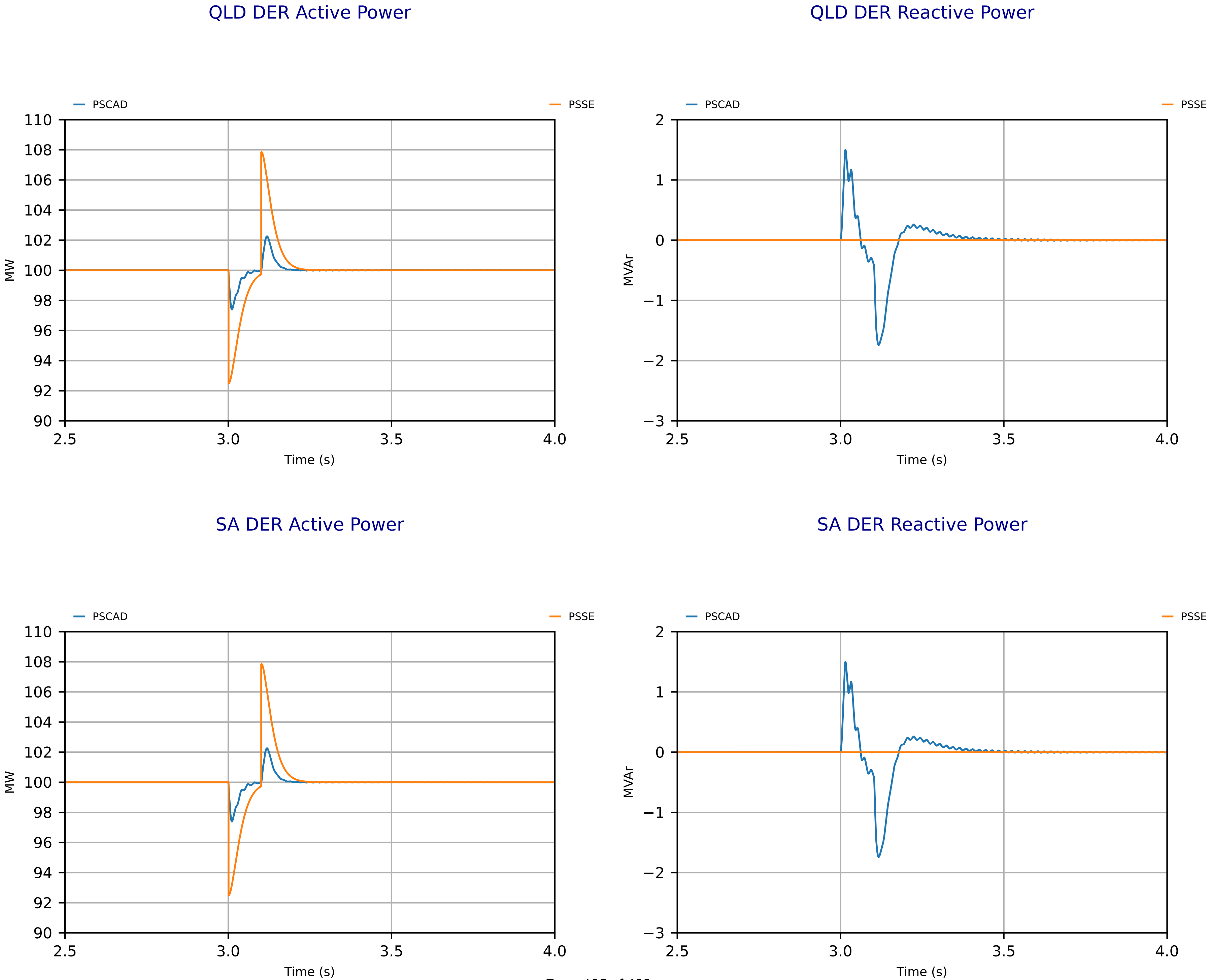
LG fault for 100 ms


DER_SMIB_SCR_10_XR_3_T1_1
Voltage
PSCAD
PSSE
Grid Voltage
pu
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
0.90
2.5
3.0
3.5
4.0
Time (s)
Frequency
PSCAD
PSSE
Hz
50.5
50.4
50.3
50.2
50.1
50.0
49.9
49.8
49.7
49.6
49.5
2.5
3.0
3.5
4.0
Time (s)

DER_SMIB_SCR_10_XR_3_T1_2



DER_SMIB_SCR_10_XR_3_T1_3



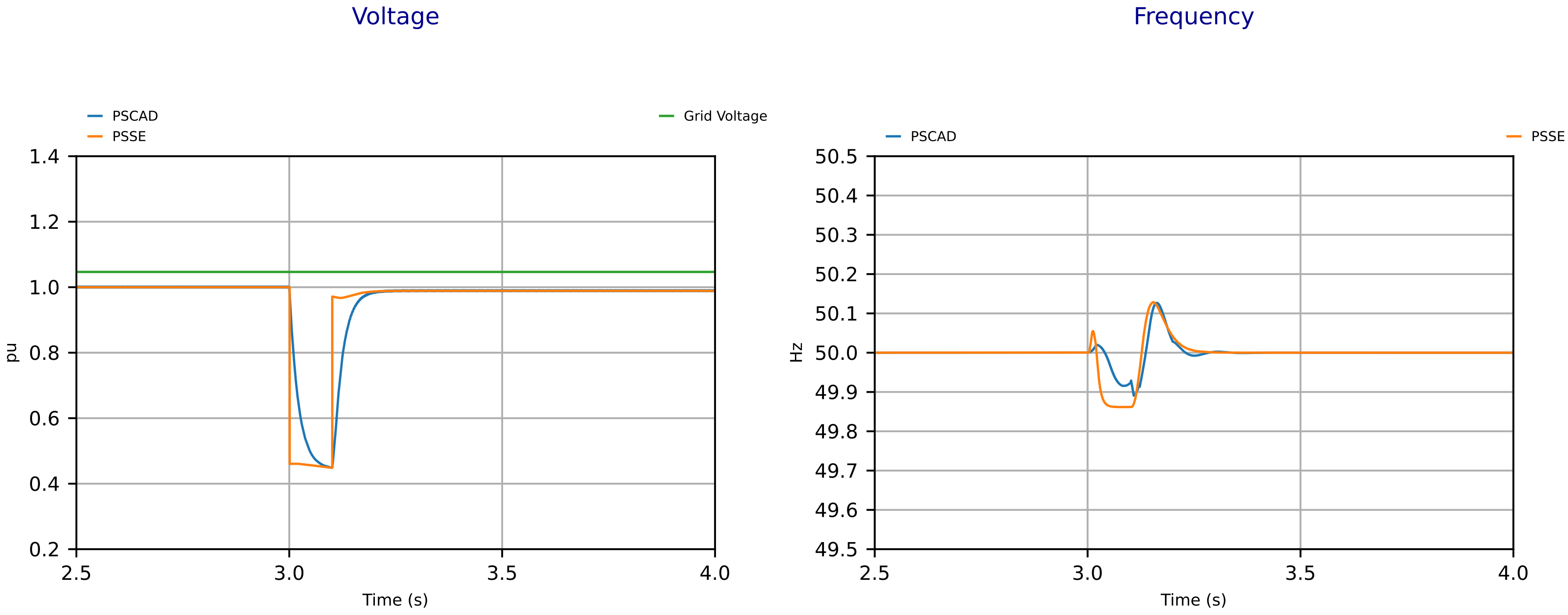
DER SMIB

SCR = 10, X/R = 3

Test #2:

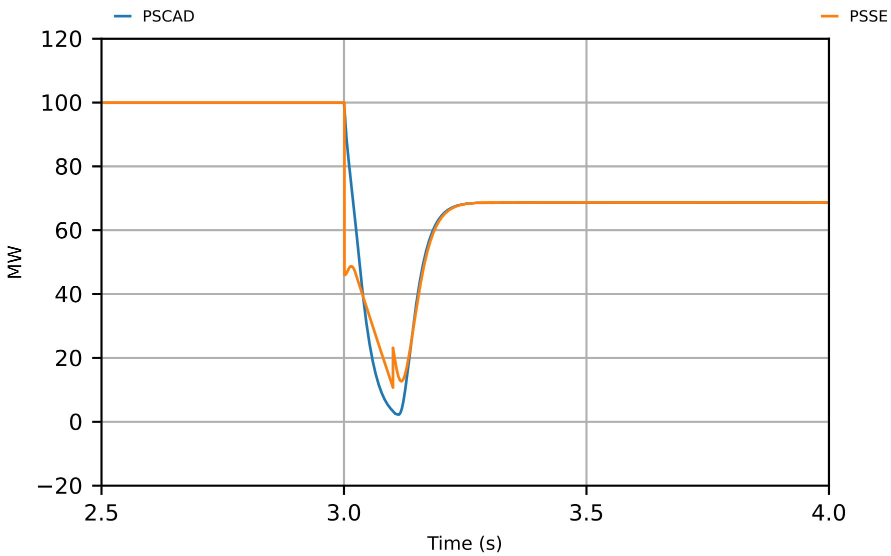
LLG fault for 100 ms

DER_SMIB_SCR_10_XR_3_T2_1

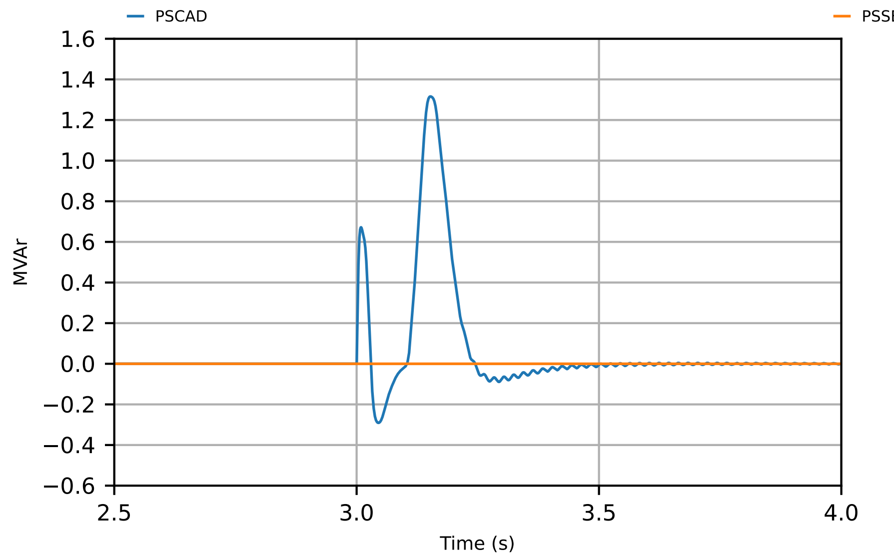


DER_SMIB_SCR_10_XR_3_T2_2

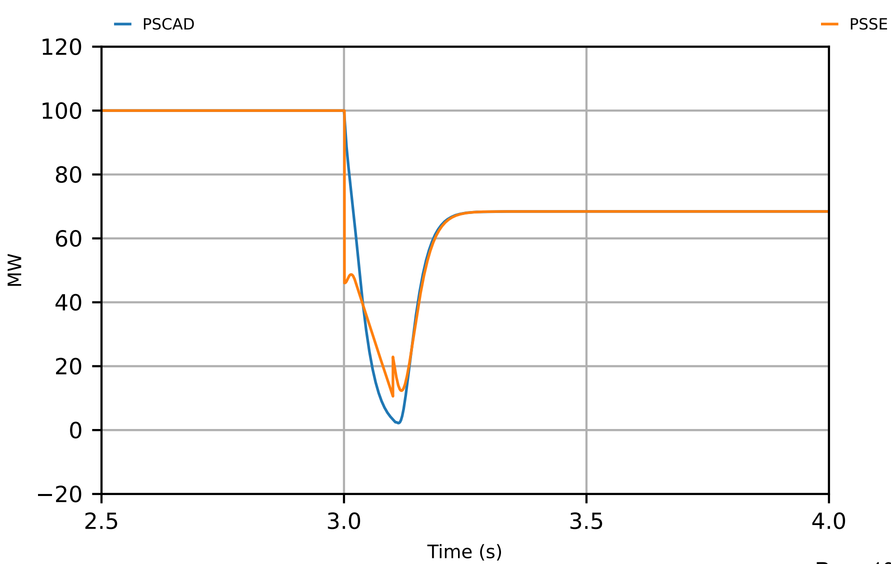
NSW DER Active Power



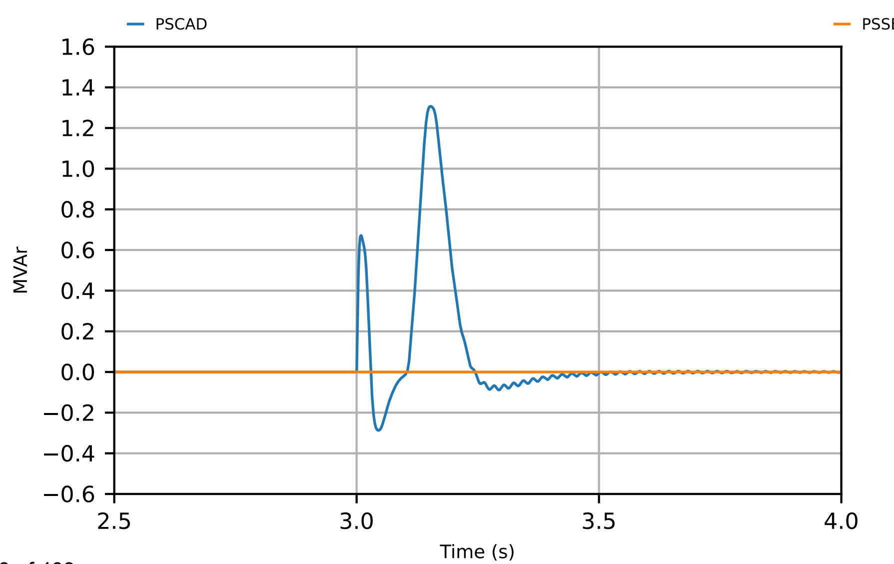
NSW DER Reactive Power



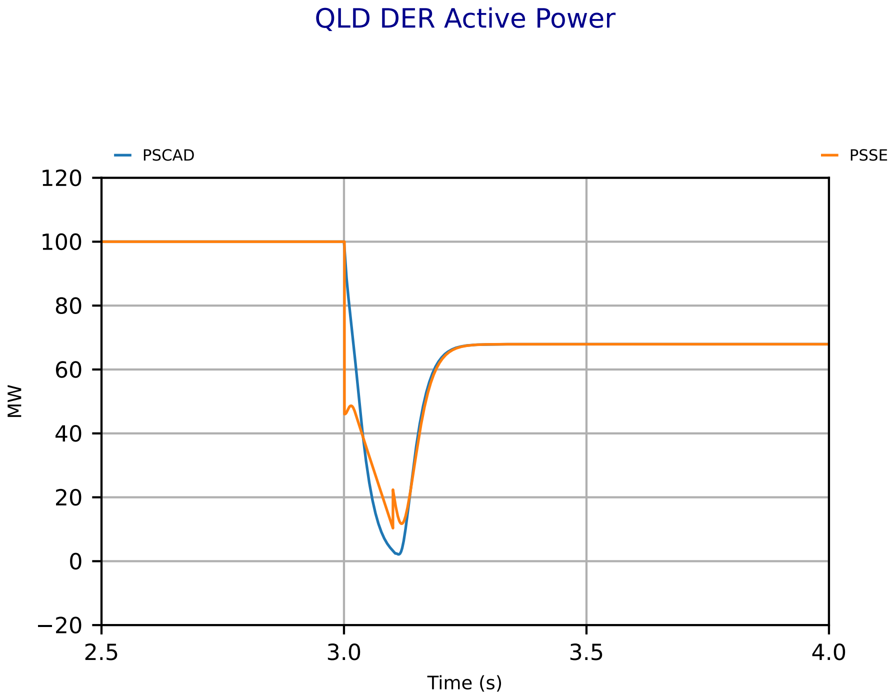
VIC DER Active Power

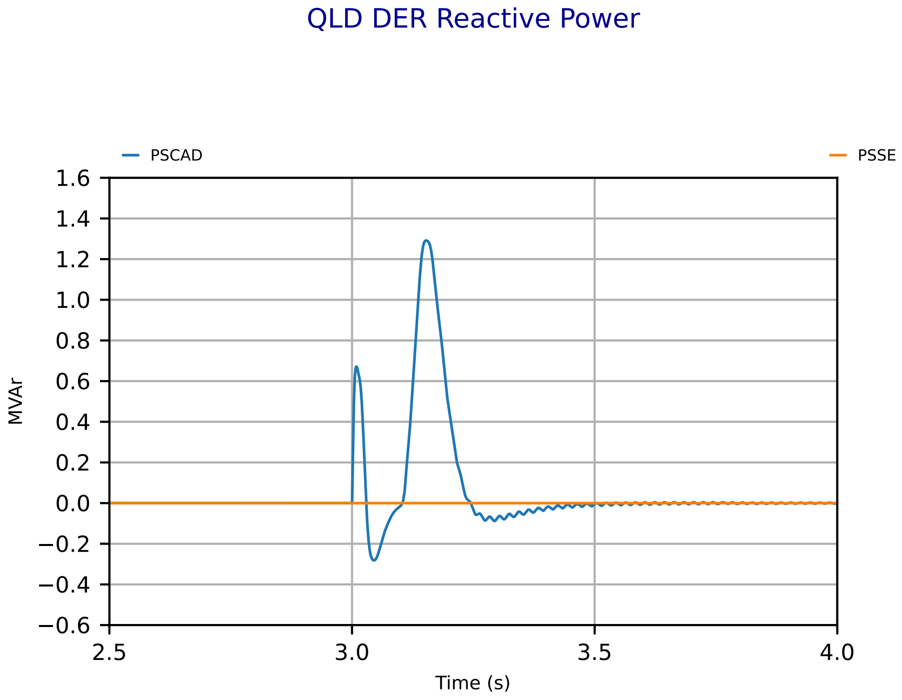


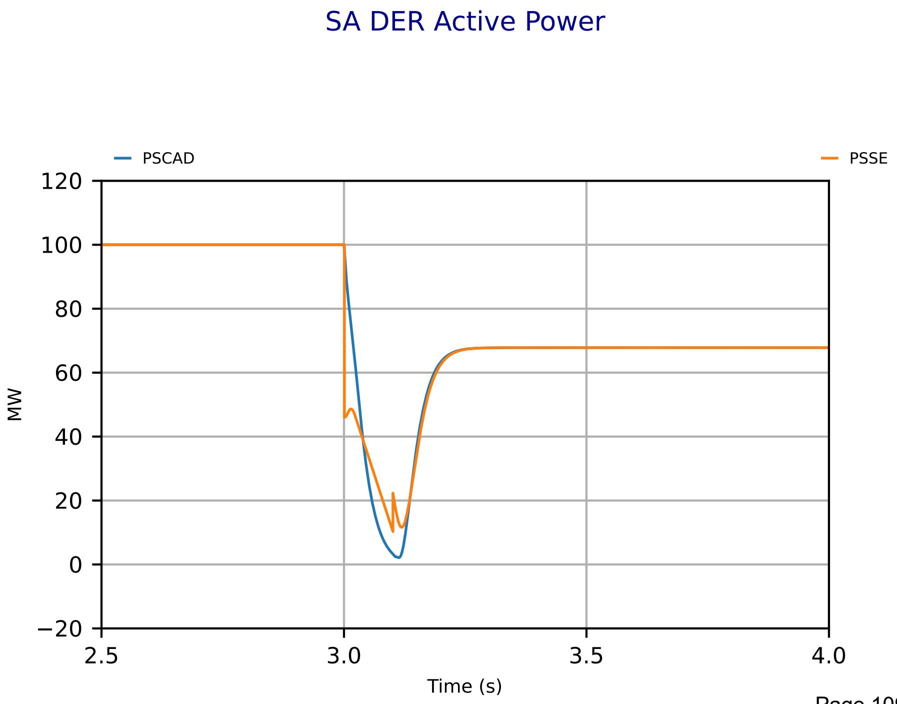
VIC DER Reactive Power

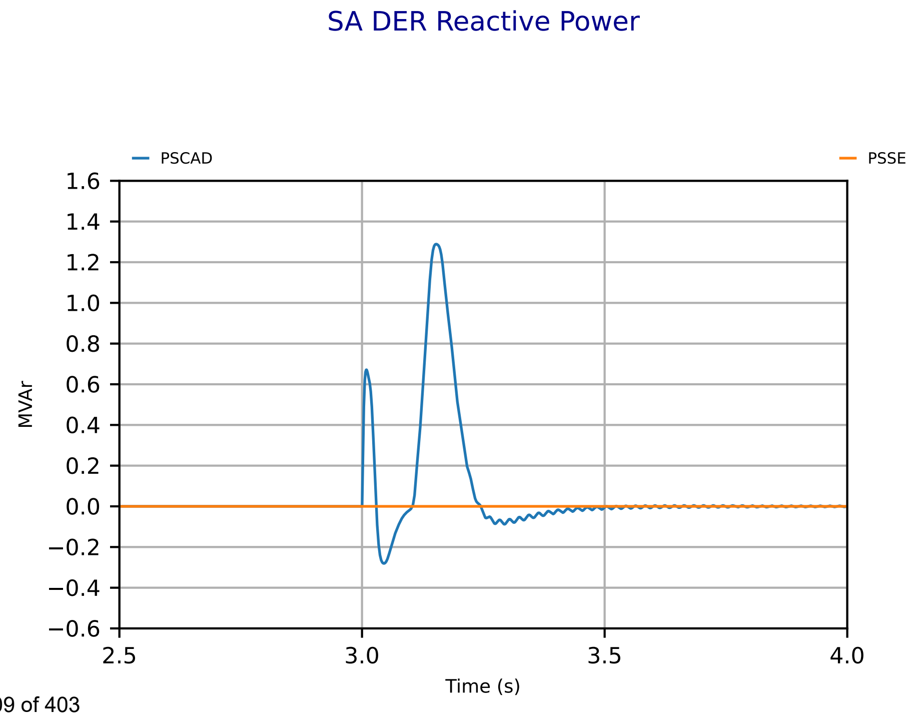


DER_SMIB_SCR_10_XR_3_T2_3









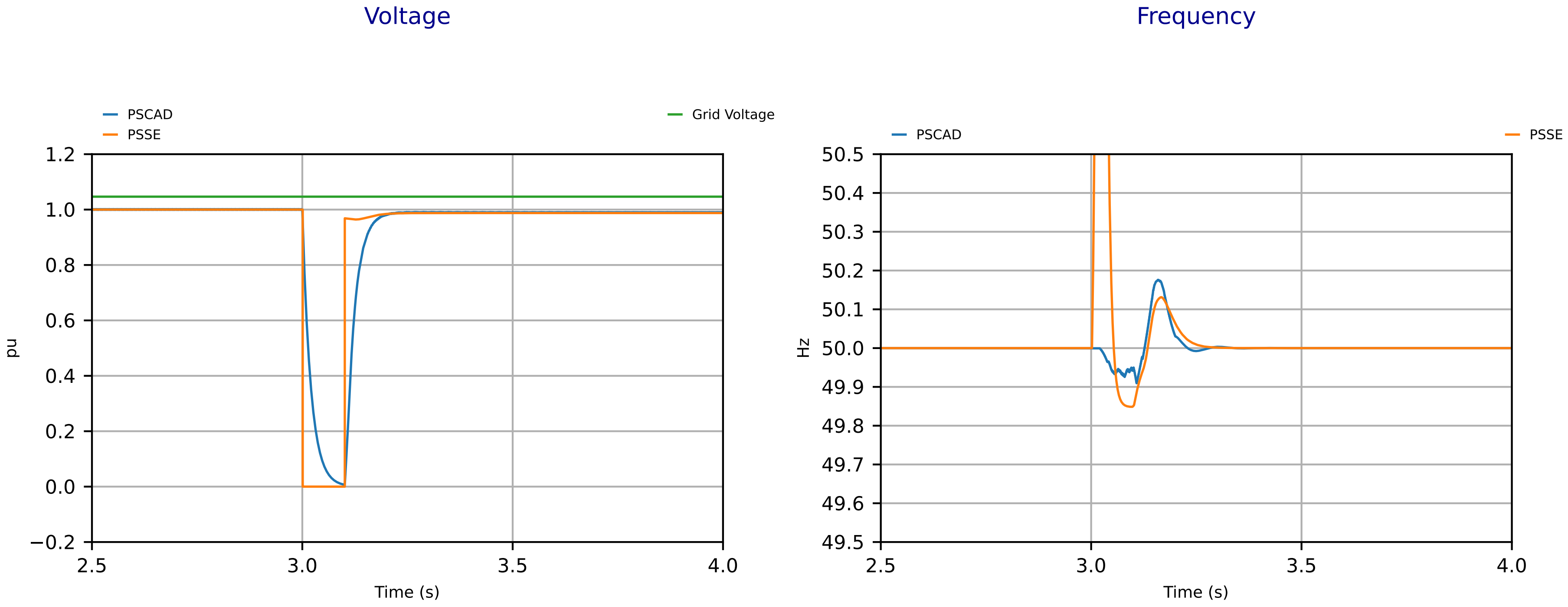
DER SMIB

SCR = 10, X/R = 3

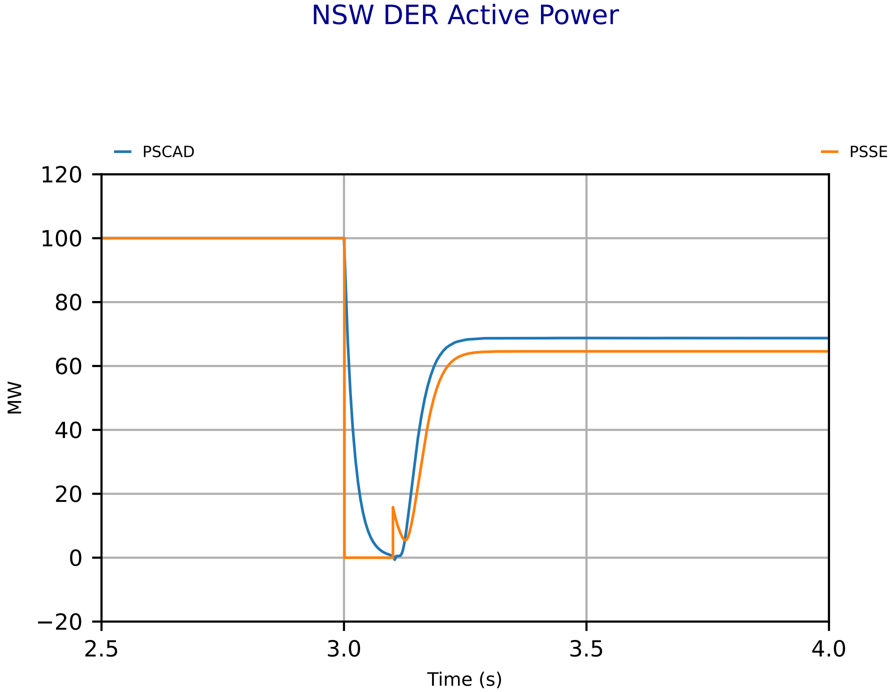
Test #3:

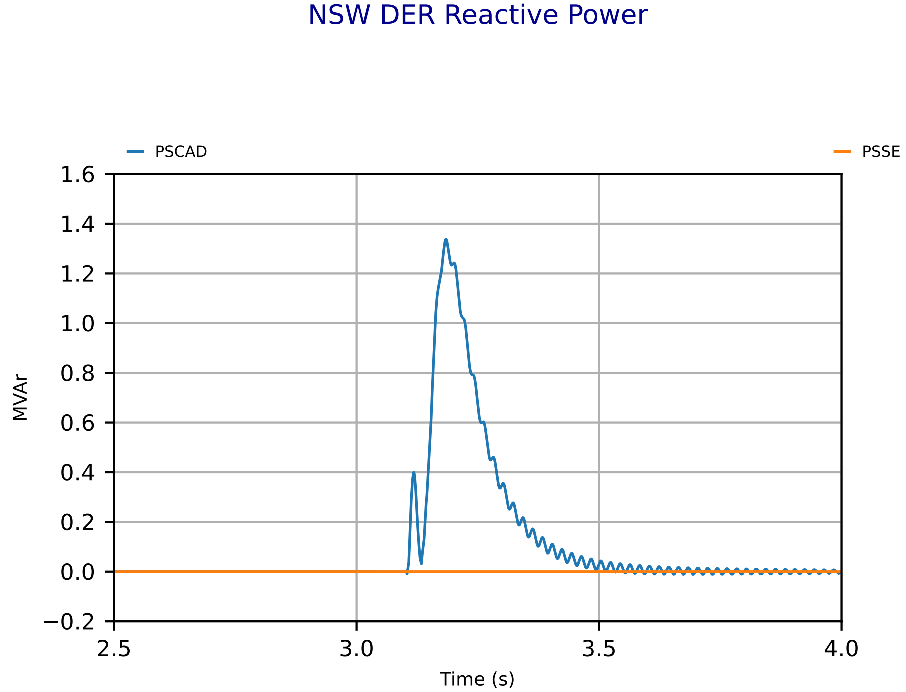
3PH-G fault for 100 ms

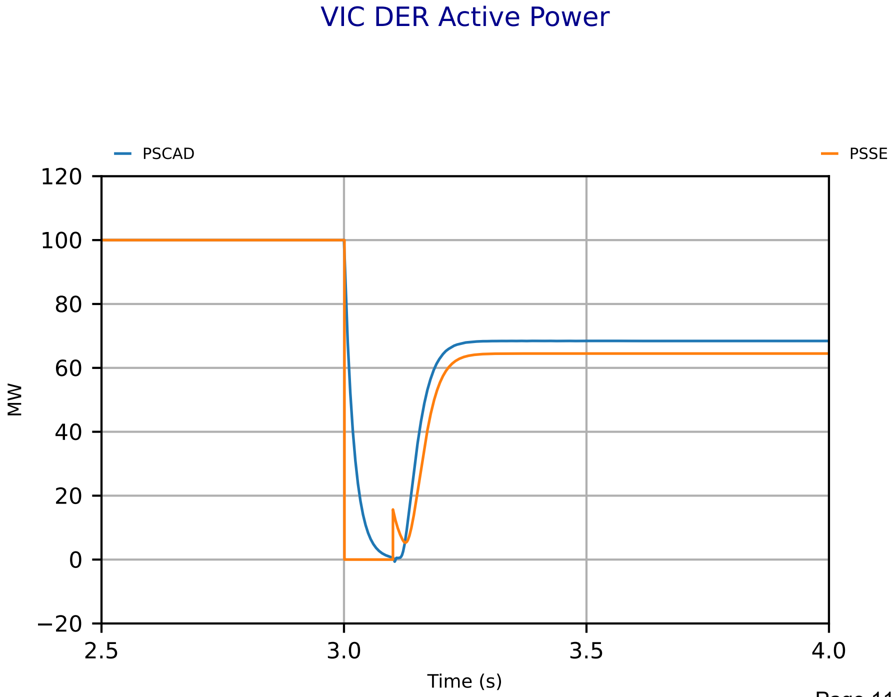
DER_SMIB_SCR_10_XR_3_T3_1

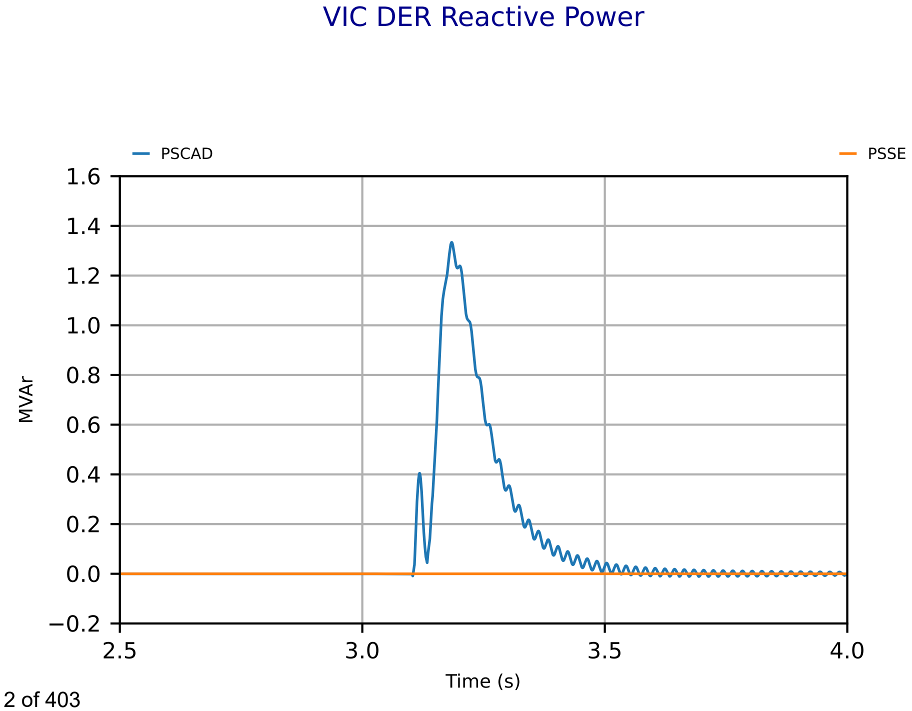


DER_SMIB_SCR_10_XR_3_T3_2

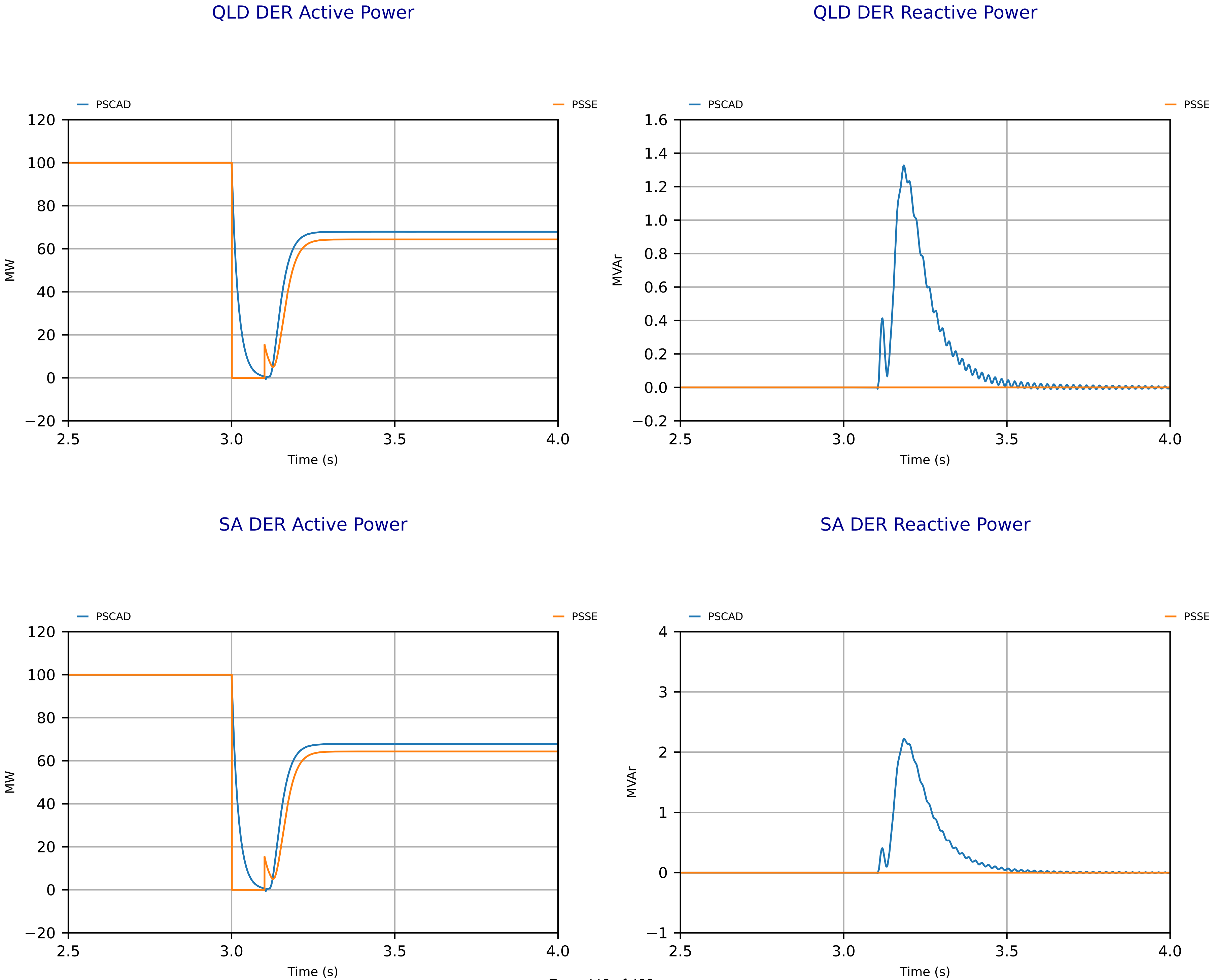








DER_SMIB_SCR_10_XR_3_T3_3



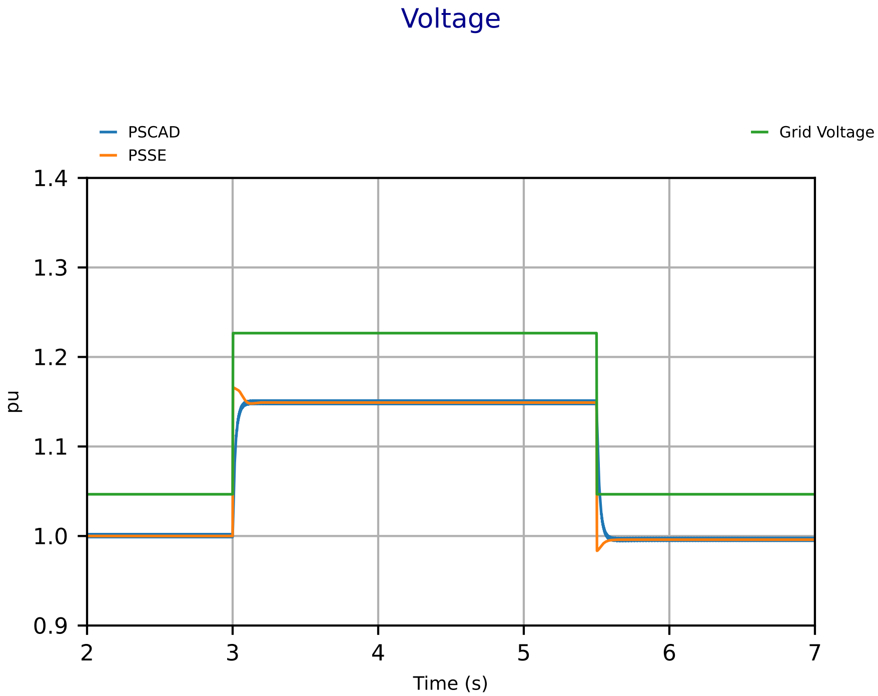
DER SMIB

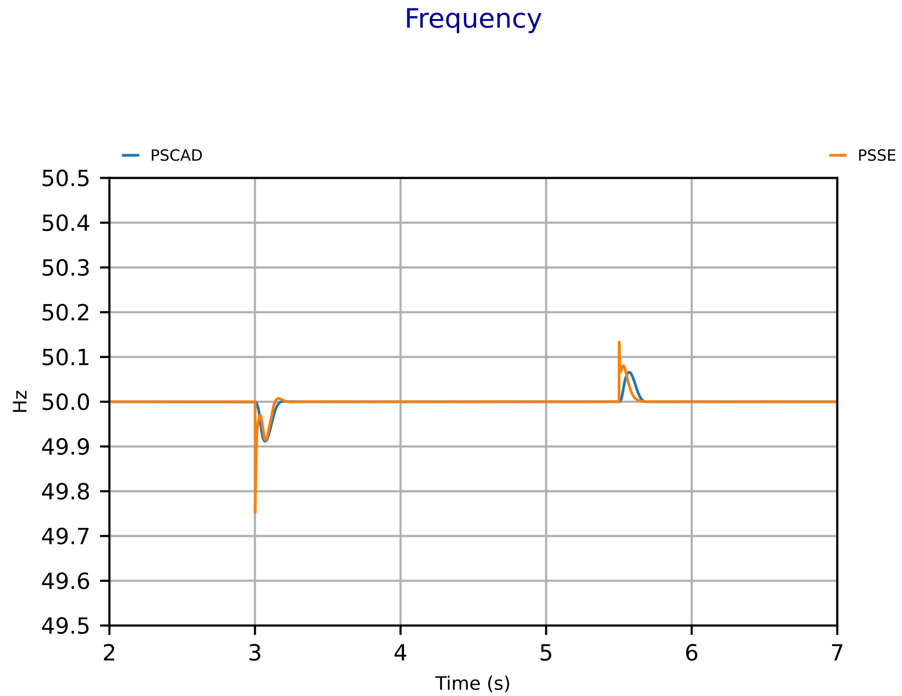
SCR = 10, X/R = 3

Test #4:

~115% Voltage disturbance for 2.5 s

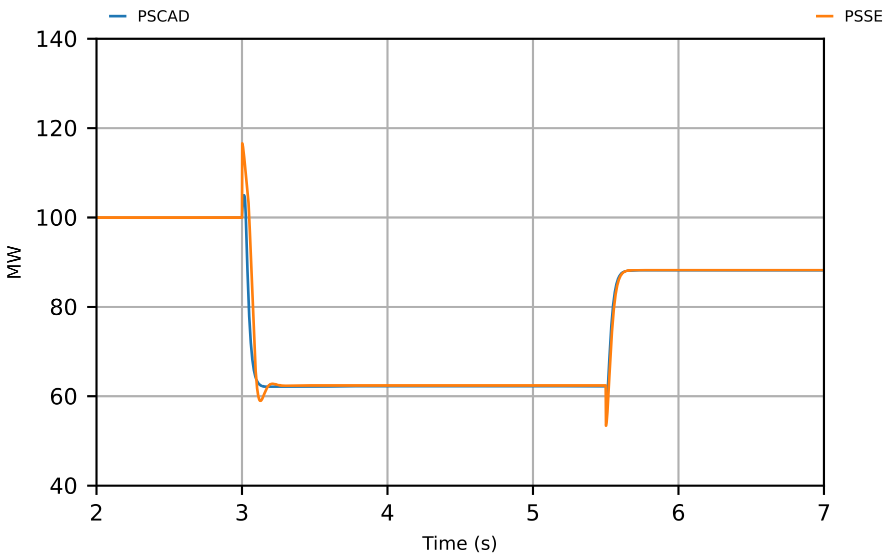
DER_SMIB_SCR_10_XR_3_T4_1



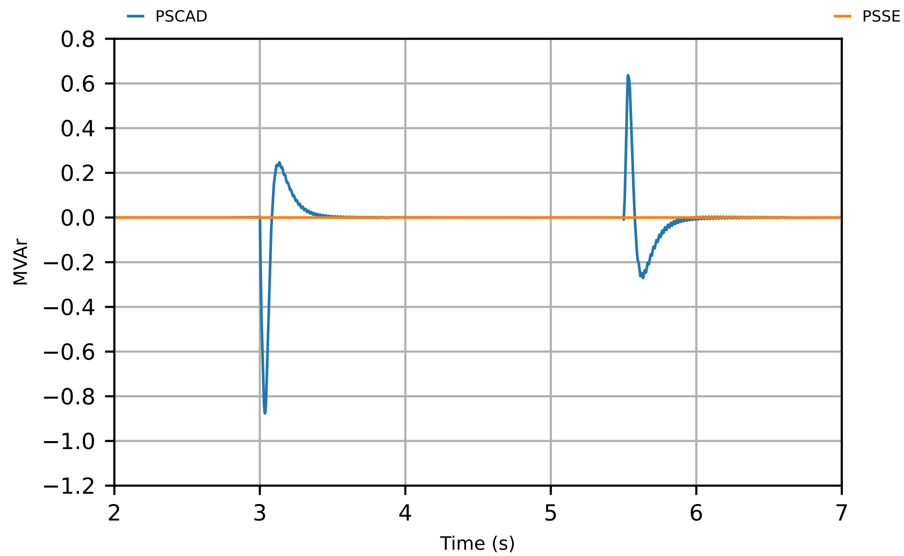


DER_SMIB_SCR_10_XR_3_T4_2

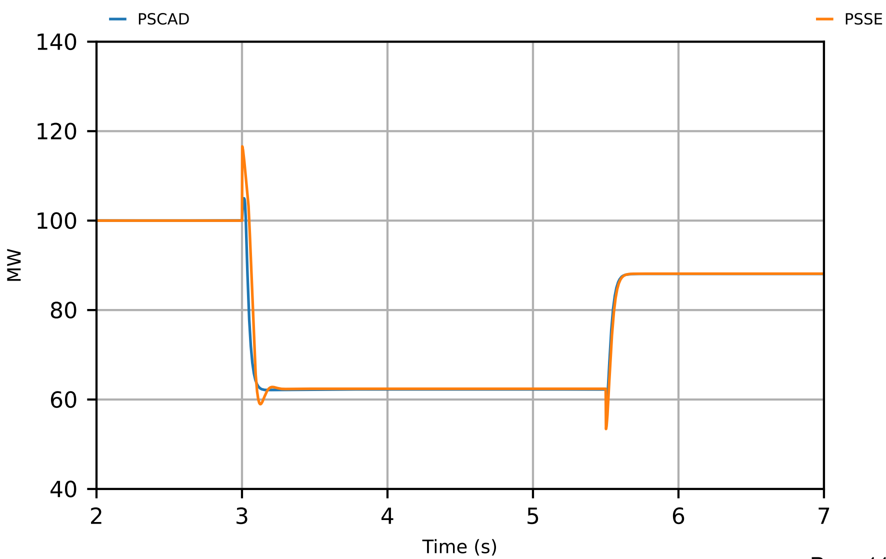
NSW DER Active Power



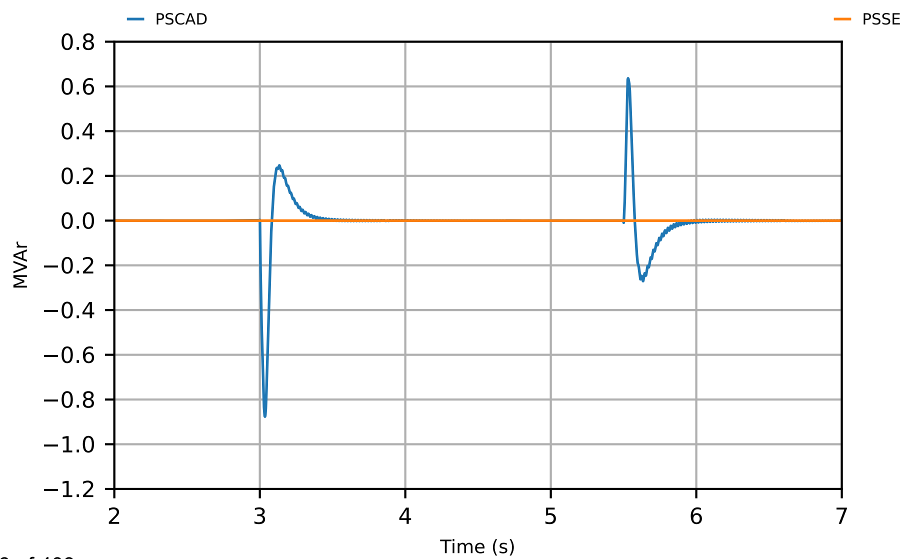
NSW DER Reactive Power



VIC DER Active Power

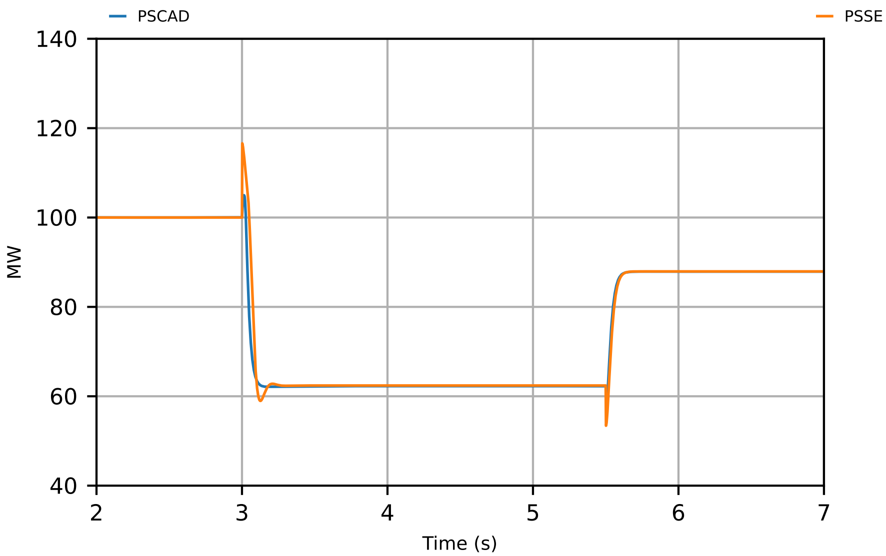


VIC DER Reactive Power

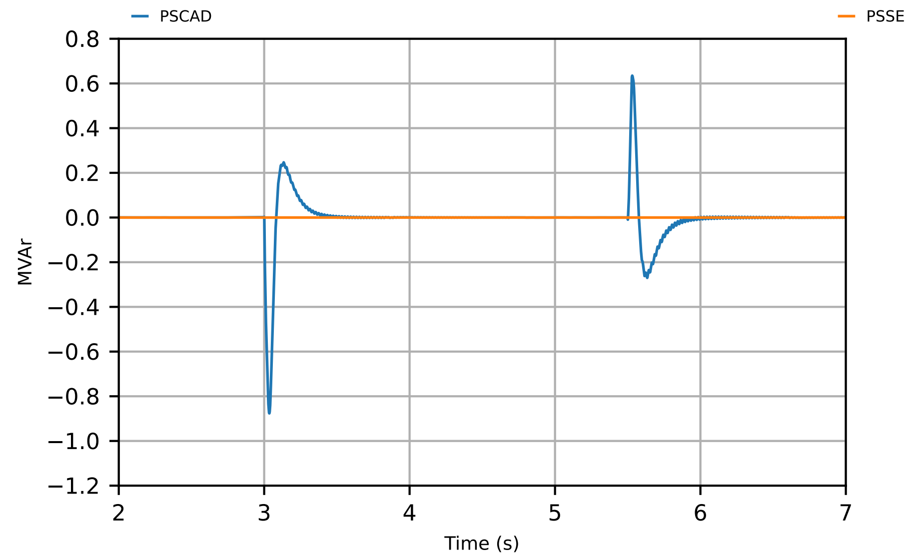


DER_SMIB_SCR_10_XR_3_T4_3

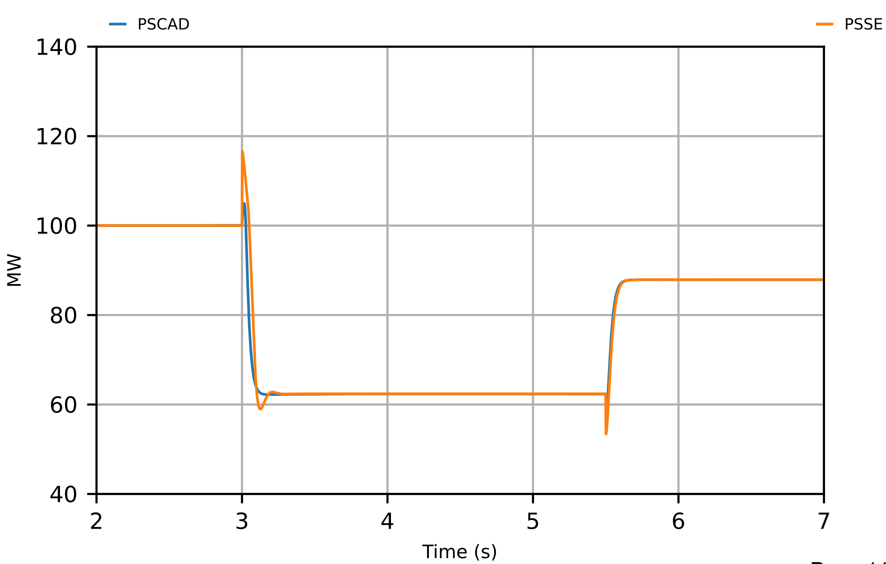
QLD DER Active Power



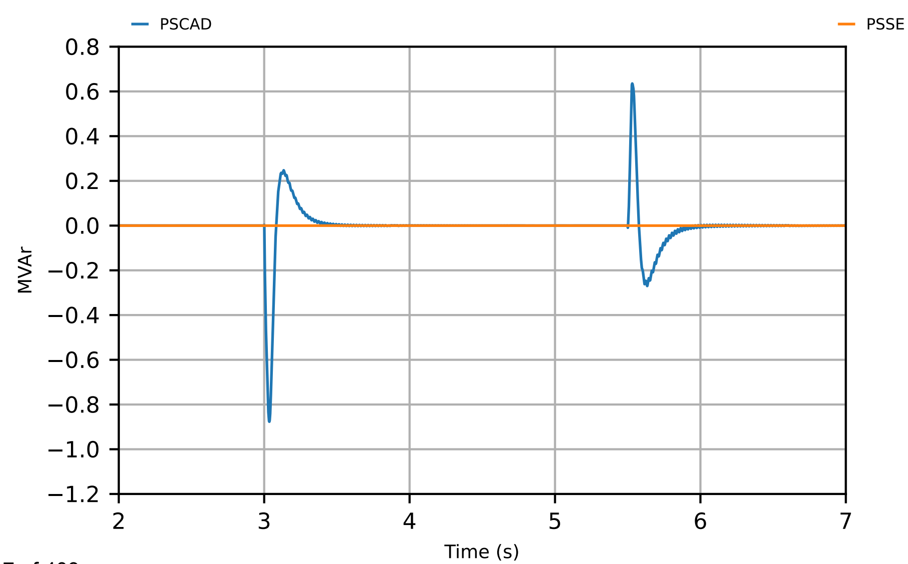
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



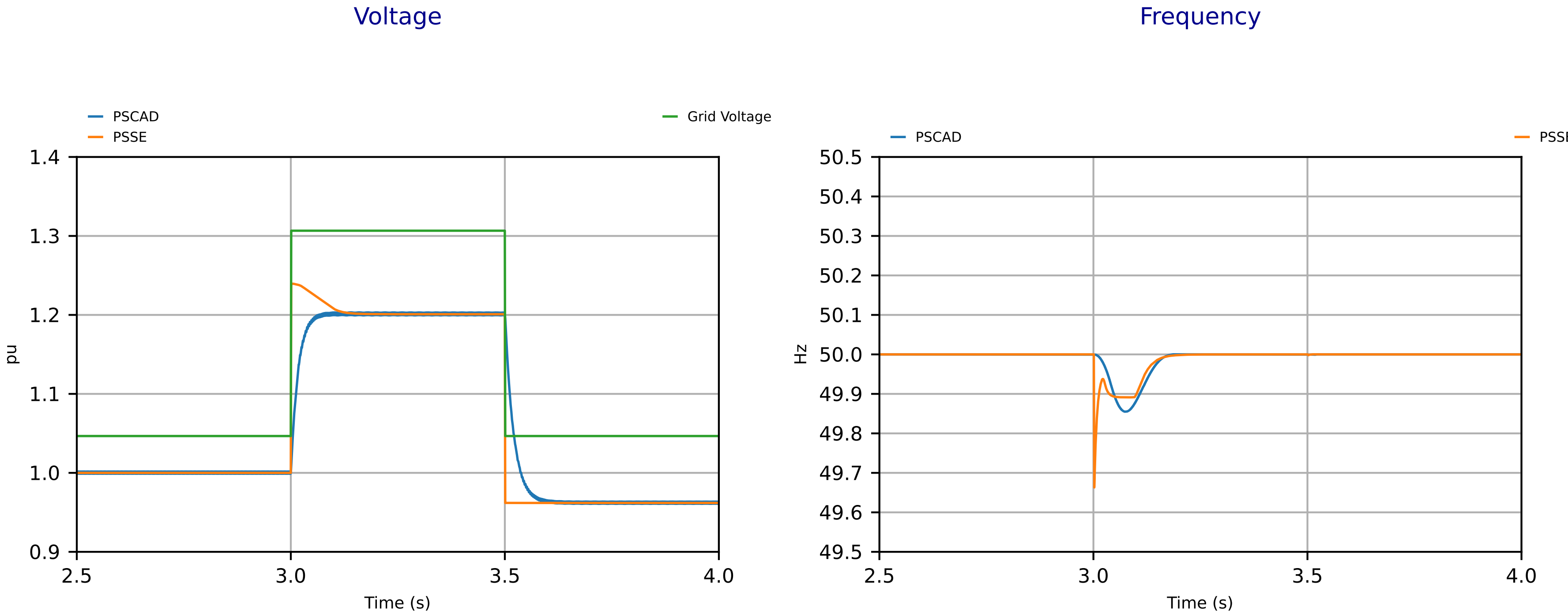
DER SMIB

SCR = 10, X/R = 3

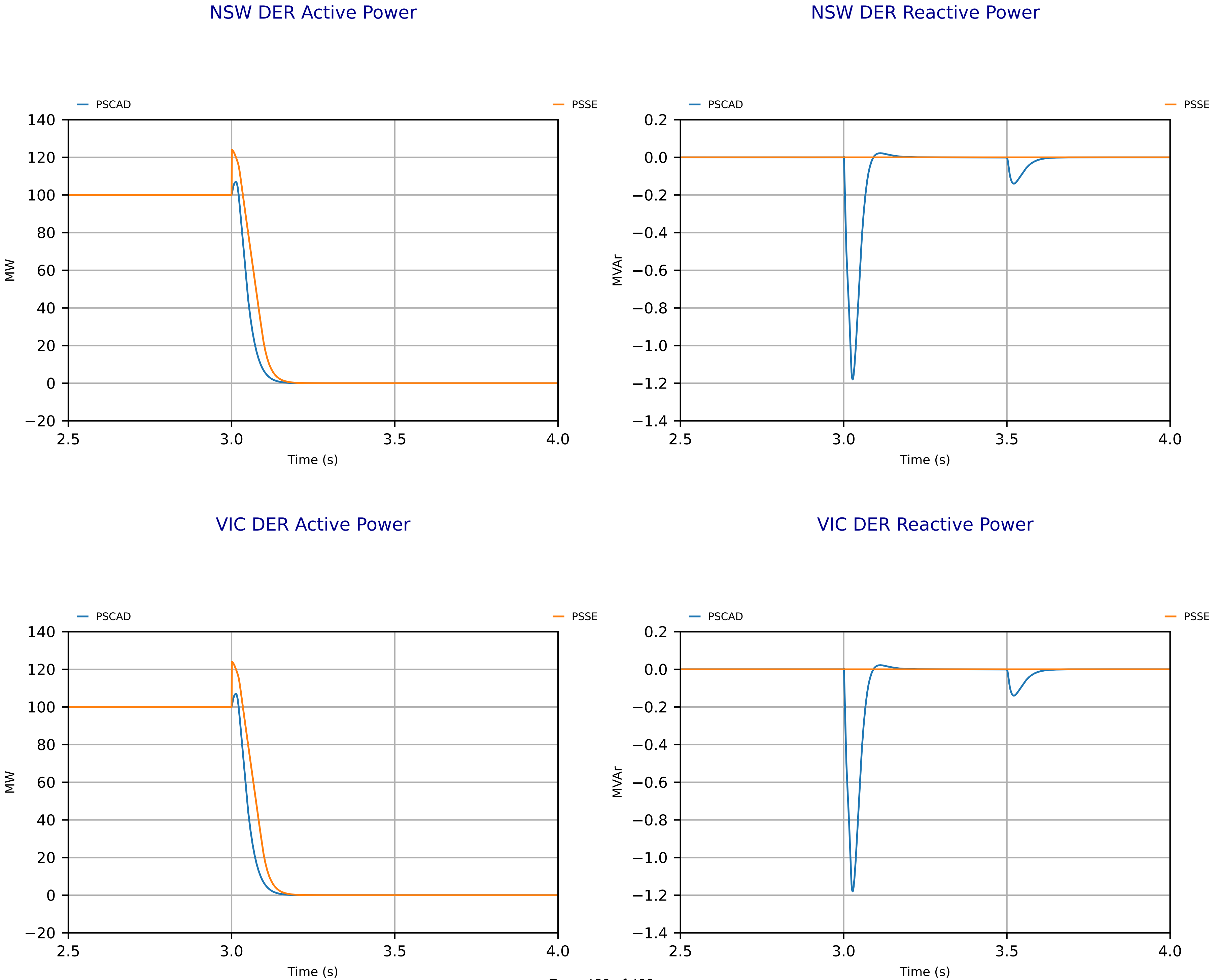
Test #5:

~120% Voltage disturbance for 500 ms

DER_SMIB_SCR_10_XR_3_T5_1

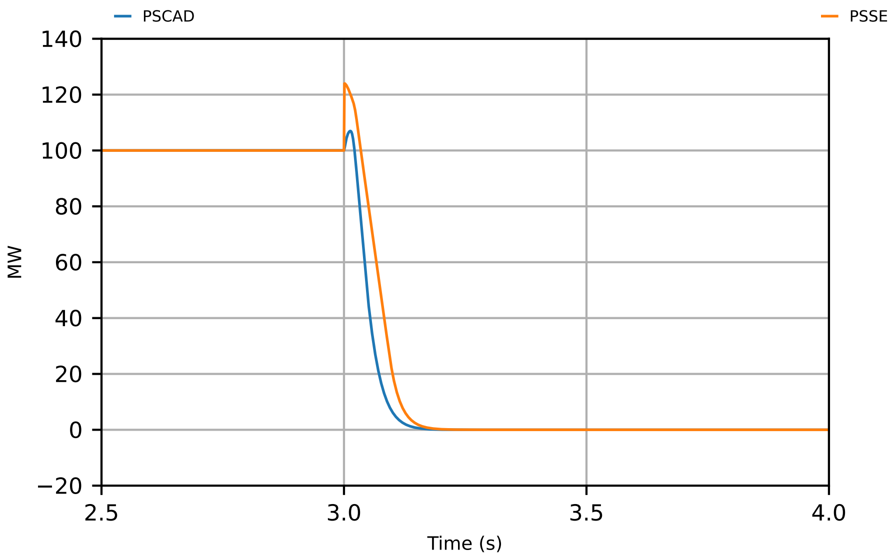


DER_SMIB_SCR_10_XR_3_T5_2

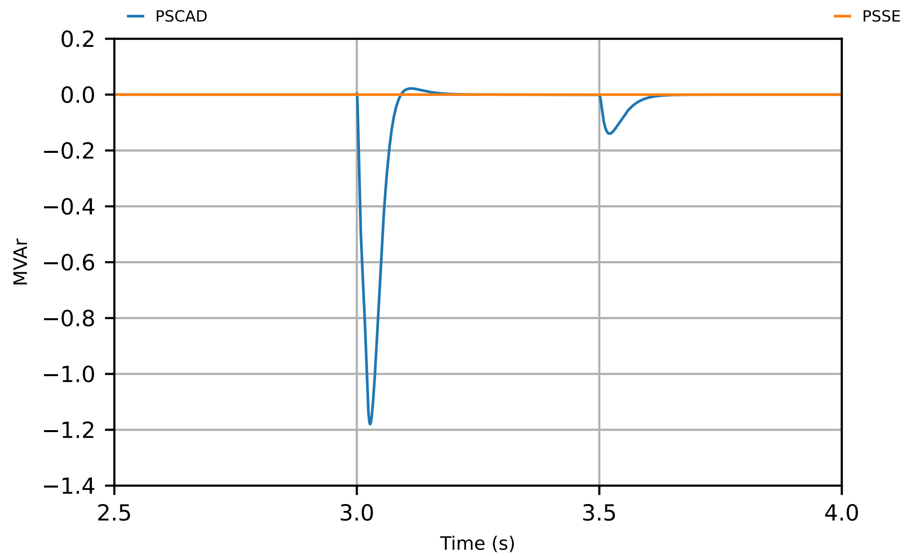


DER_SMIB_SCR_10_XR_3_T5_3

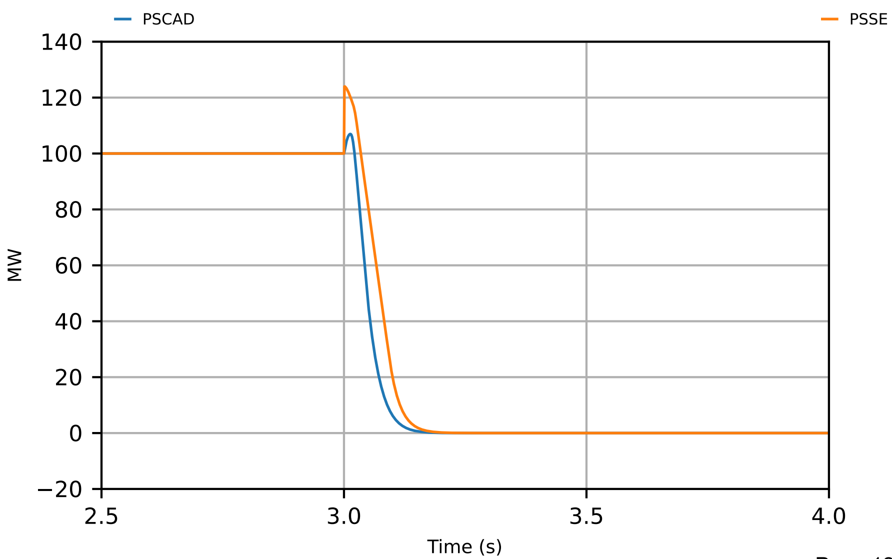
QLD DER Active Power



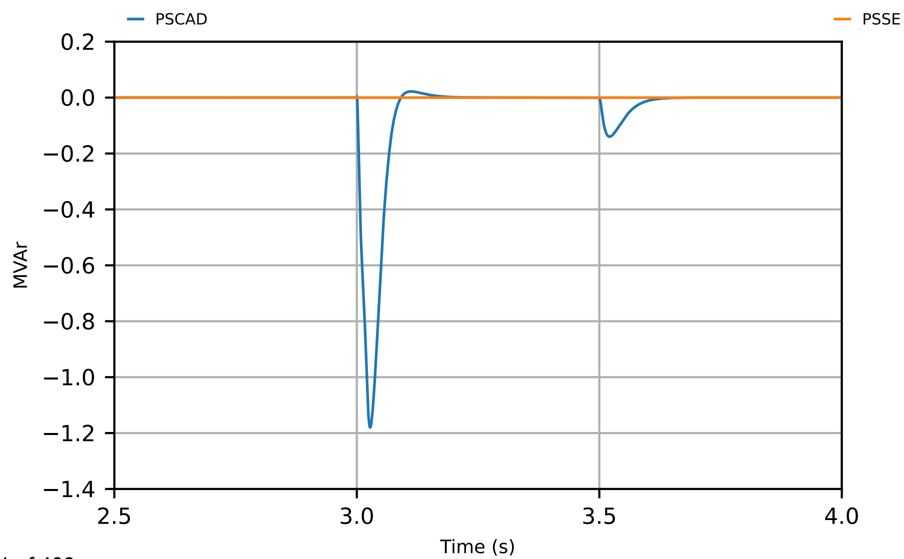
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



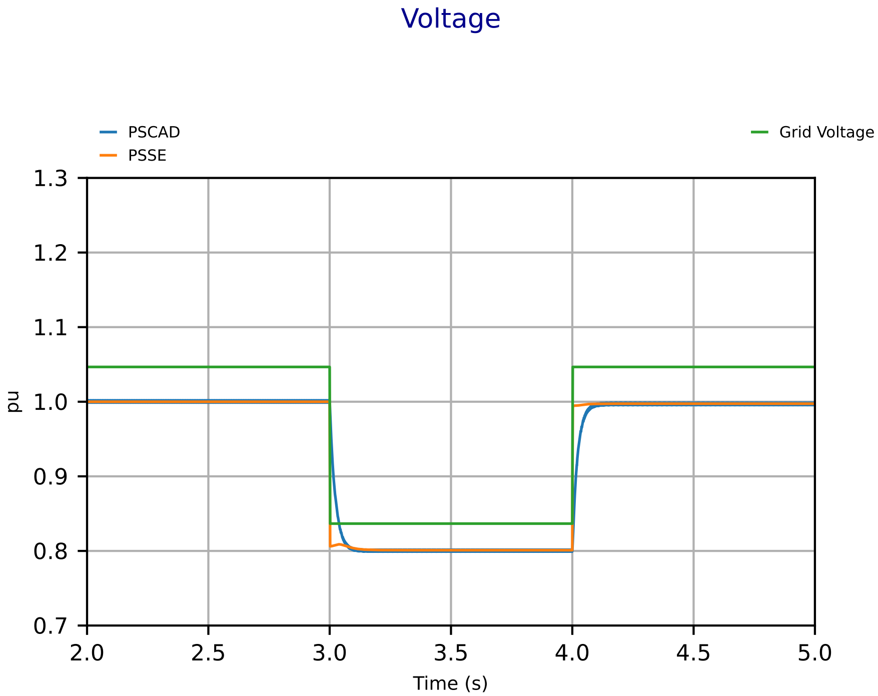
DER SMIB

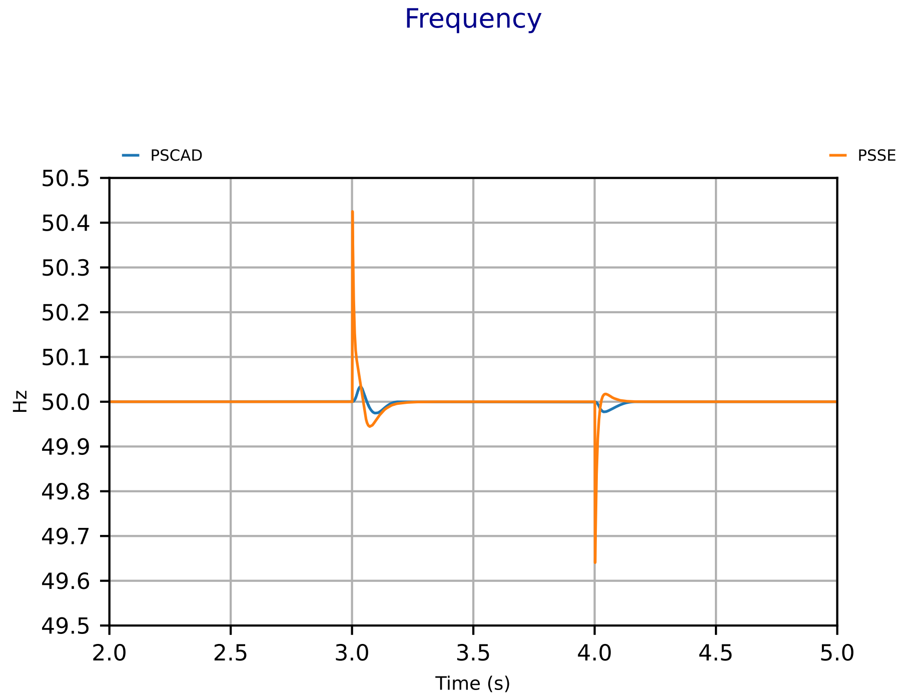
SCR = 10, X/R = 3

Test #6:

~80% Voltage disturbance for 1 sec

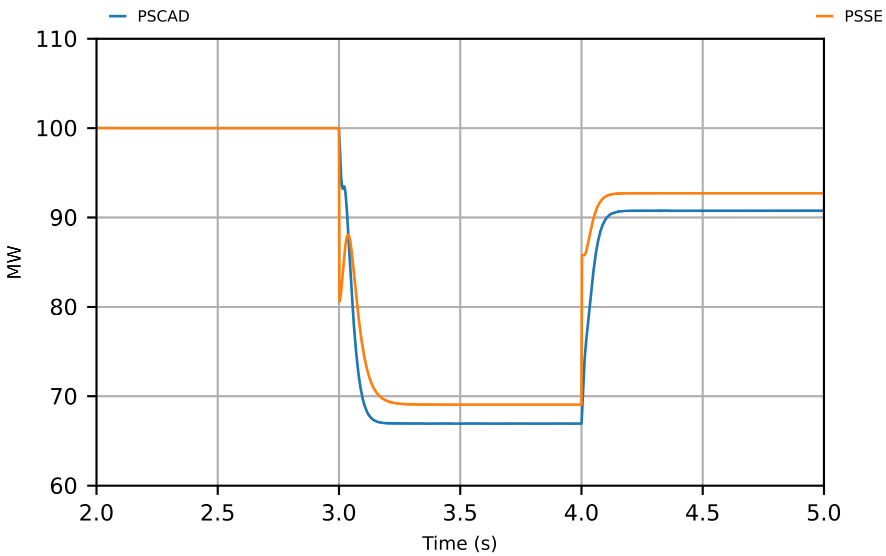
DER_SMIB_SCR_10_XR_3_T6_1



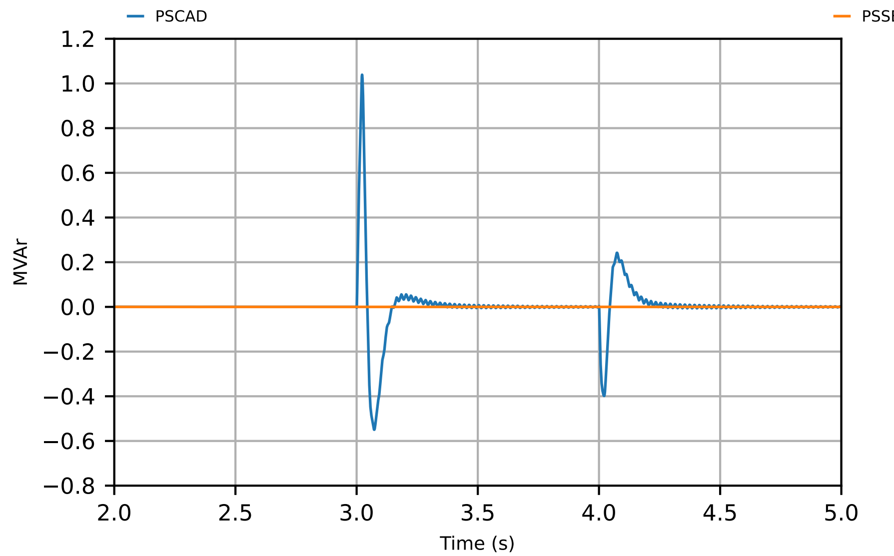


DER_SMIB_SCR_10_XR_3_T6_2

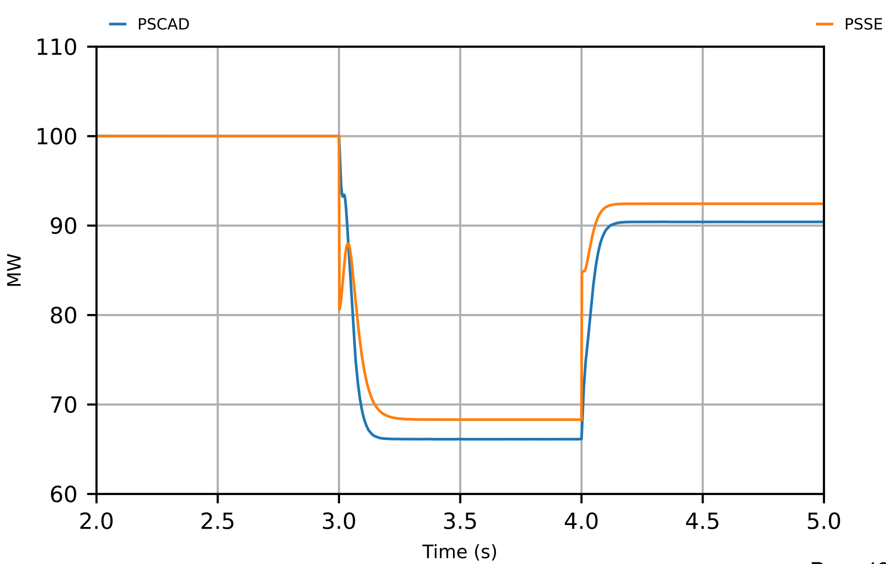
NSW DER Active Power



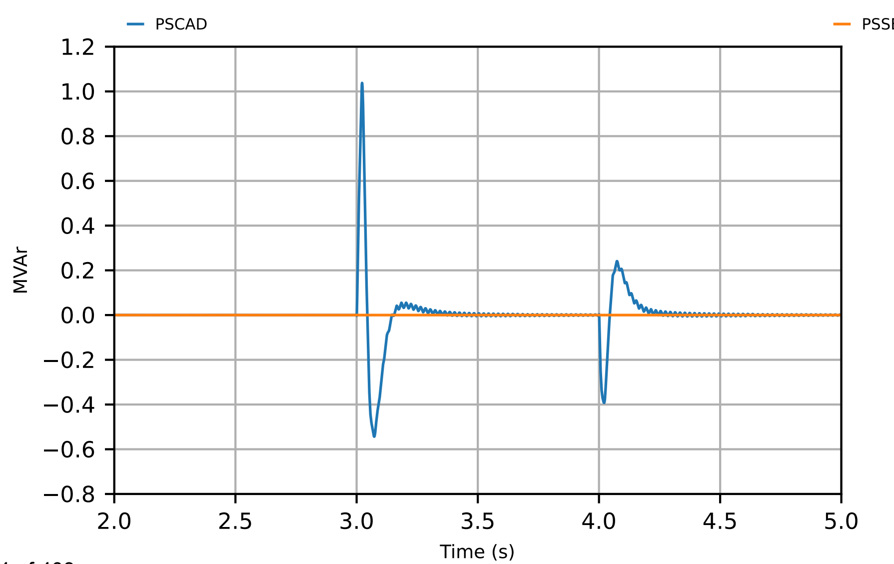
NSW DER Reactive Power



VIC DER Active Power

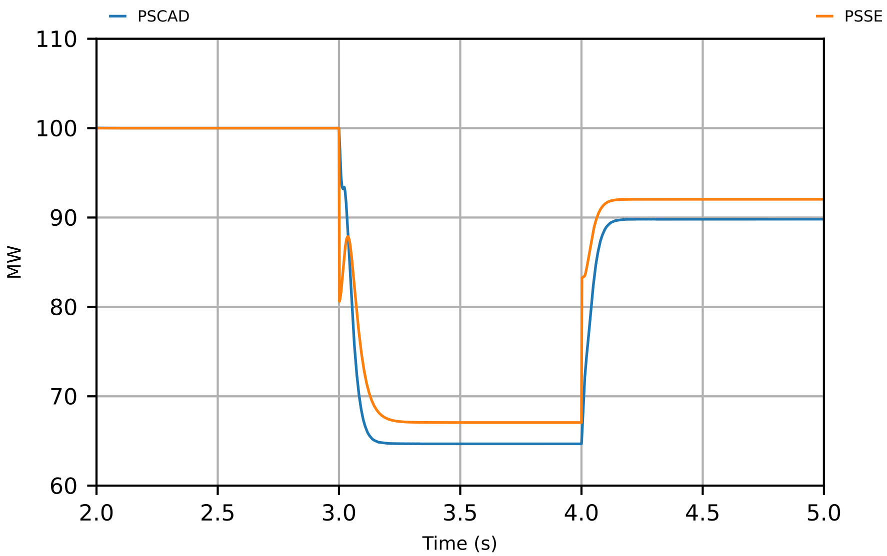


VIC DER Reactive Power

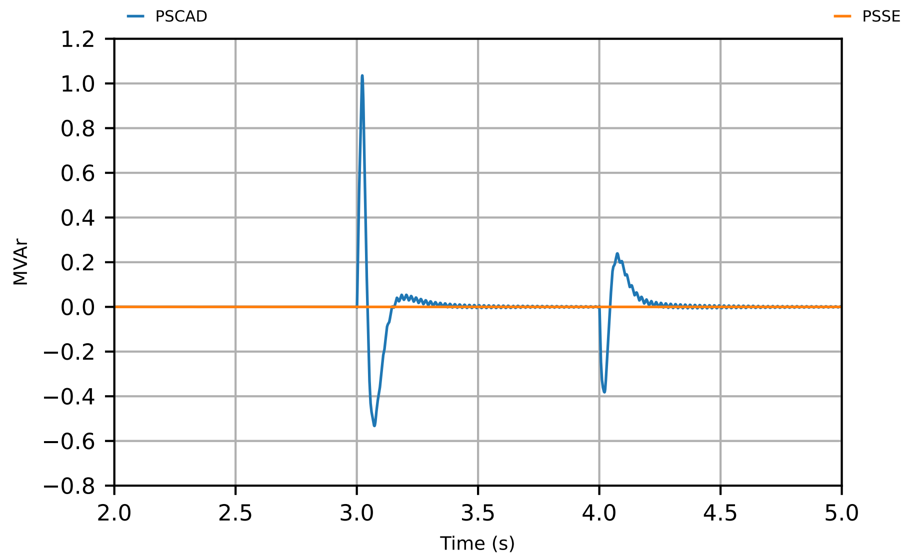


DER_SMIB_SCR_10_XR_3_T6_3

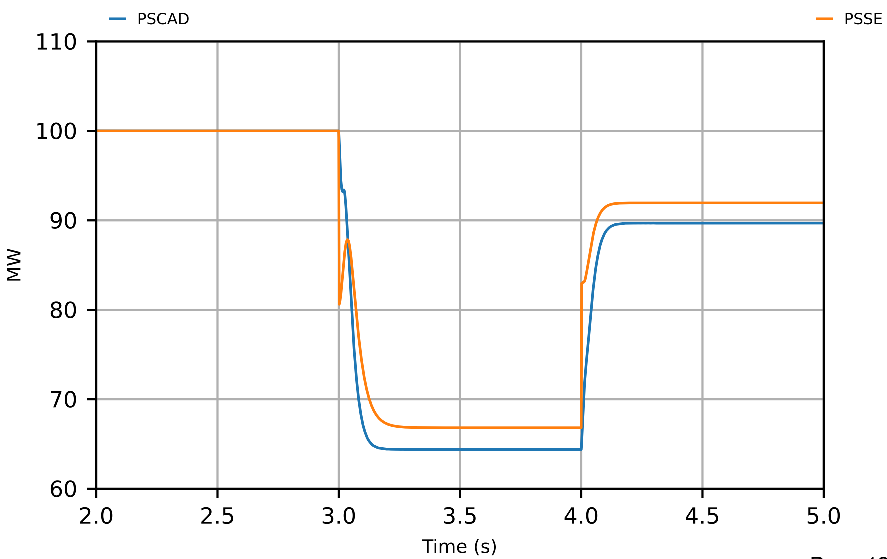
QLD DER Active Power



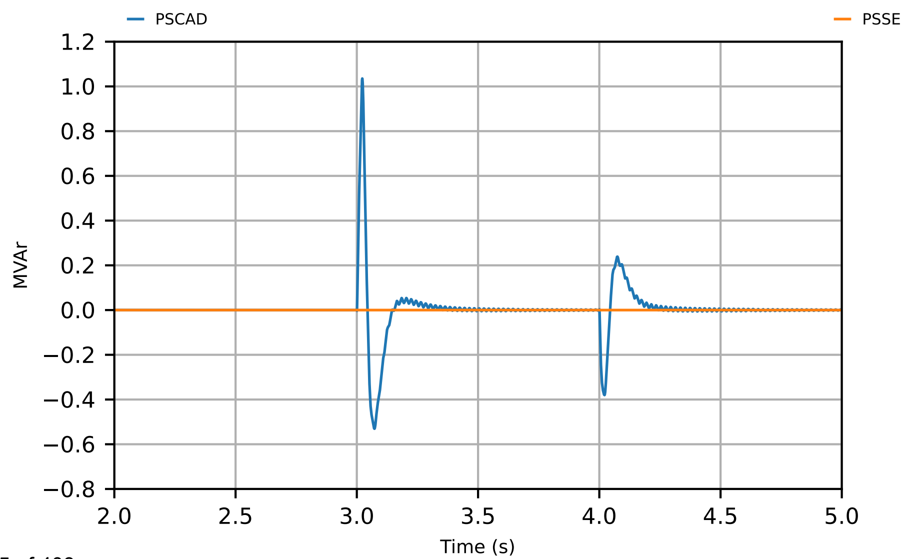
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



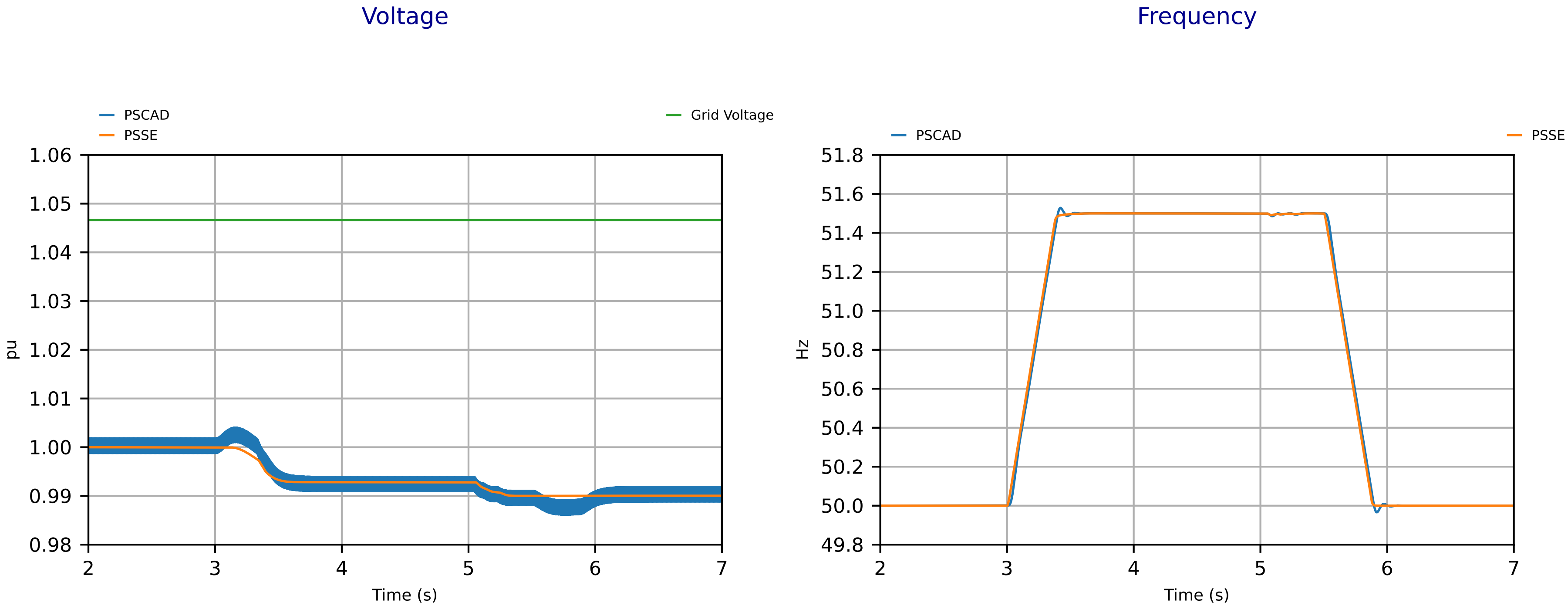
DER SMIB

SCR = 10, X/R = 3

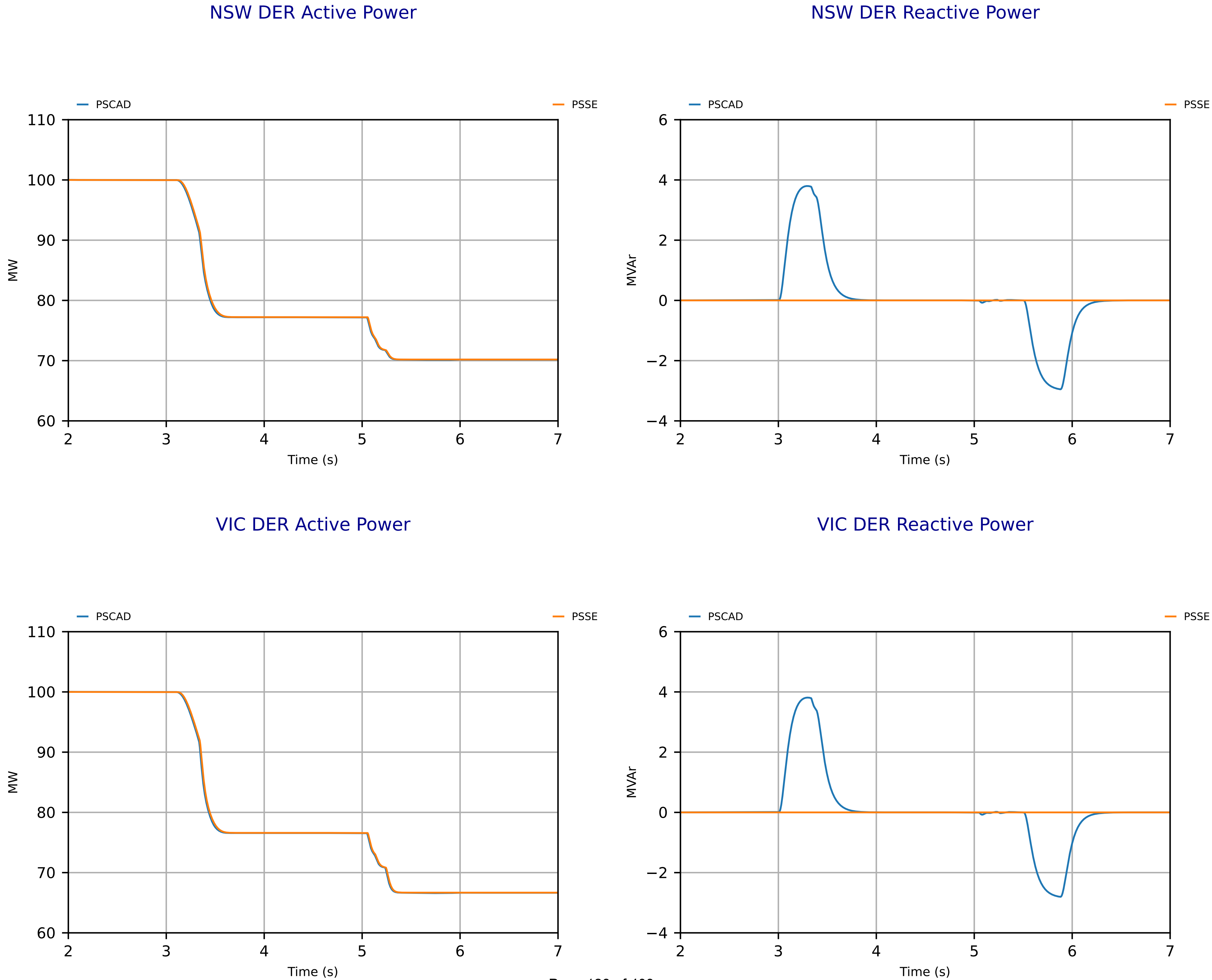
Test #7:

51.5 Hz frequency step for 2.5 sec (4 Hz/s)

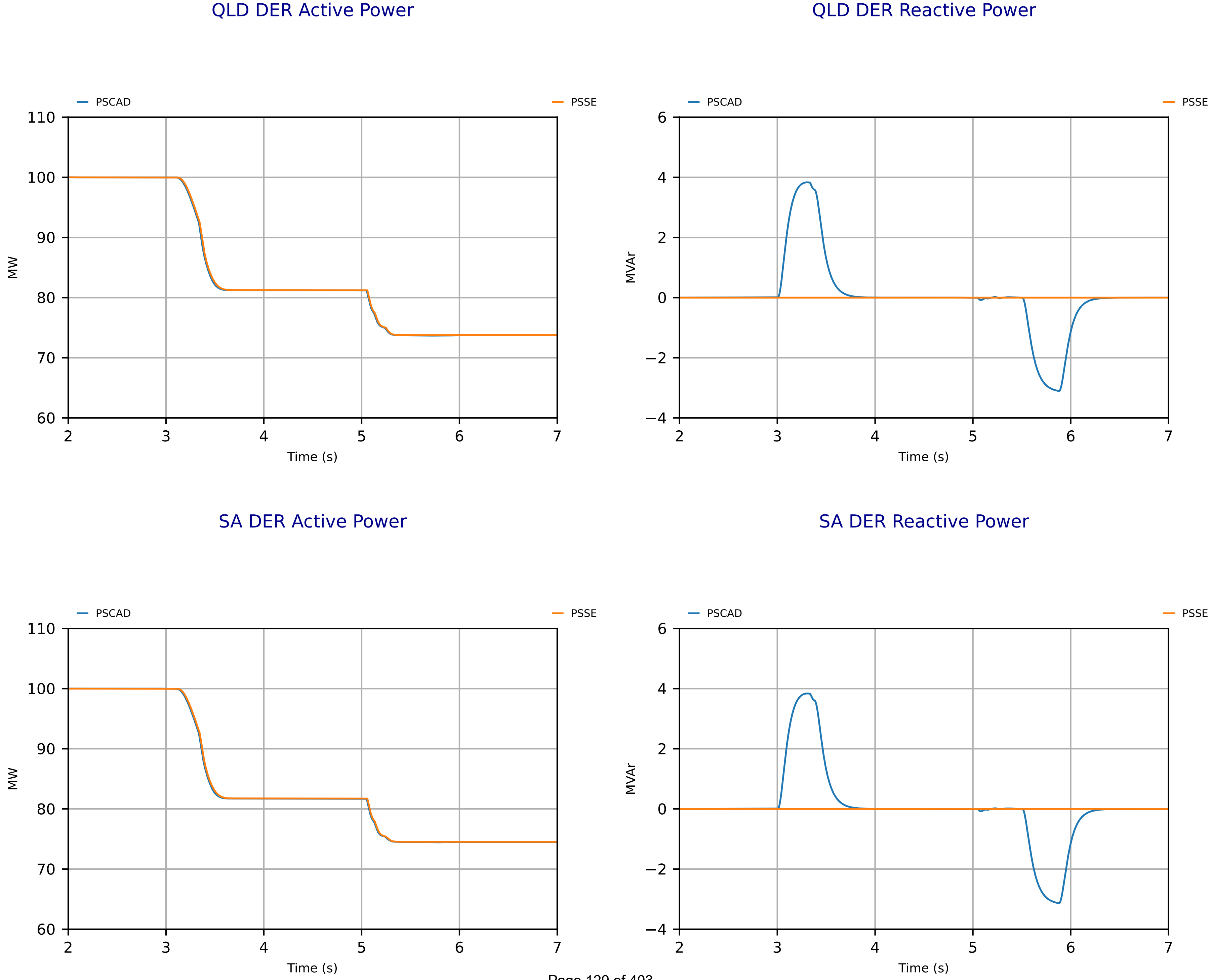
DER_SMIB_SCR_10_XR_3_T7_1



DER_SMIB_SCR_10_XR_3_T7_2



DER_SMIB_SCR_10_XR_3_T7_3



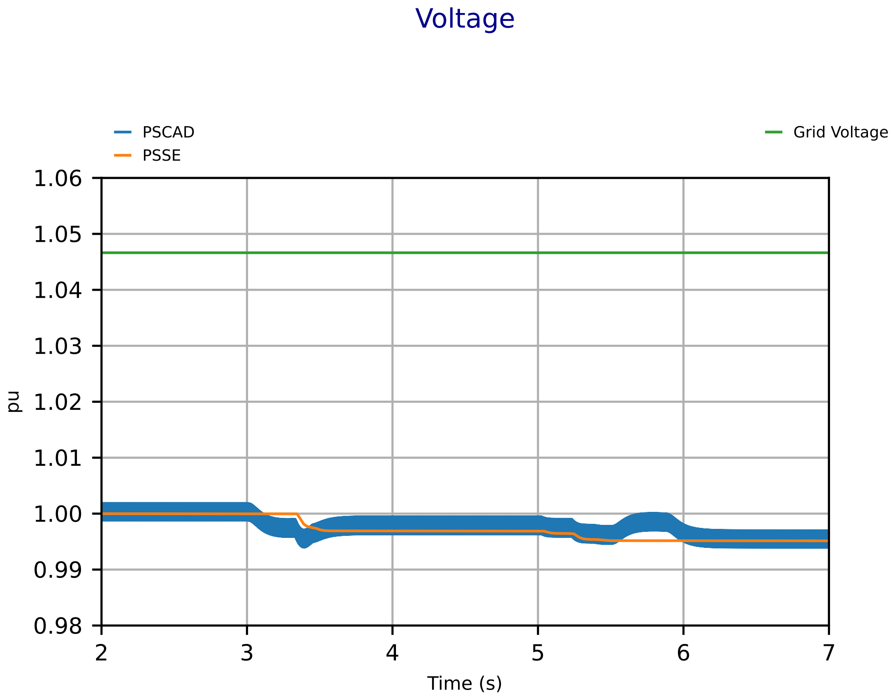
DER SMIB

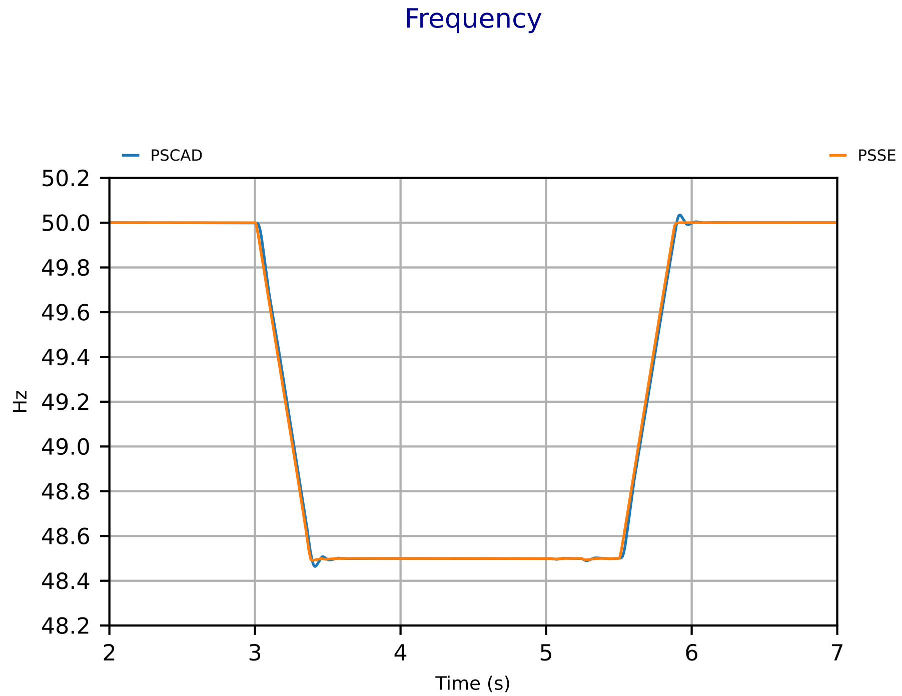
SCR = 10, X/R = 3

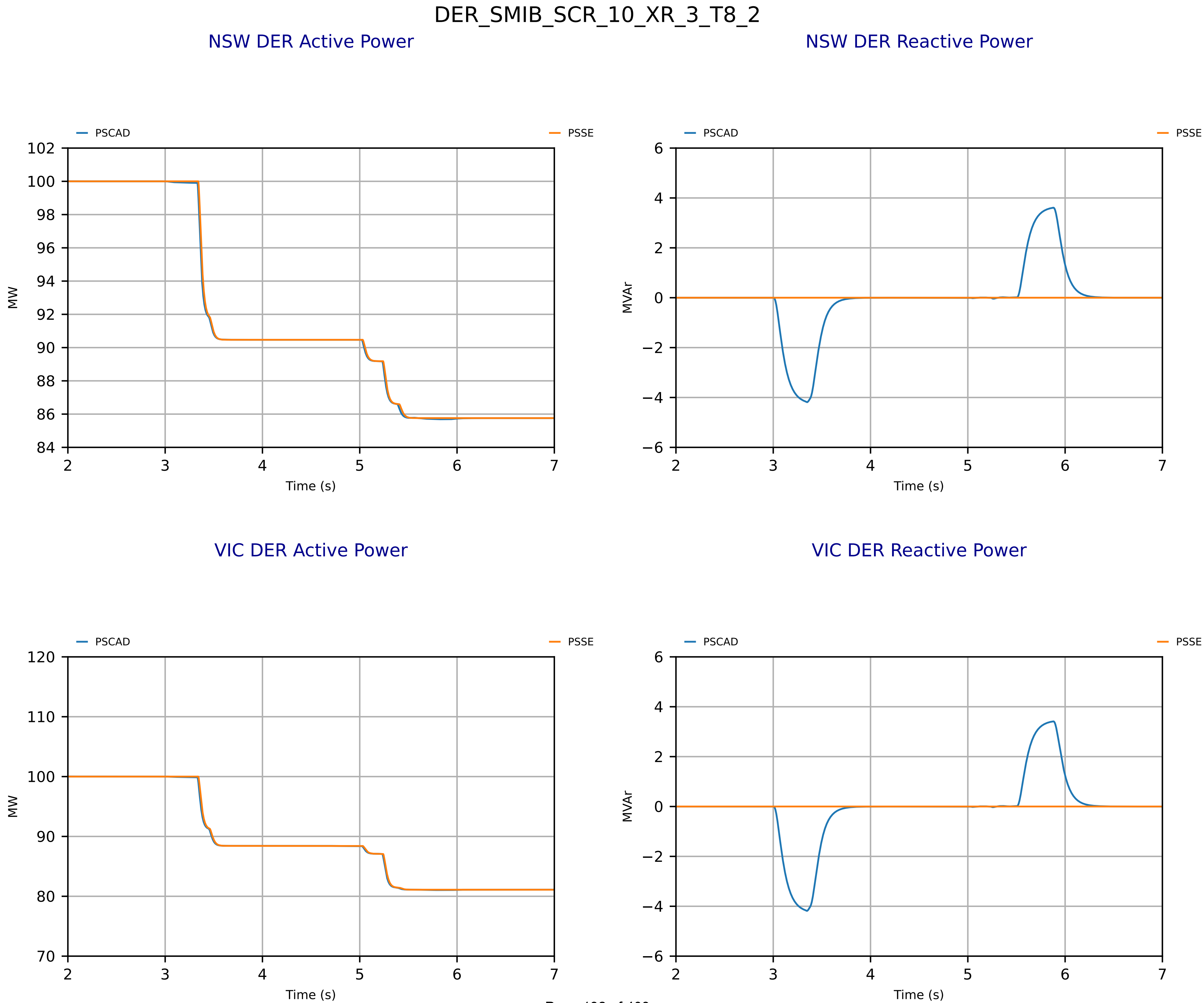
Test #8:

48.5 Hz frequency step for 2.5 sec (4 Hz/s)

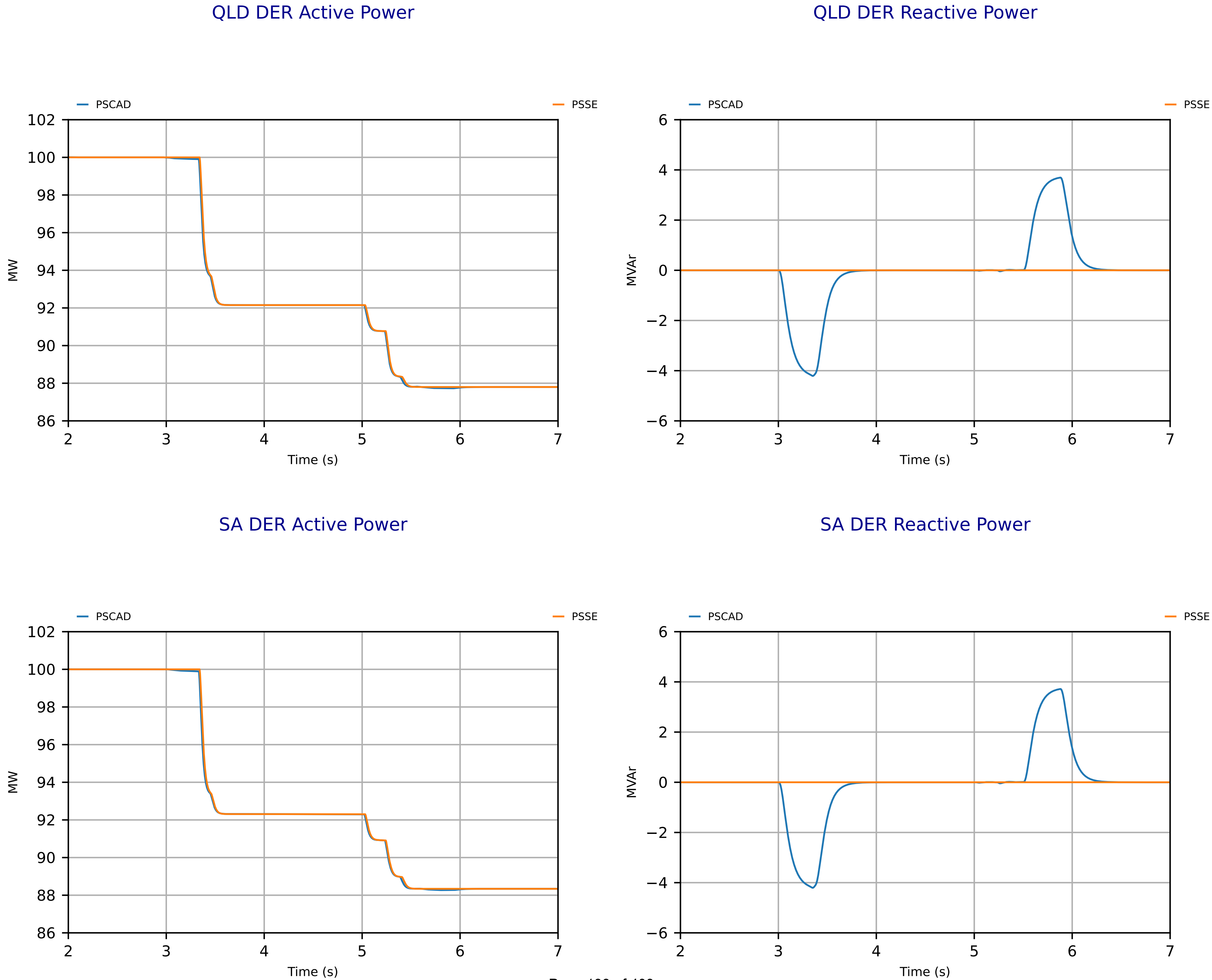
DER_SMIB_SCR_10_XR_3_T8_1






DER_SMIB_SCR_10_XR_3_T8_2
NSW DER Active Power
PSCAD
PSSE
MW
Time (s)
NSW DER Reactive Power
MVAr
VIC DER Active Power
VIC DER Reactive Power

DER_SMIB_SCR_10_XR_3_T8_3



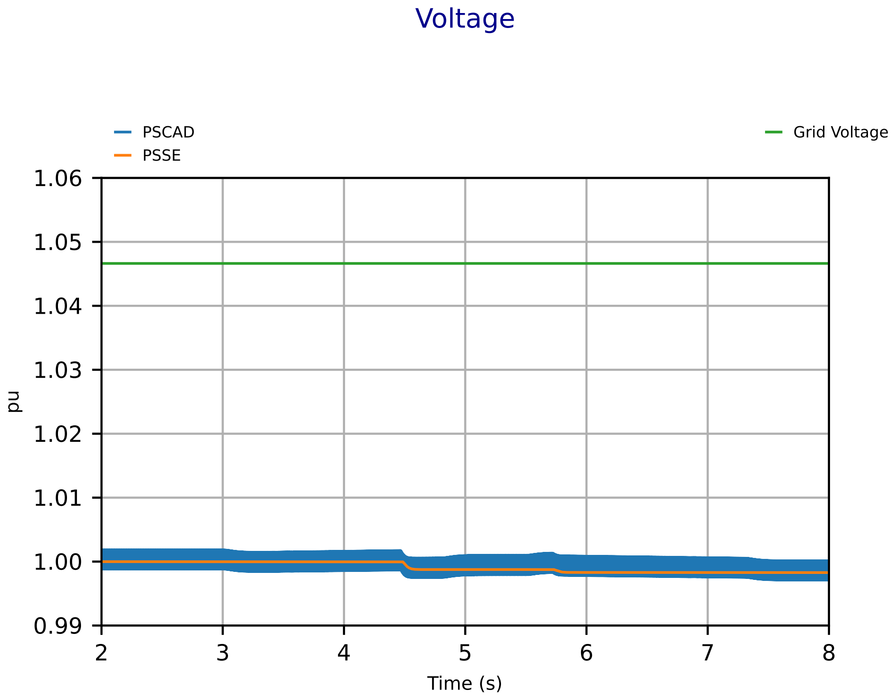
DER SMIB

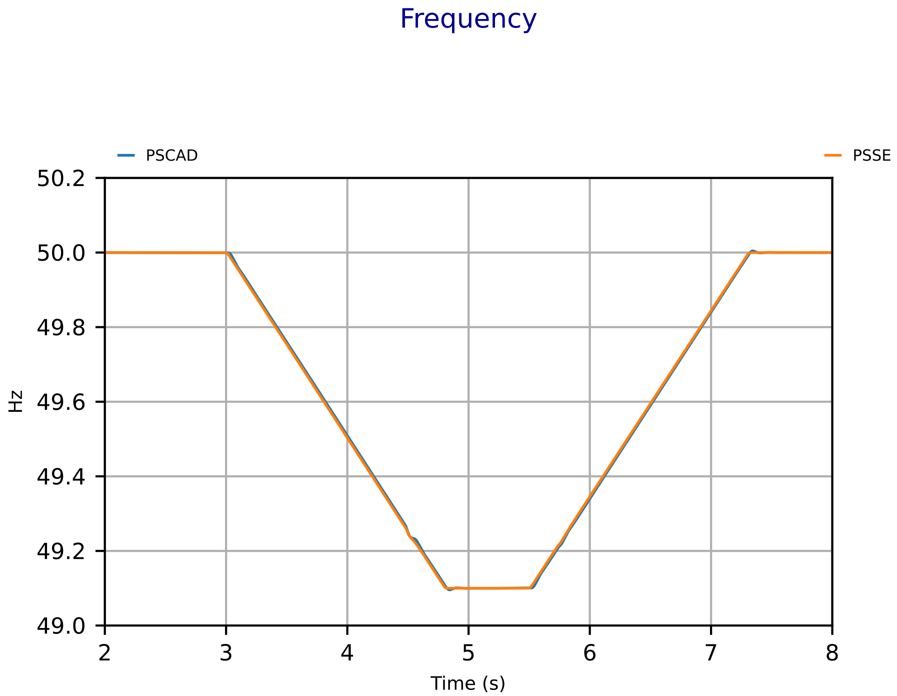
SCR = 10, X/R = 3

Test #9:

49.1 Hz slow frequency ramp (0.5 Hz/s)

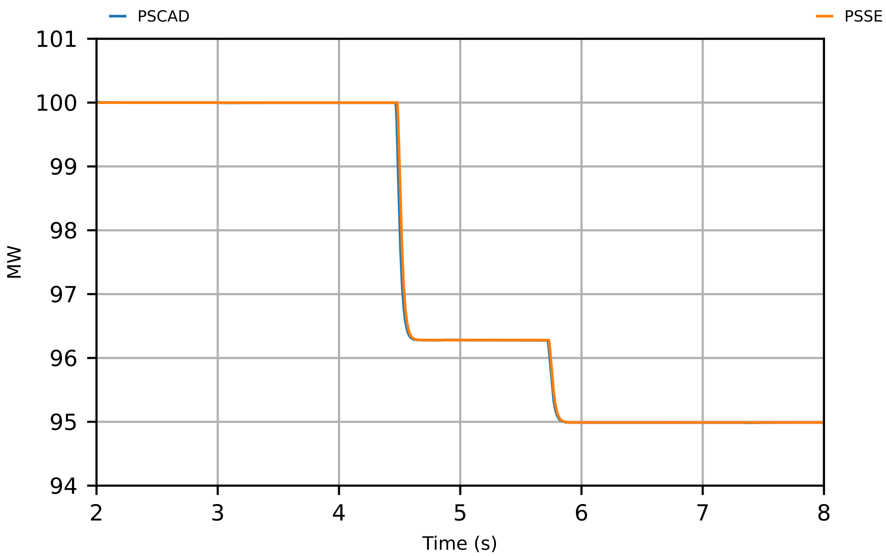
DER_SMIB_SCR_10_XR_3_T9_1



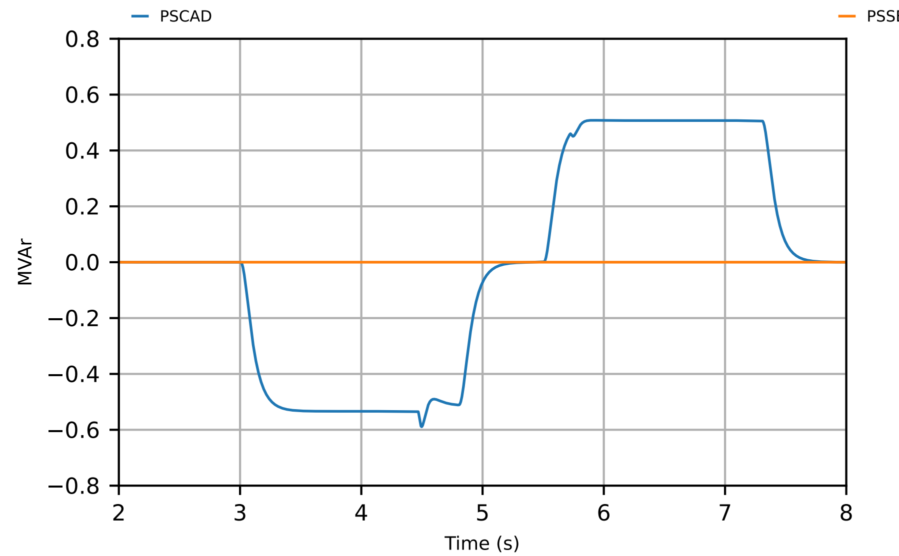


DER_SMIB_SCR_10_XR_3_T9_2

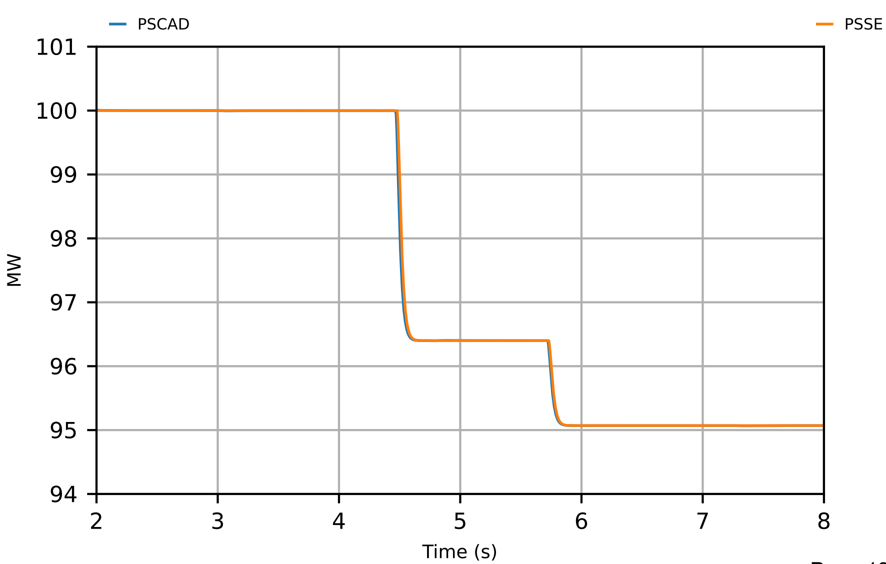
NSW DER Active Power



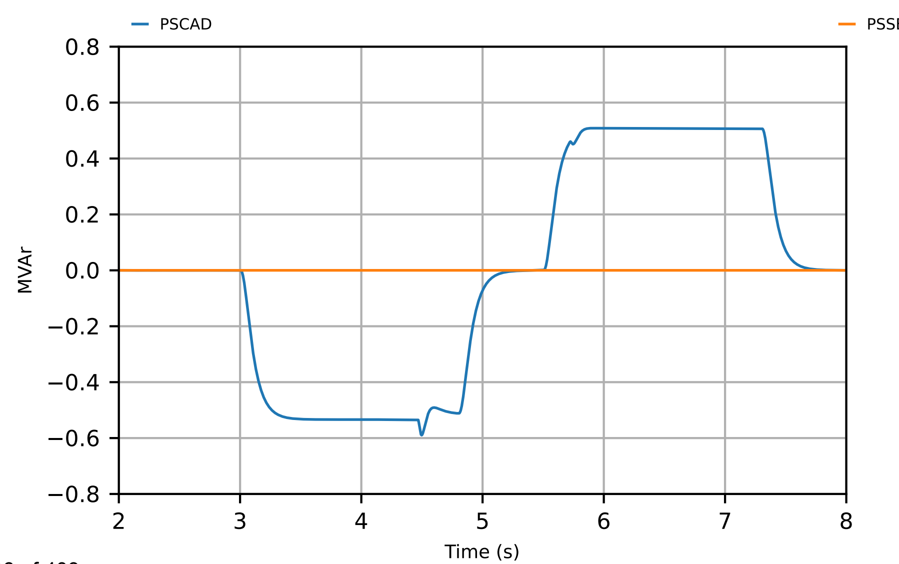
NSW DER Reactive Power



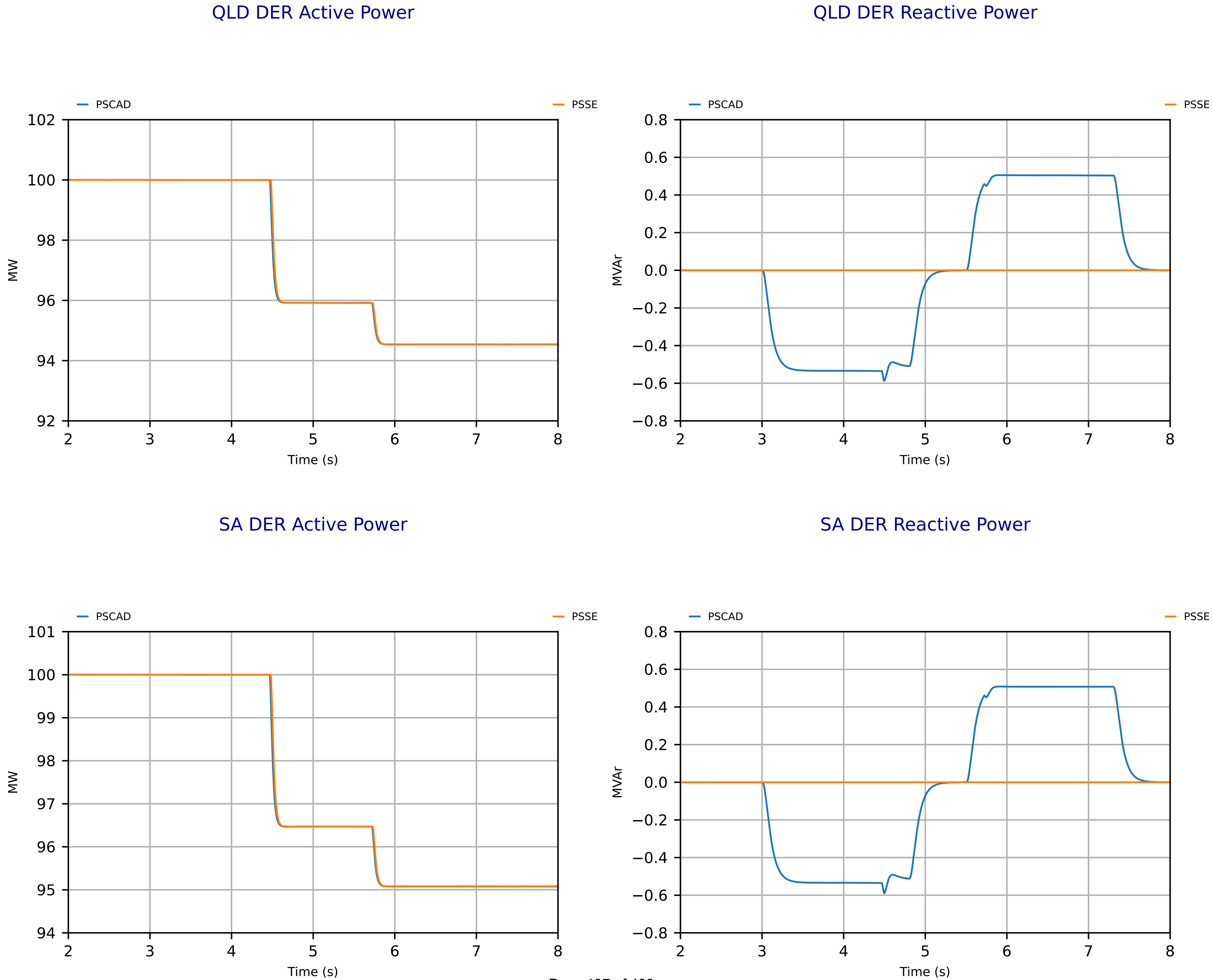
VIC DER Active Power



VIC DER Reactive Power



DER_SMIB_SCR_10_XR_3_T9_3



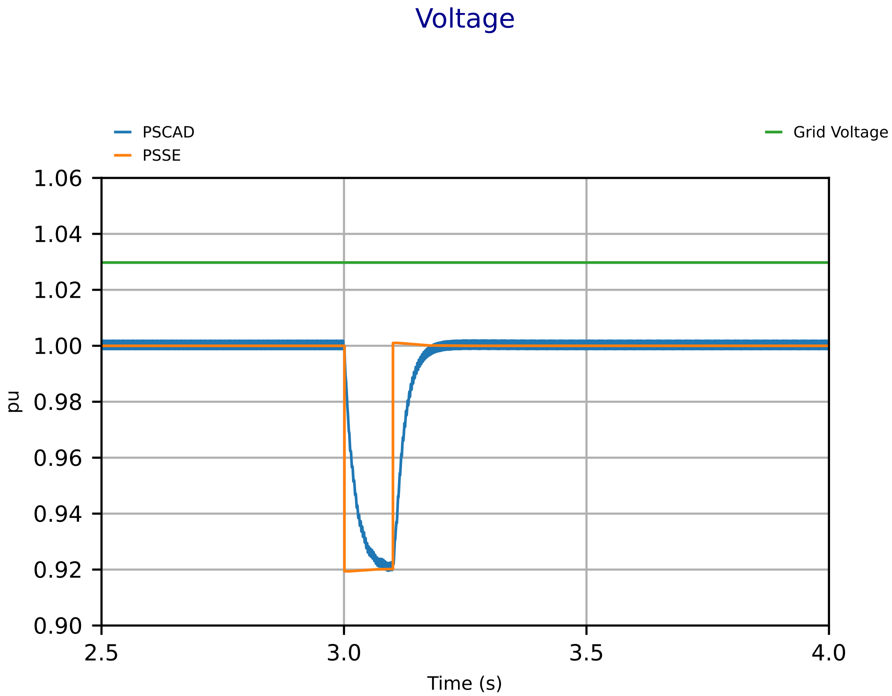
DER SMIB

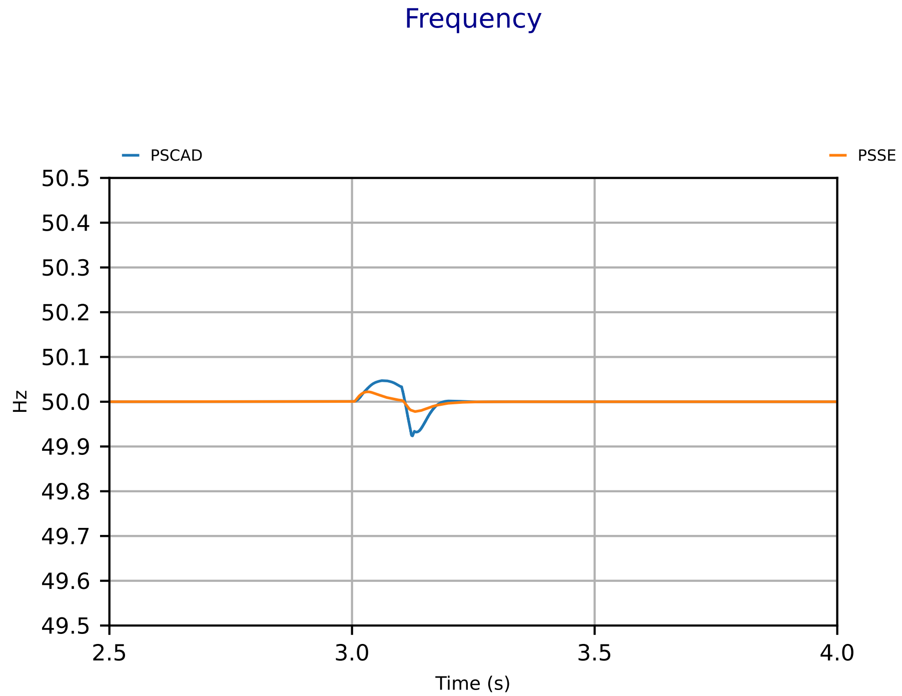
SCR = 10, X/R = 14

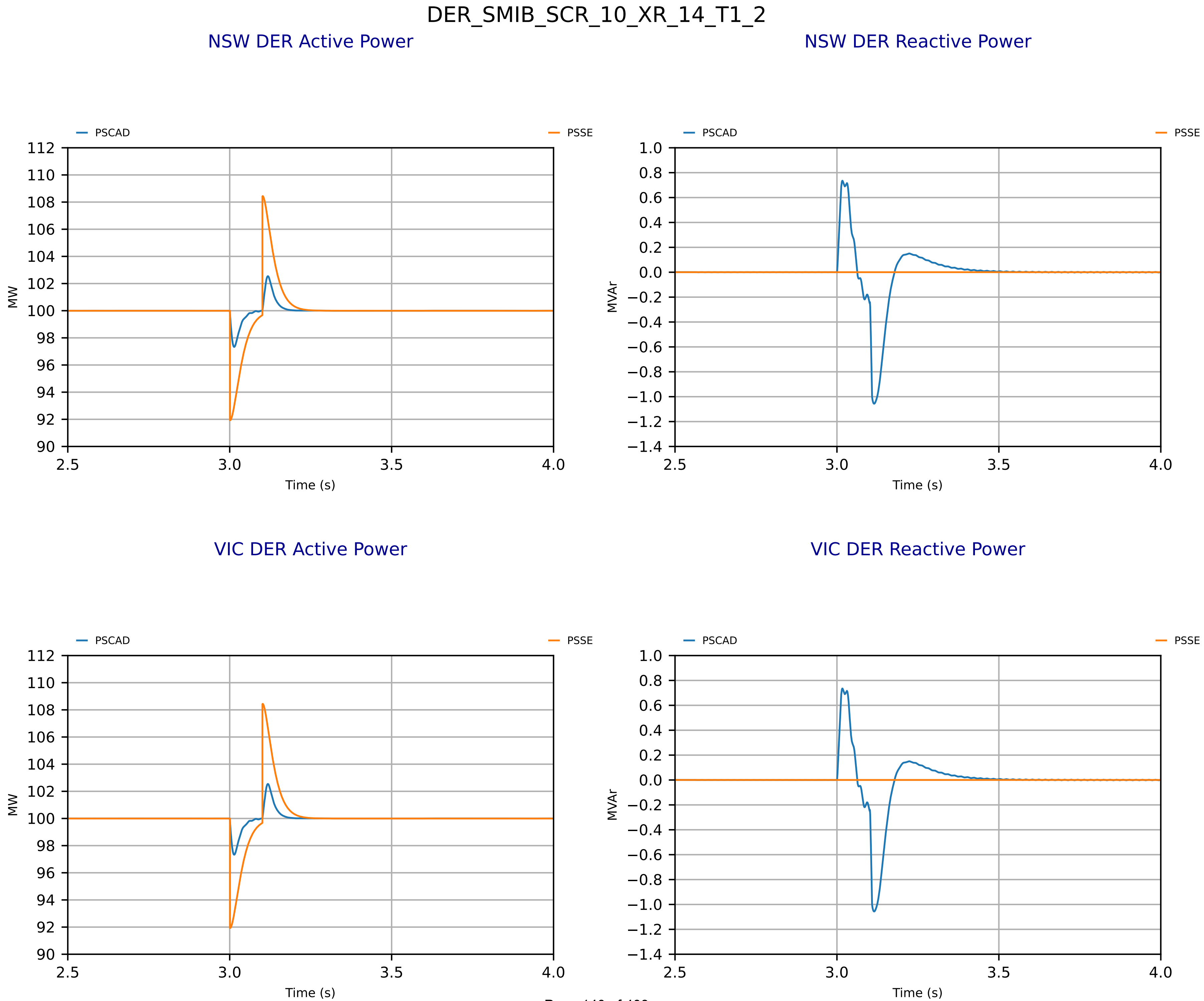
Test #1:

LG fault for 100 ms

DER_SMIB_SCR_10_XR_14_T1_1



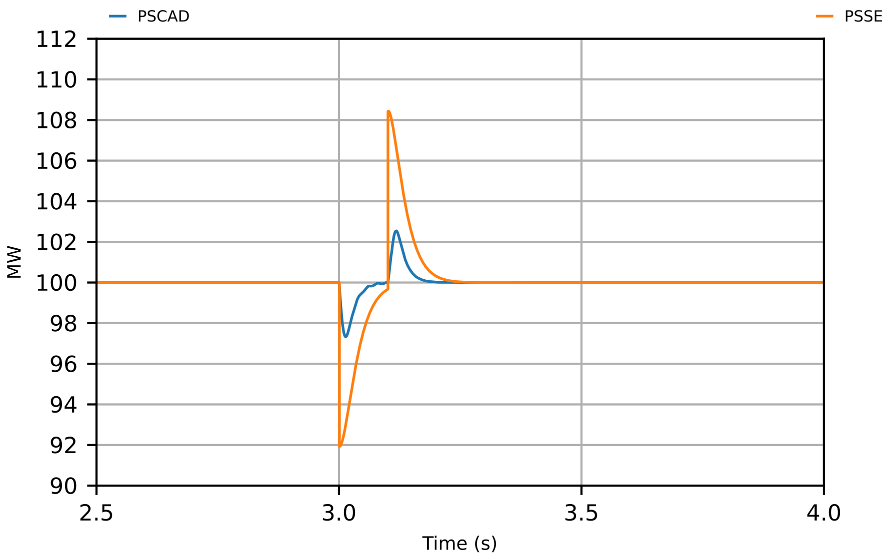




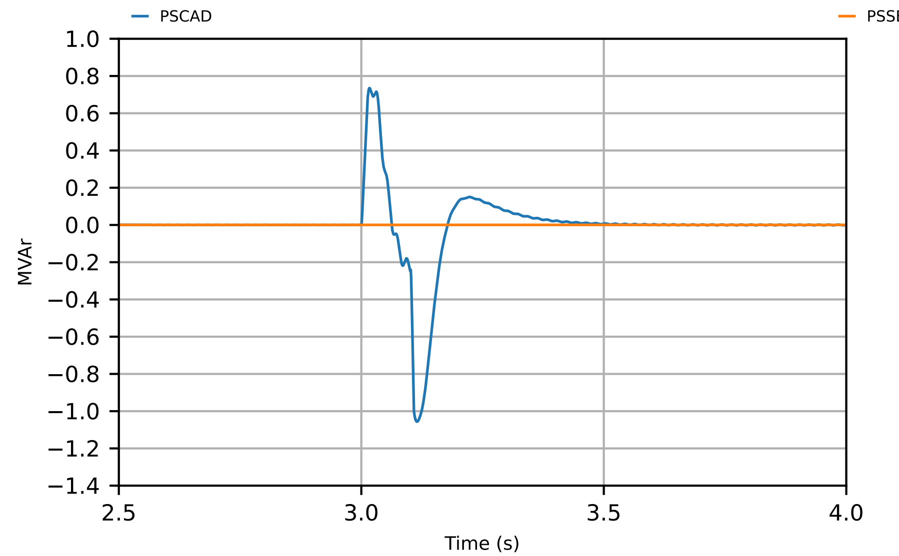
DER_SMIB_SCR_10_XR_14_T1_2
NSW DER Active Power
NSW DER Reactive Power
PSCAD
PSSE
MW
MVAr
Time (s)
VIC DER Active Power
VIC DER Reactive Power

DER_SMIB_SCR_10_XR_14_T1_3

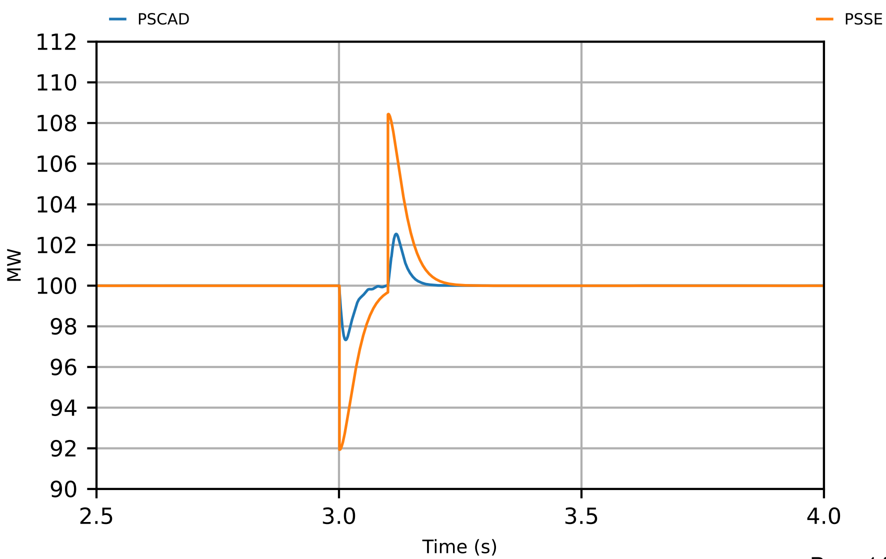
QLD DER Active Power



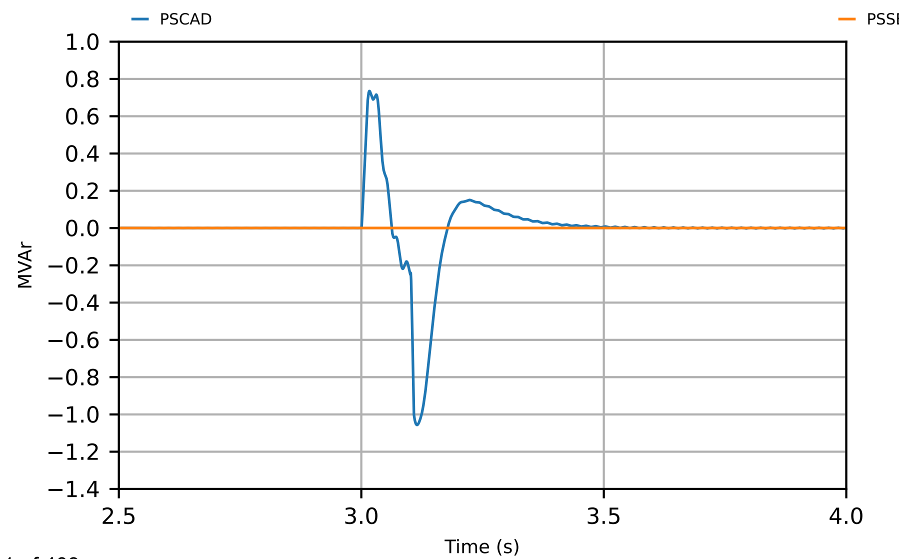
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



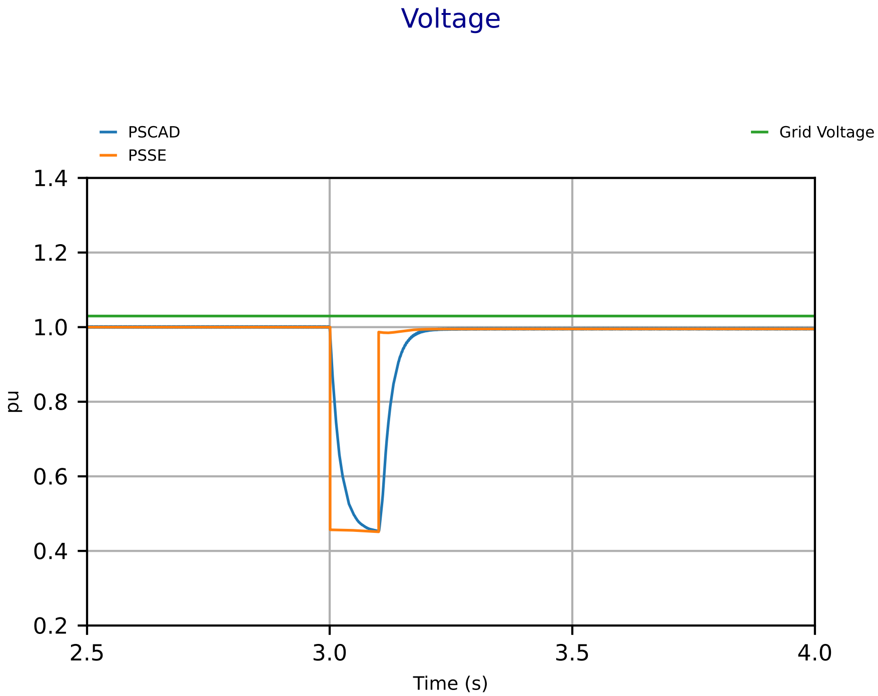
DER SMIB

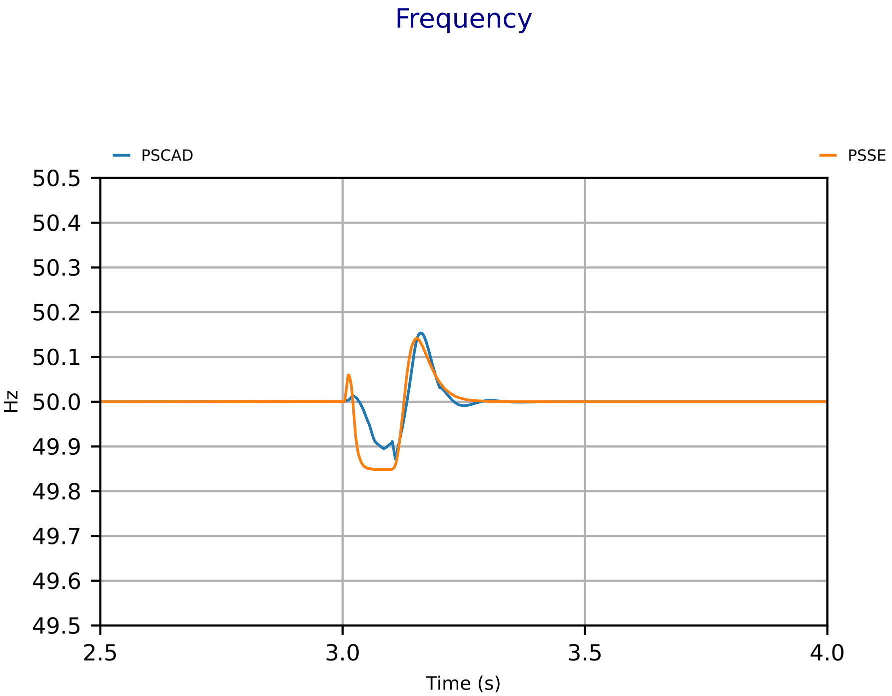
SCR = 10, X/R = 14

Test #2:

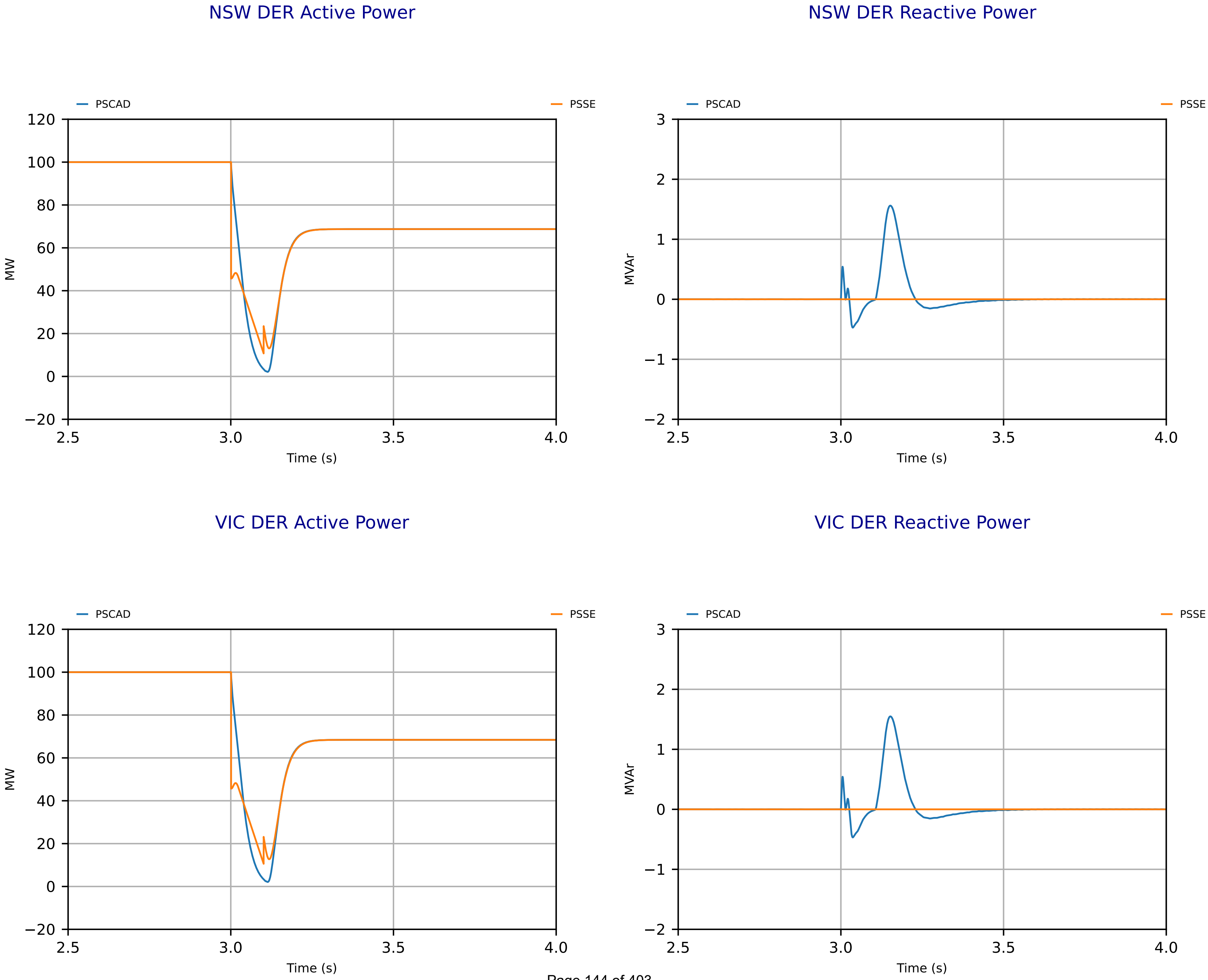
LLG fault for 100 ms

DER_SMIB_SCR_10_XR_14_T2_1

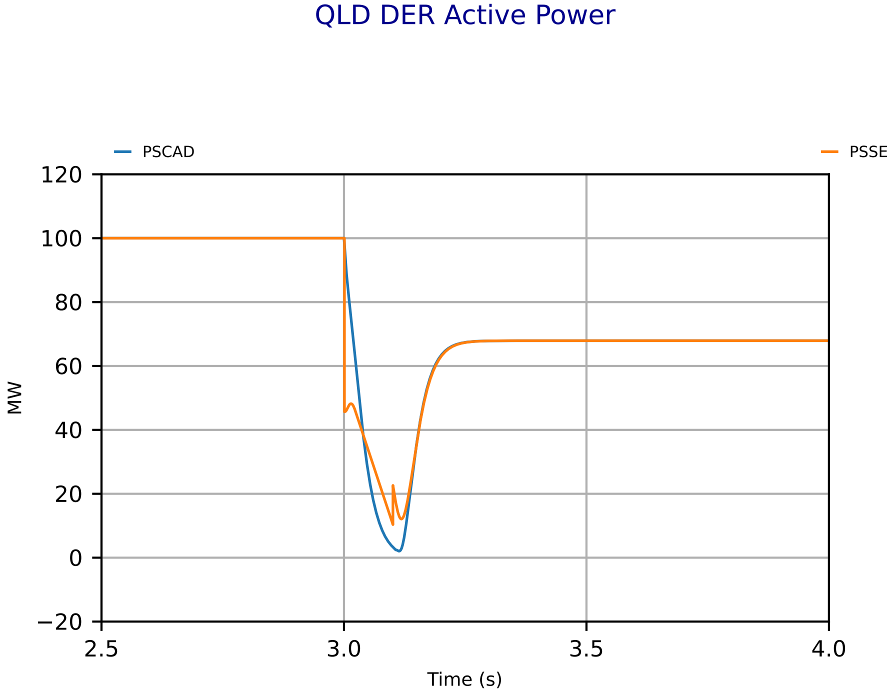


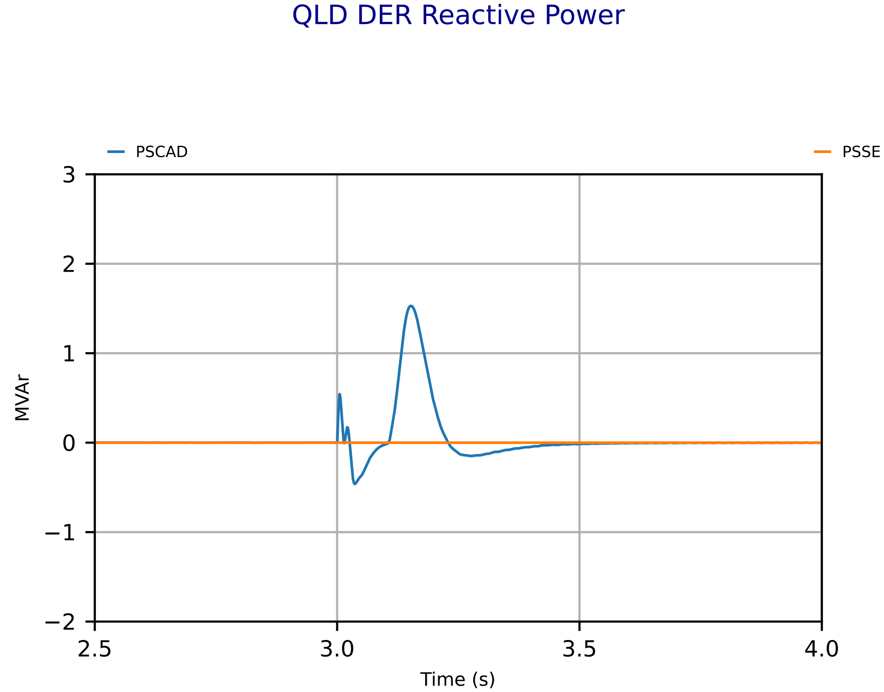


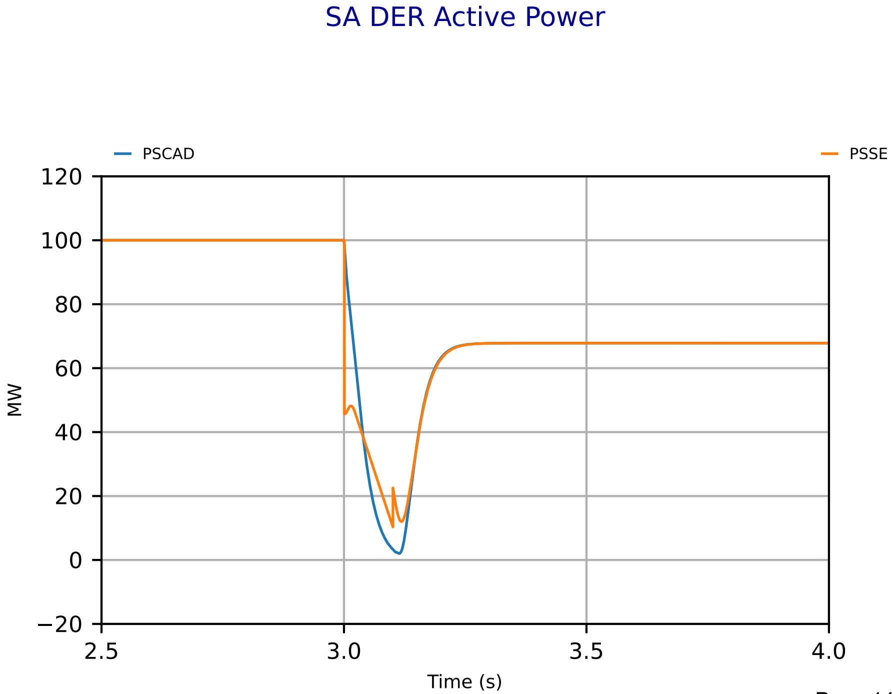
DER_SMIB_SCR_10_XR_14_T2_2

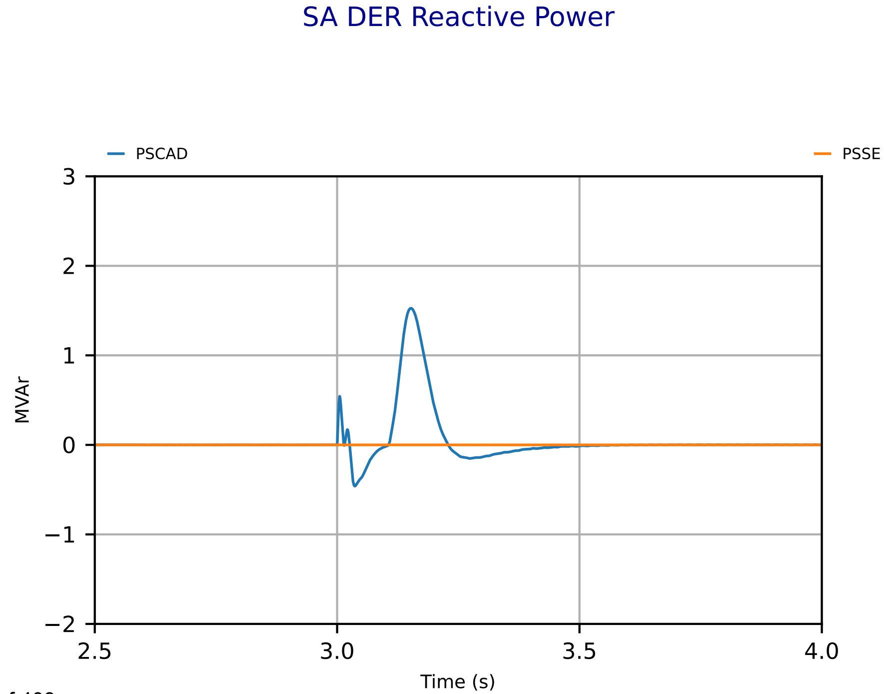


DER_SMIB_SCR_10_XR_14_T2_3









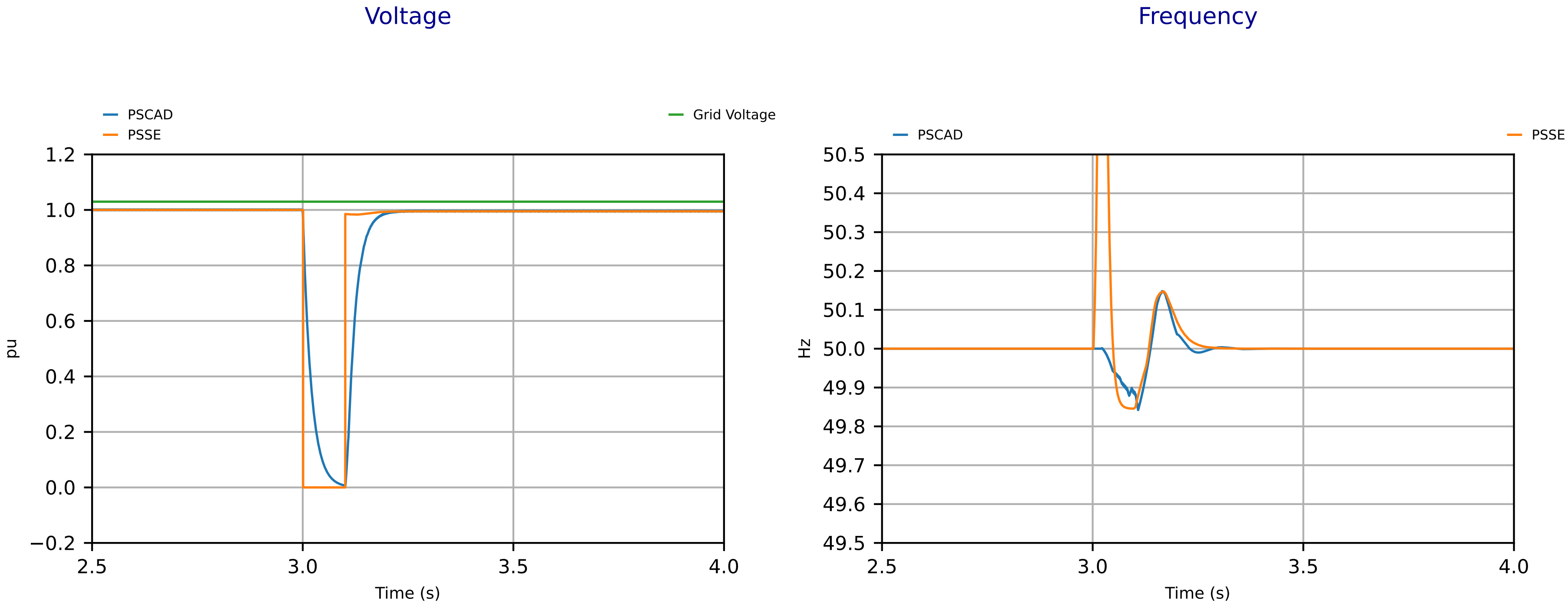
DER SMIB

SCR = 10, X/R = 14

Test #3:

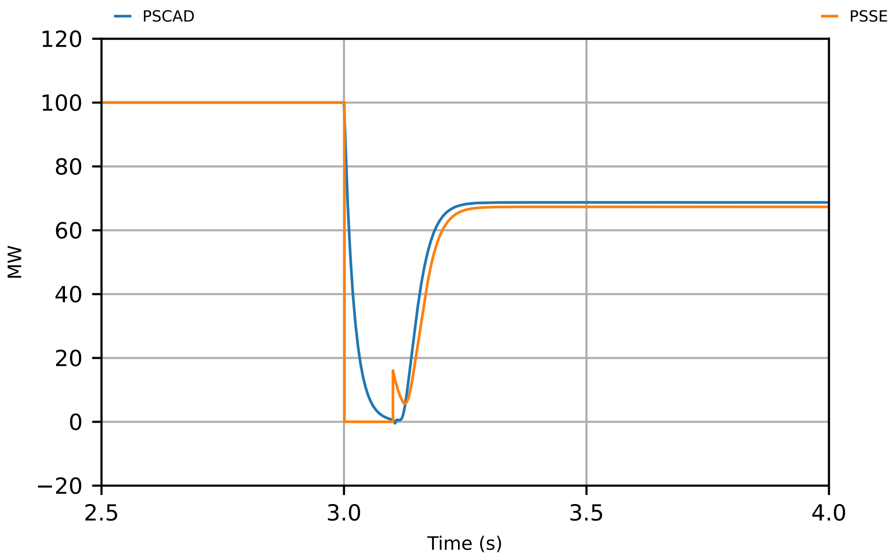
3PH-G fault for 100 ms

DER_SMIB_SCR_10_XR_14_T3_1

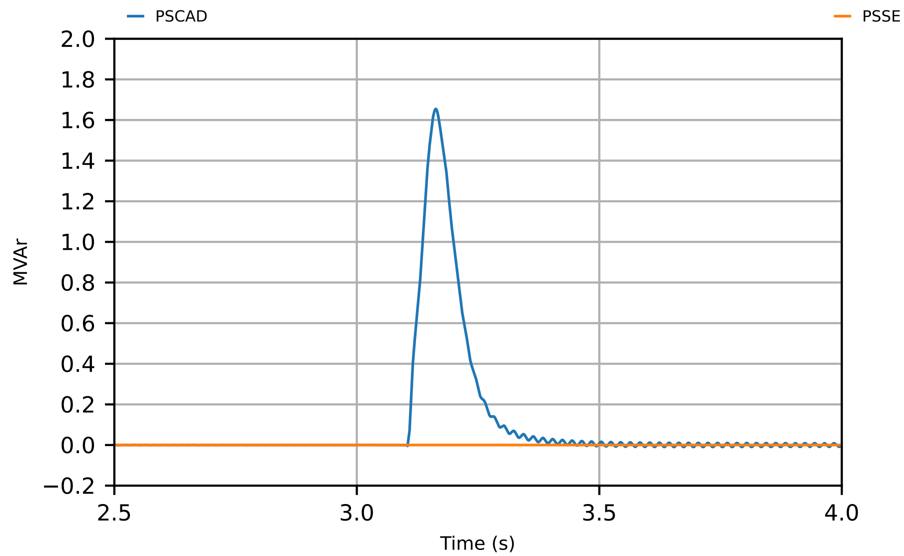


DER_SMIB_SCR_10_XR_14_T3_2

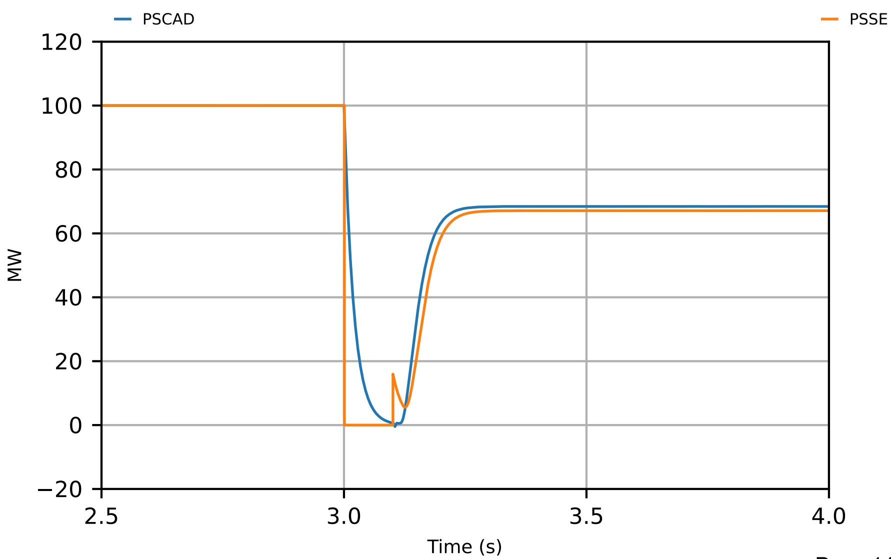
NSW DER Active Power



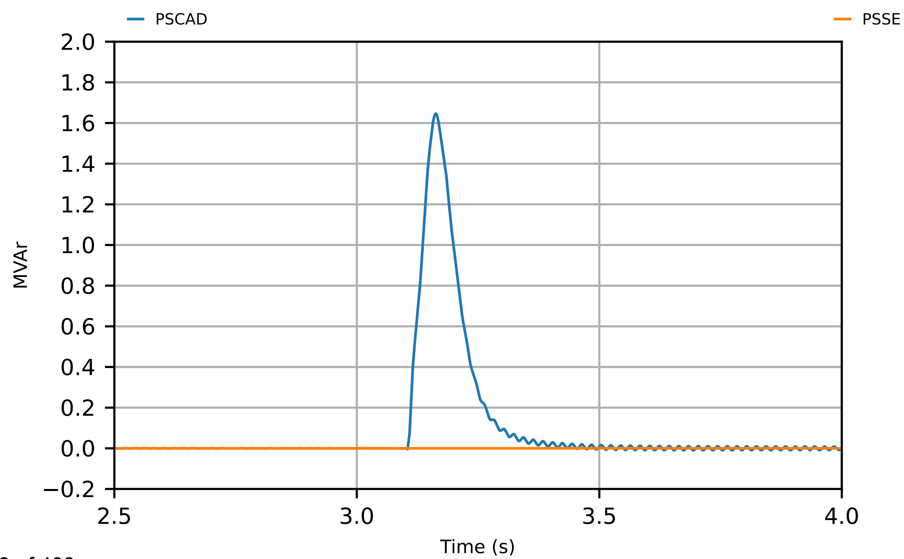
NSW DER Reactive Power

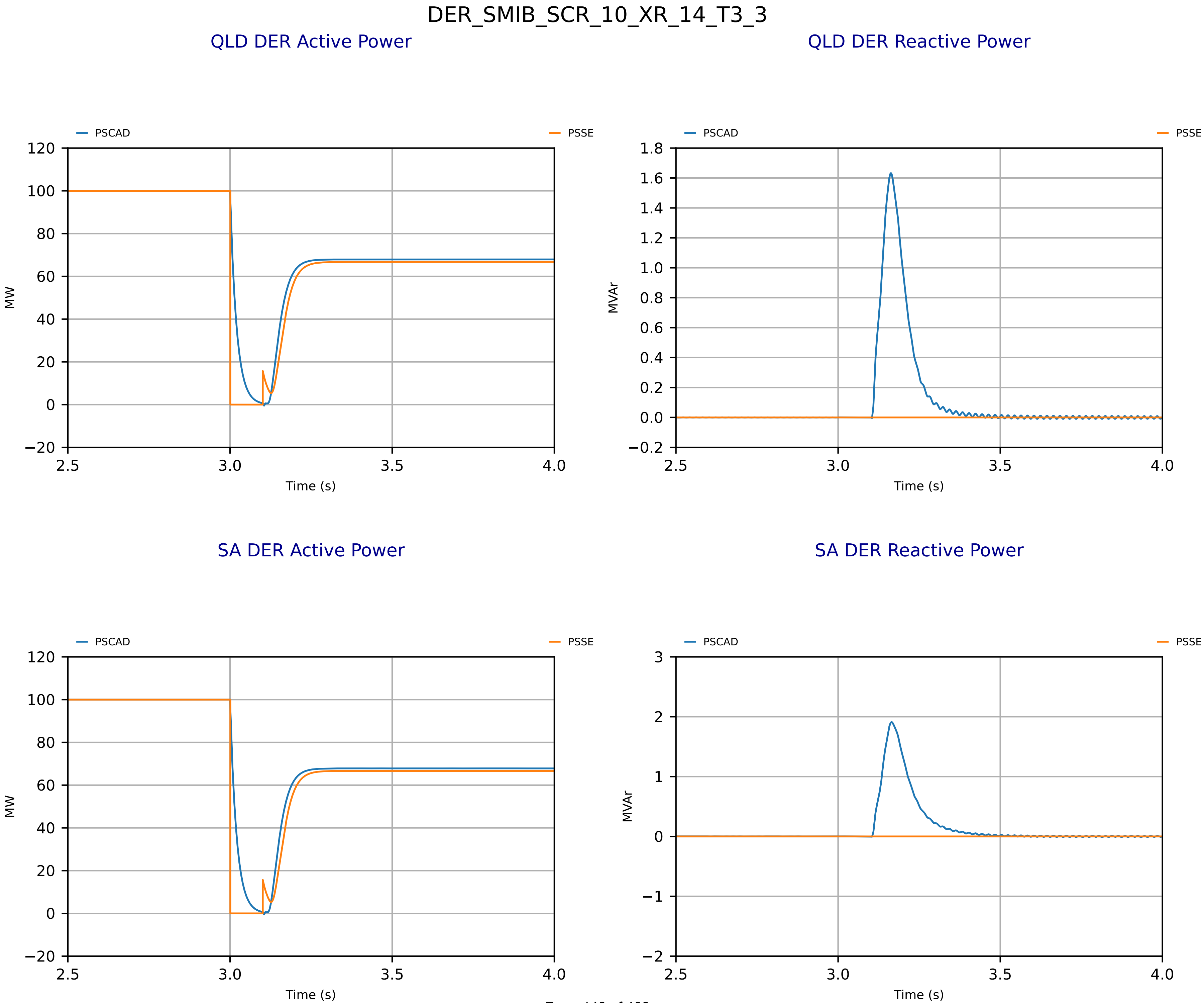


VIC DER Active Power



VIC DER Reactive Power




DER_SMIB_SCR_10_XR_14_T3_3
QLD DER Active Power
PSCAD
PSSE
MW
Time (s)
QLD DER Reactive Power
PSCAD
PSSE
MVAr
Time (s)
SA DER Active Power
PSCAD
PSSE
MW
Time (s)
SA DER Reactive Power
PSCAD
PSSE
MVAr
Time (s)

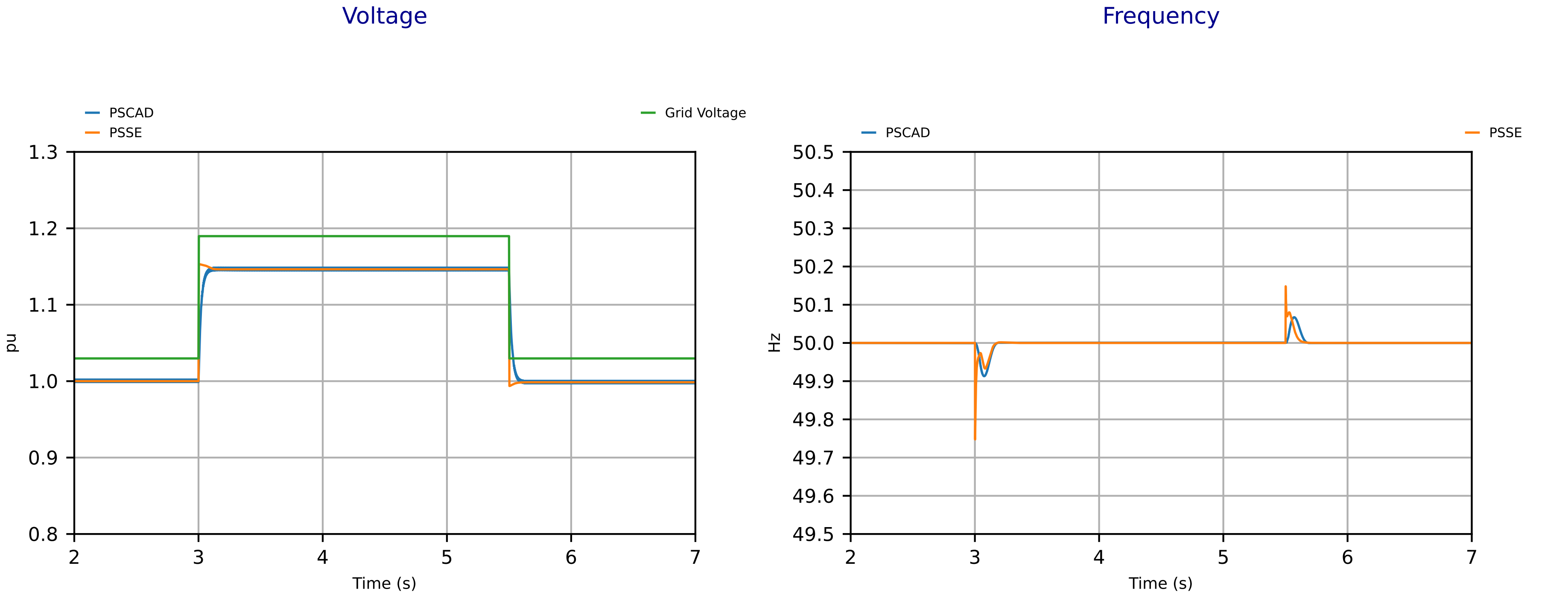
DER SMIB

SCR = 10, X/R = 14

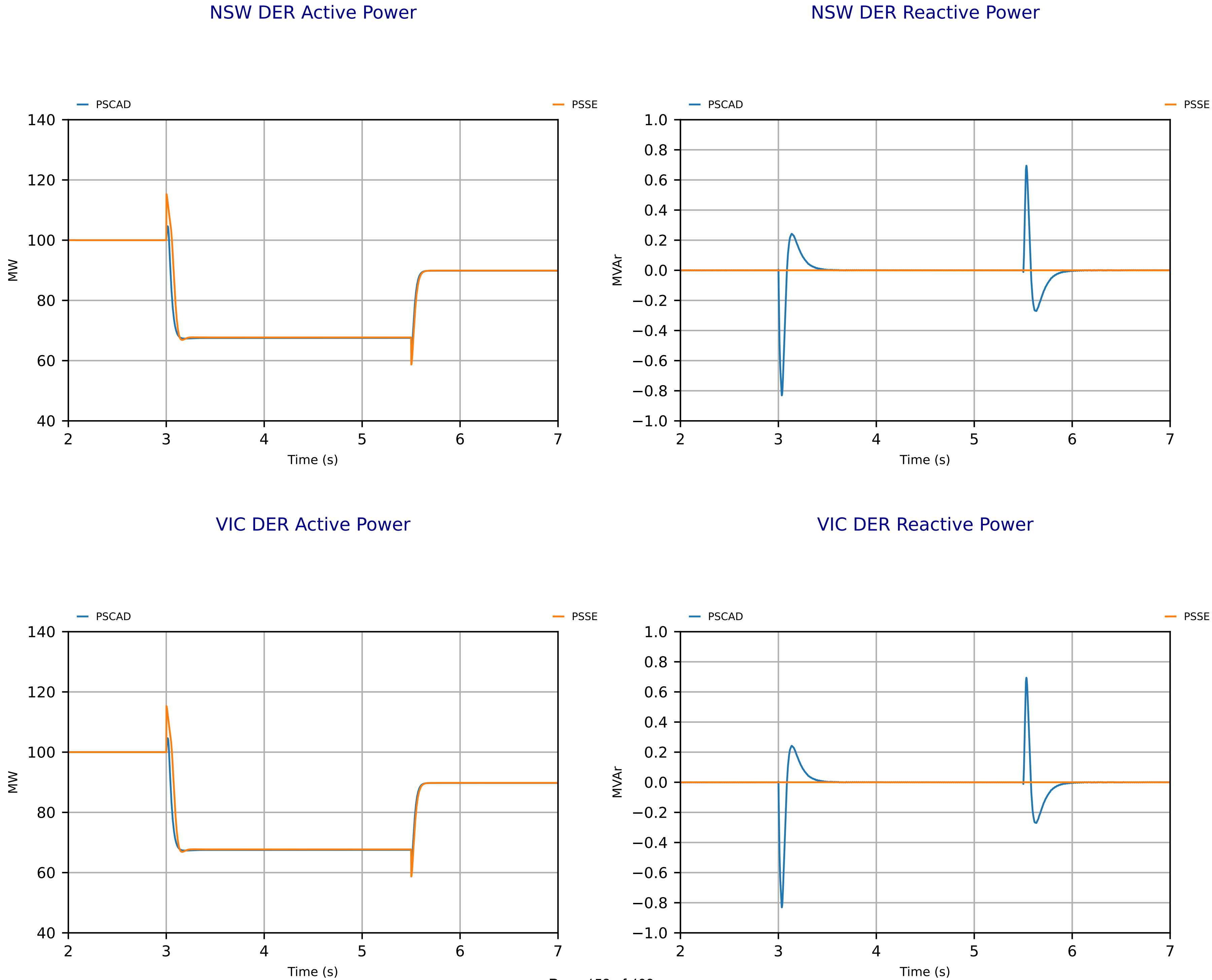
Test #4:

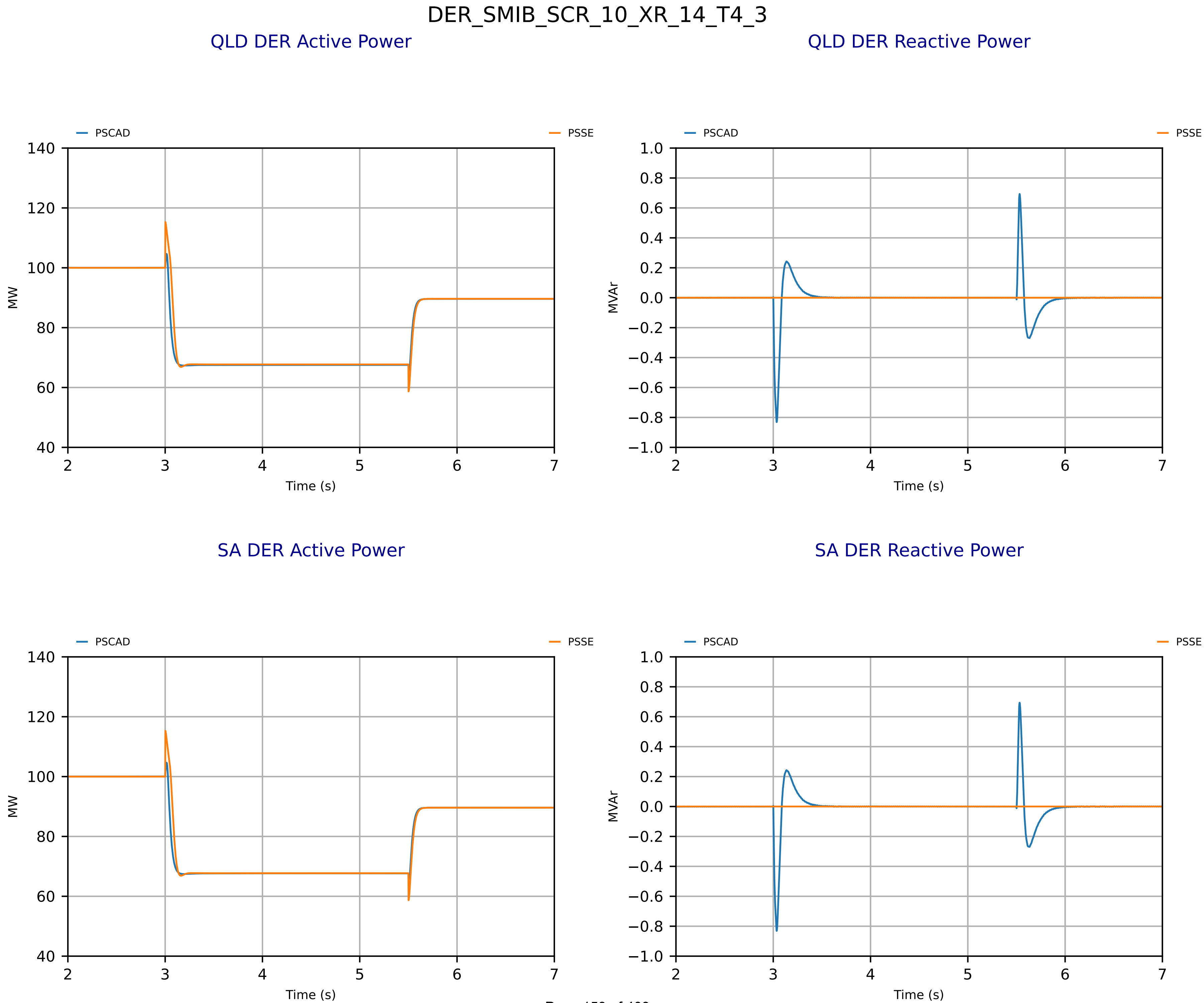
~115% Voltage disturbance for 2.5 s

DER_SMIB_SCR_10_XR_14_T4_1



DER_SMIB_SCR_10_XR_14_T4_2





DER_SMIB_SCR_10_XR_14_T4_3
QLD DER Active Power
PSCAD
PSSE
140
120
100
80
60
40
MW
2
3
4
5
6
7
Time (s)
QLD DER Reactive Power
PSCAD
PSSE
1.0
0.8
0.6
0.4
0.2
0.0
−0.2
−0.4
−0.6
−0.8
−1.0
MVAr
Time (s)
SA DER Active Power
PSCAD
PSSE
MW
Time (s)
SA DER Reactive Power
PSCAD
PSSE
MVAr
Time (s)

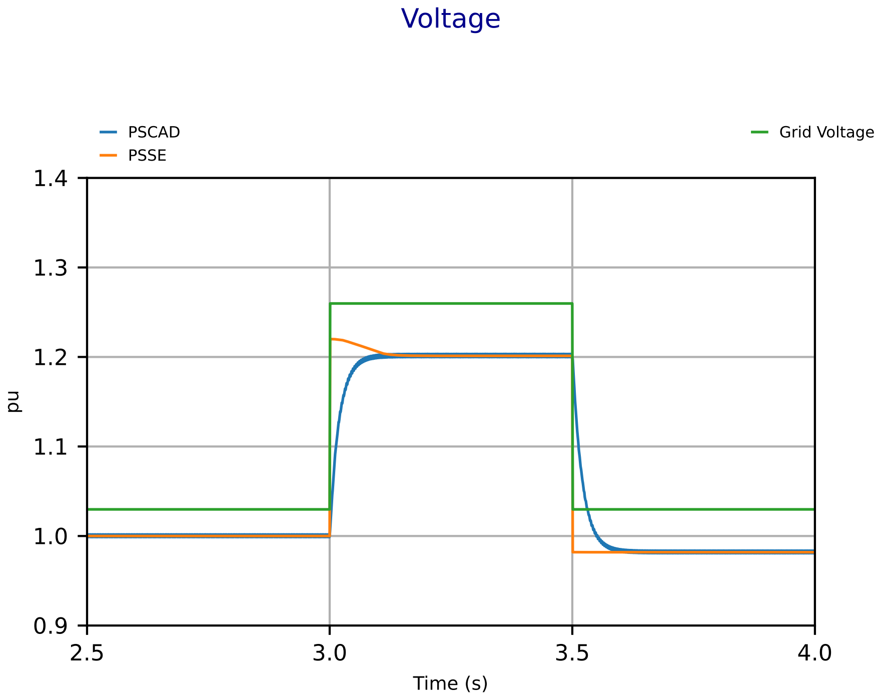
DER SMIB

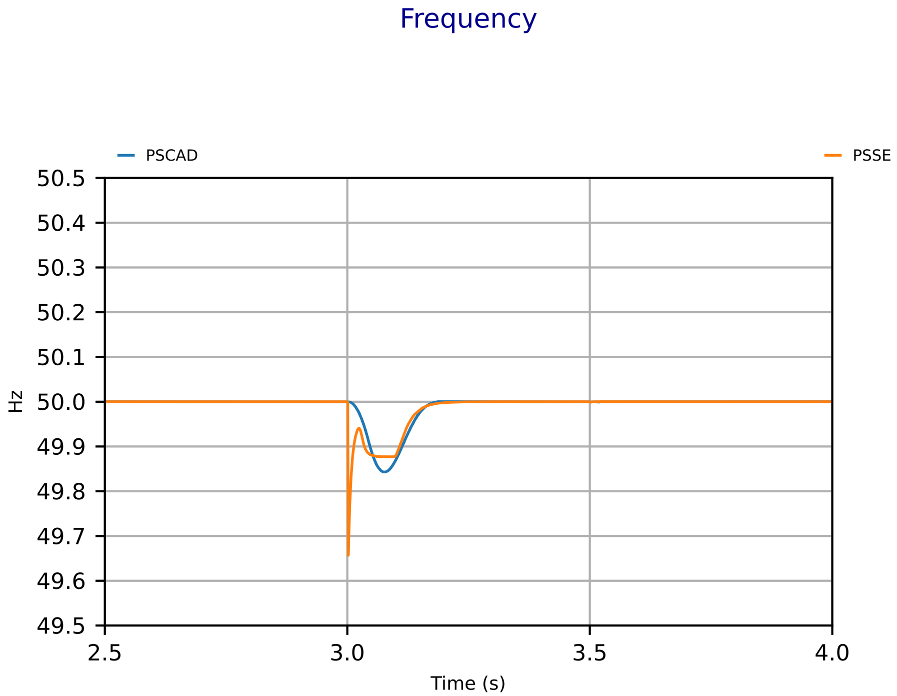
SCR = 10, X/R = 14

Test #5:

~120% Voltage disturbance for 500 ms

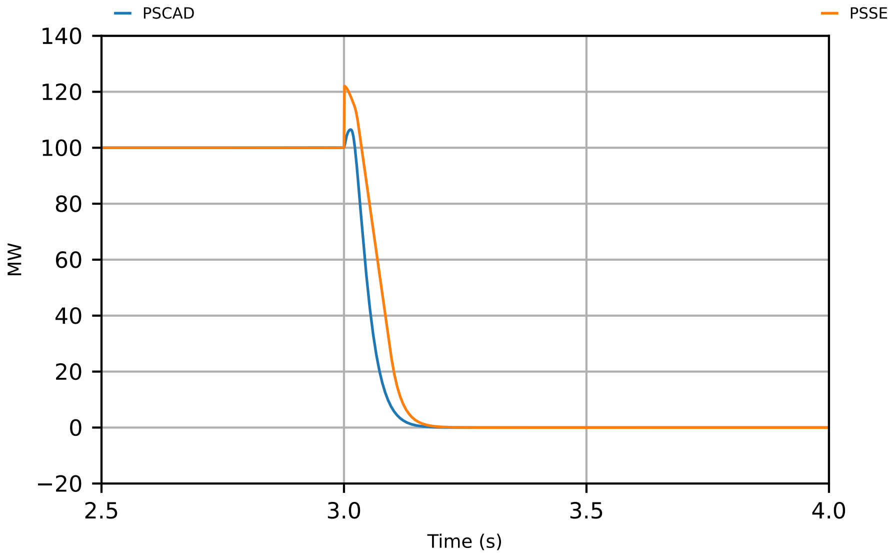
DER_SMIB_SCR_10_XR_14_T5_1



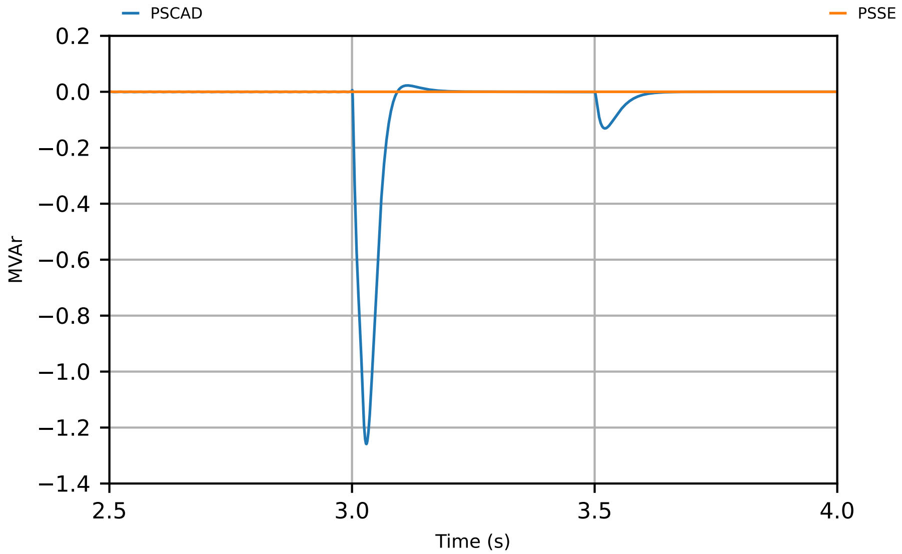


DER_SMIB_SCR_10_XR_14_T5_2

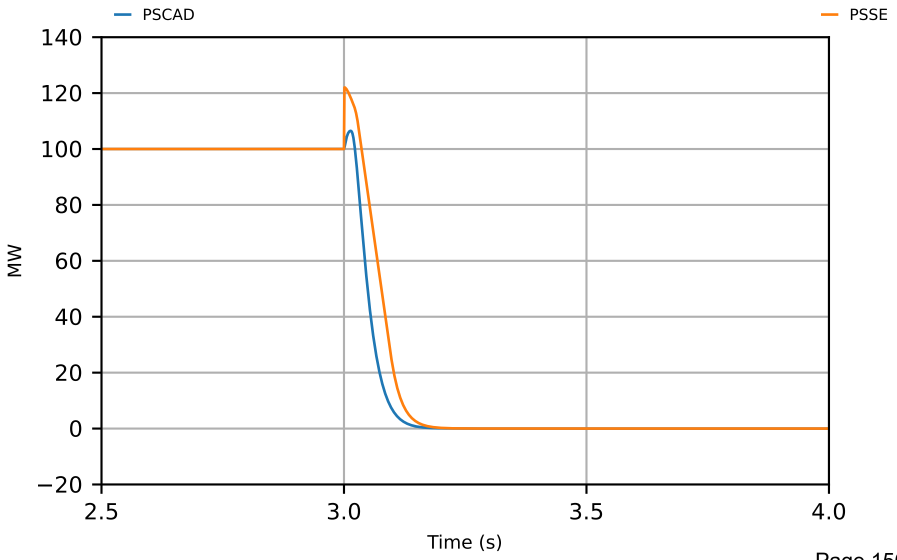
NSW DER Active Power



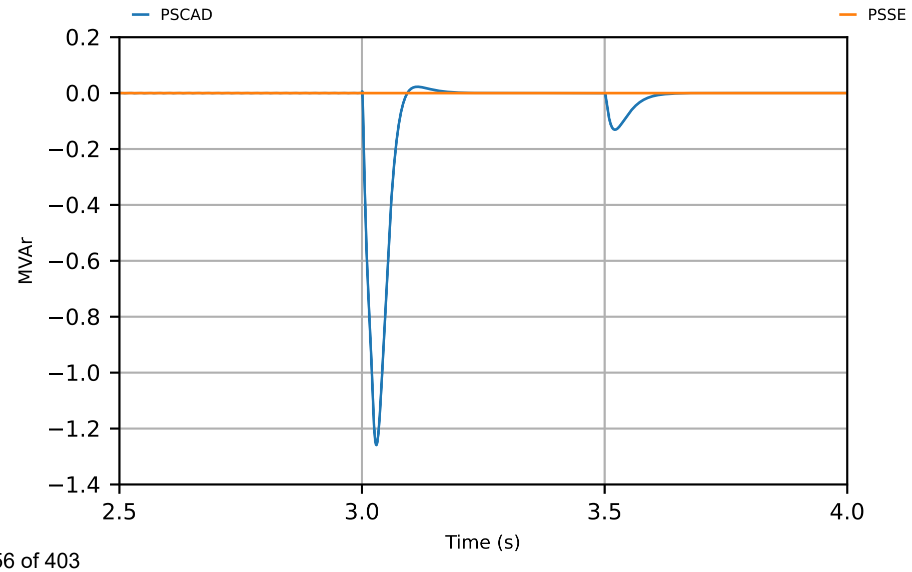
NSW DER Reactive Power



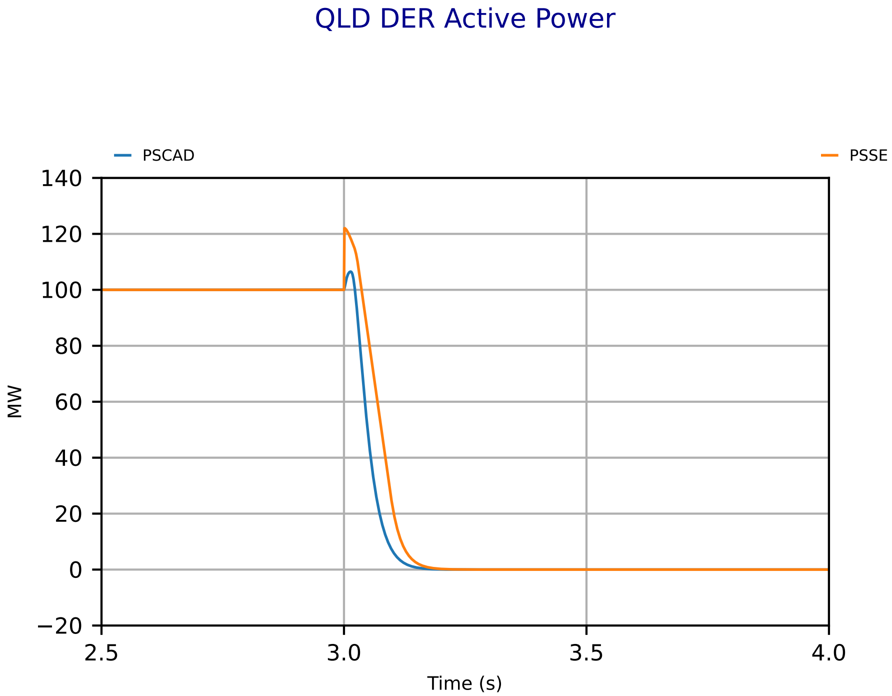
VIC DER Active Power

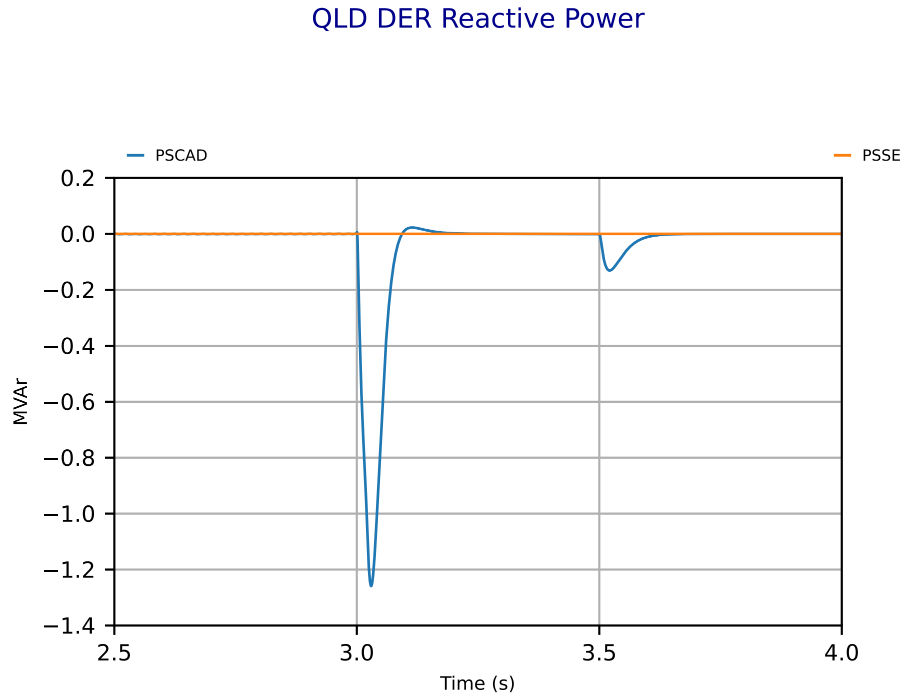


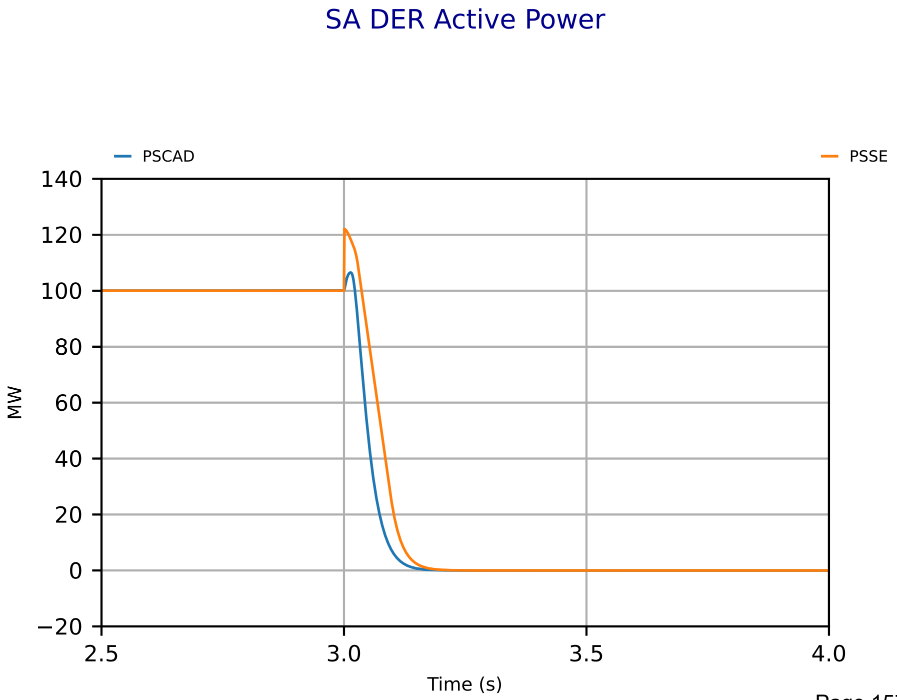
VIC DER Reactive Power

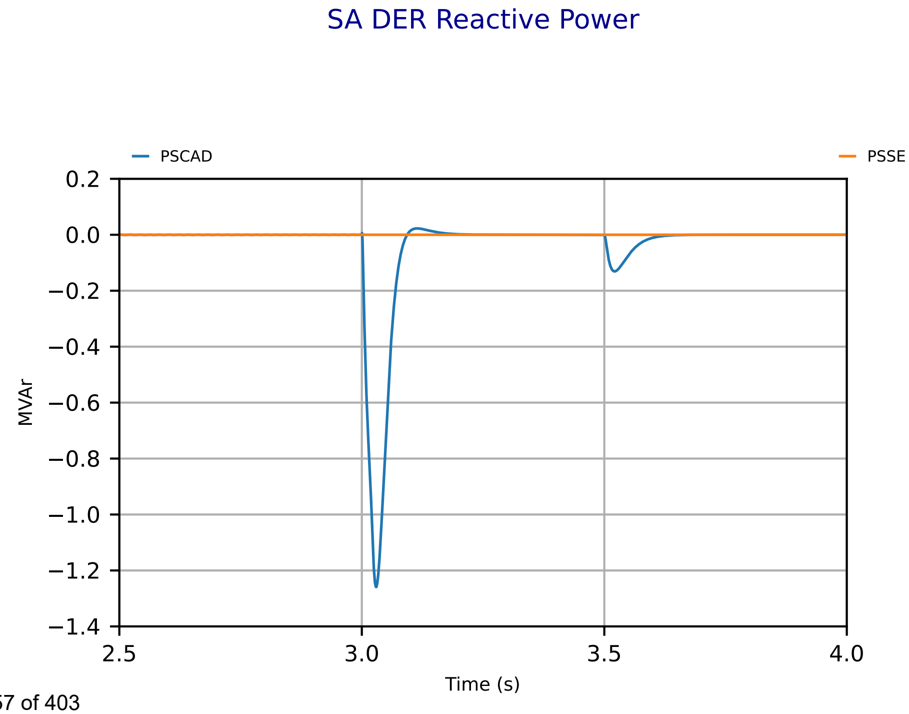


DER_SMIB_SCR_10_XR_14_T5_3









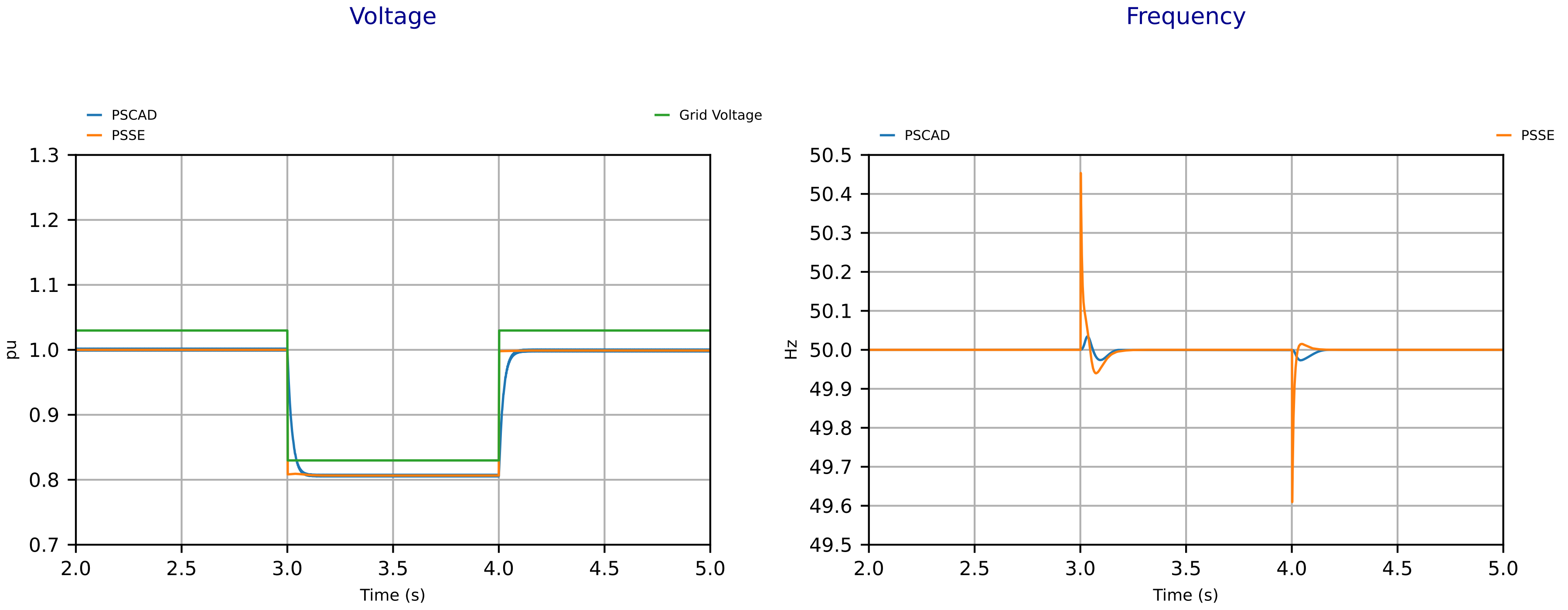
DER SMIB

SCR = 10, X/R = 14

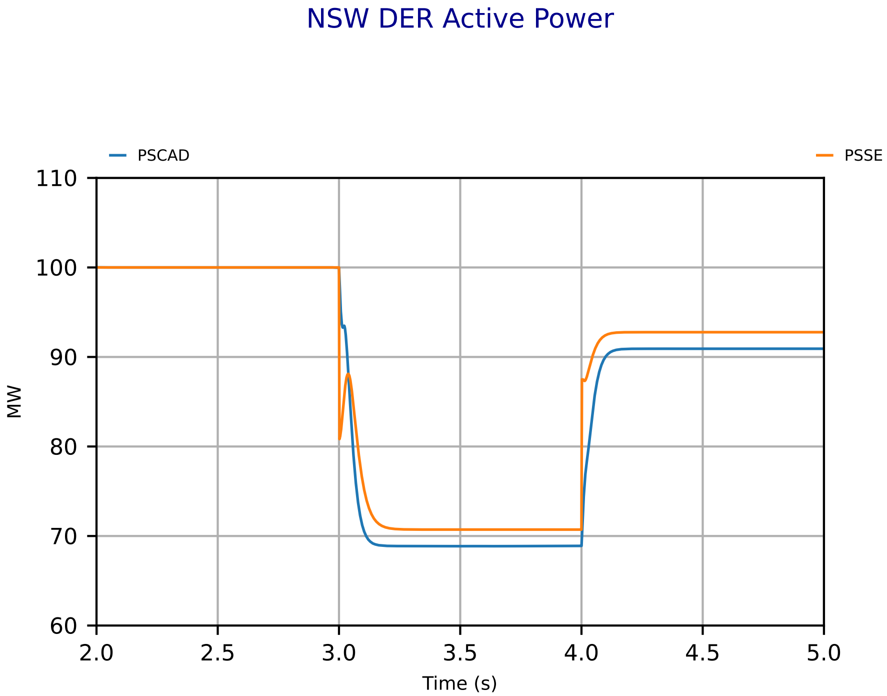
Test #6:

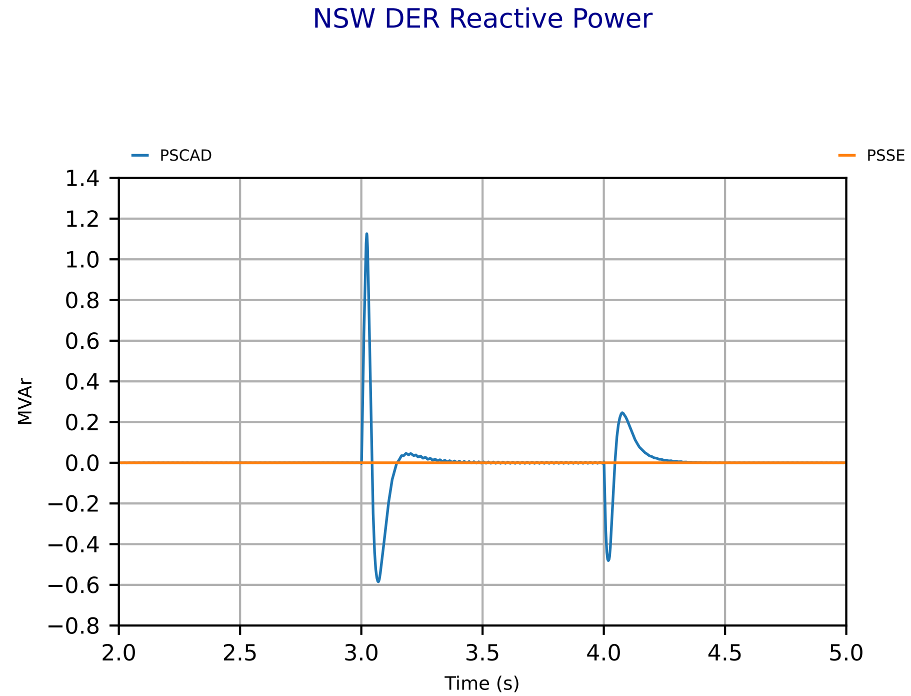
~80% Voltage disturbance for 1 sec

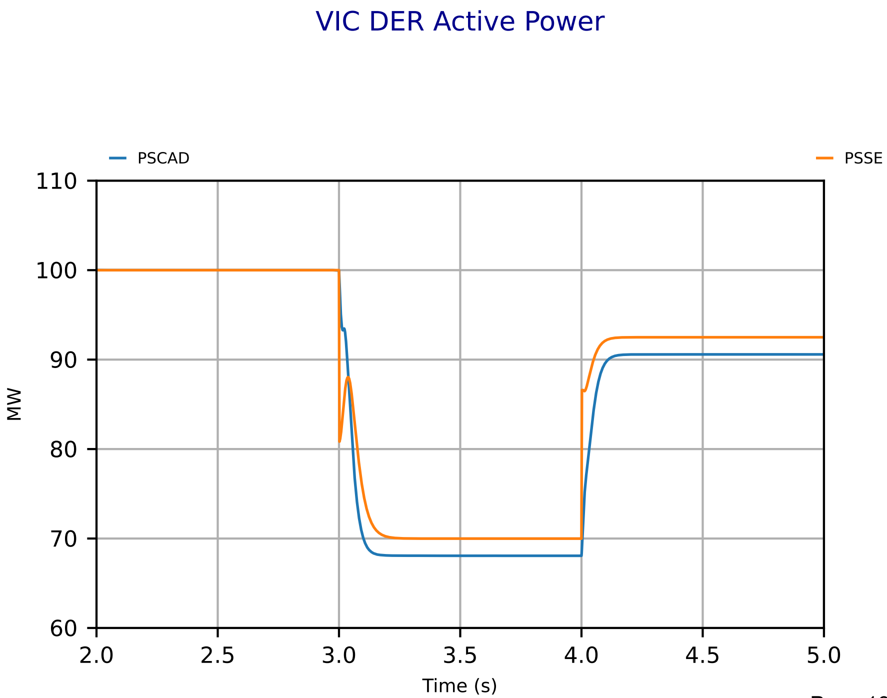
DER_SMIB_SCR_10_XR_14_T6_1

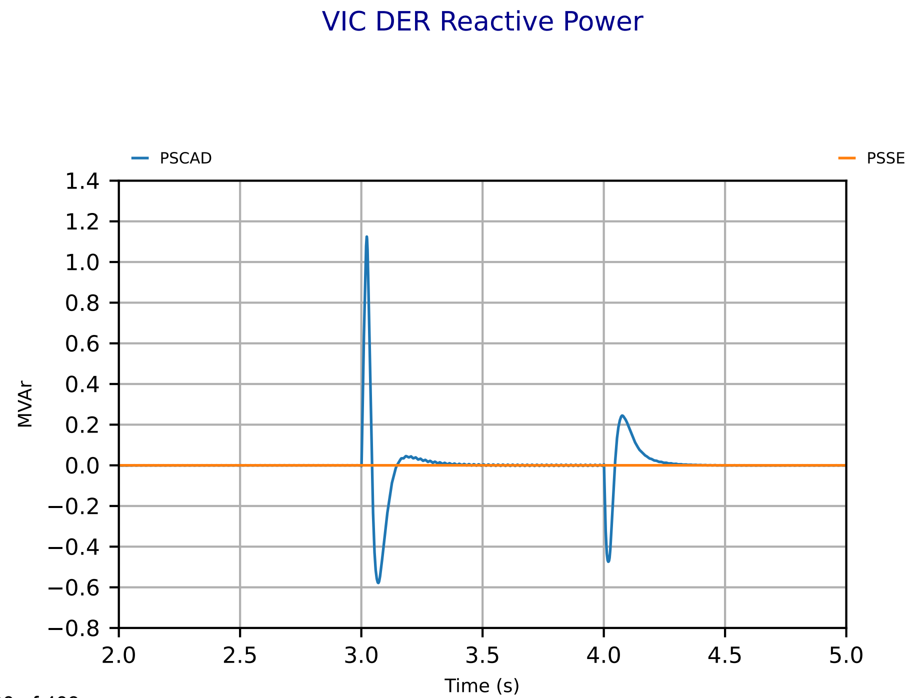


DER_SMIB_SCR_10_XR_14_T6_2



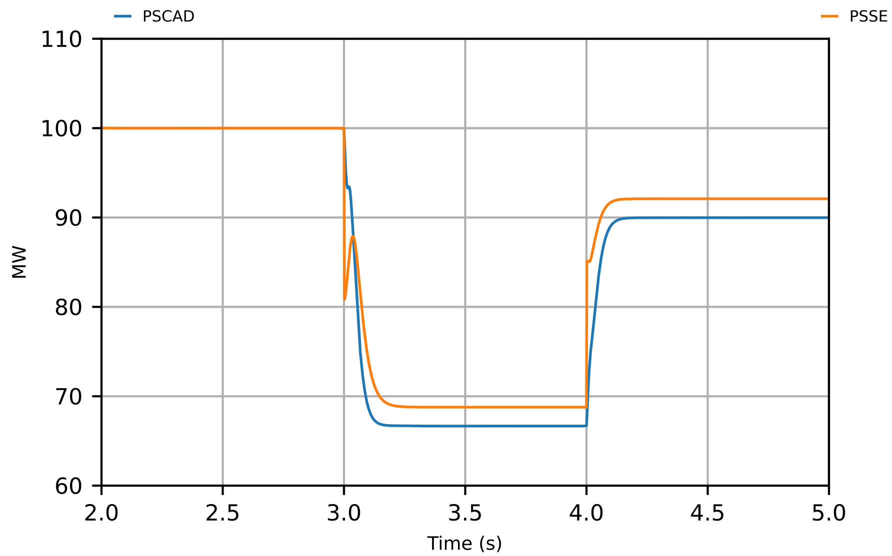




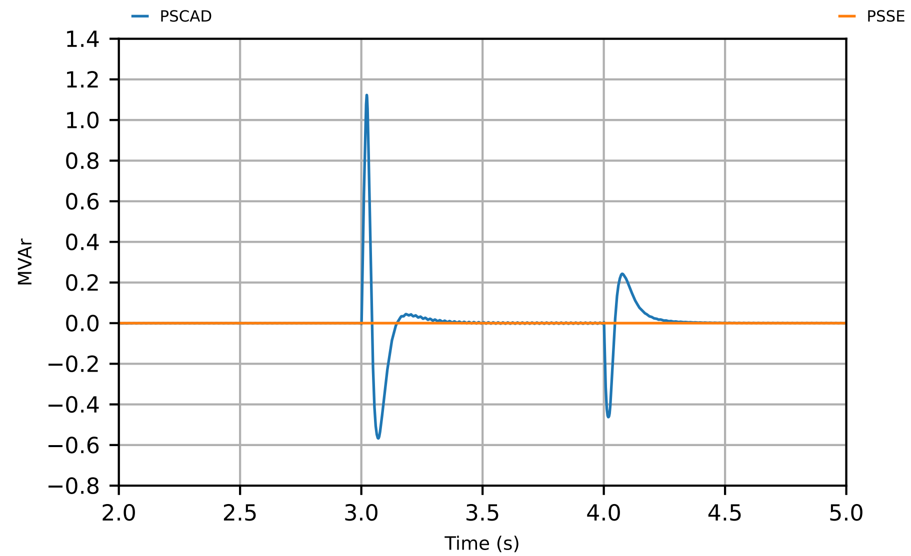


DER_SMIB_SCR_10_XR_14_T6_3

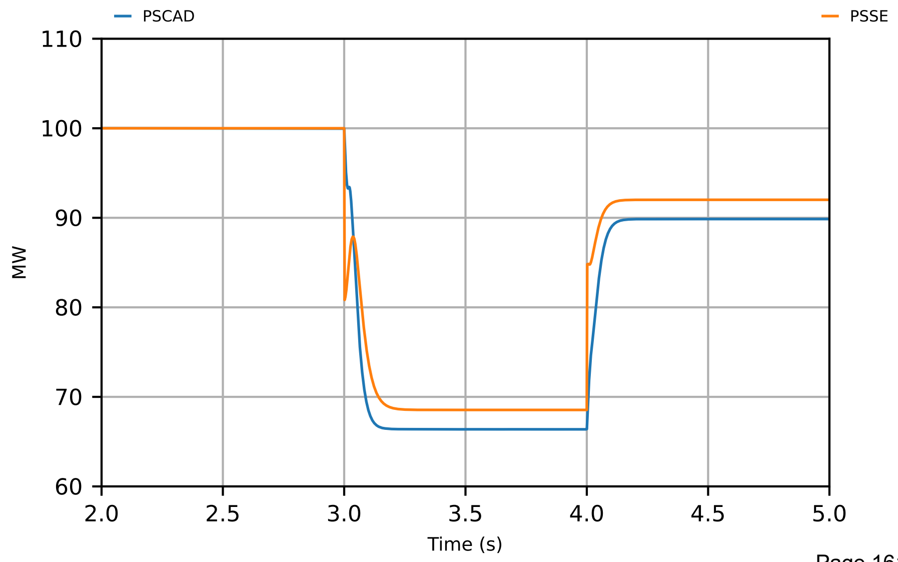
QLD DER Active Power



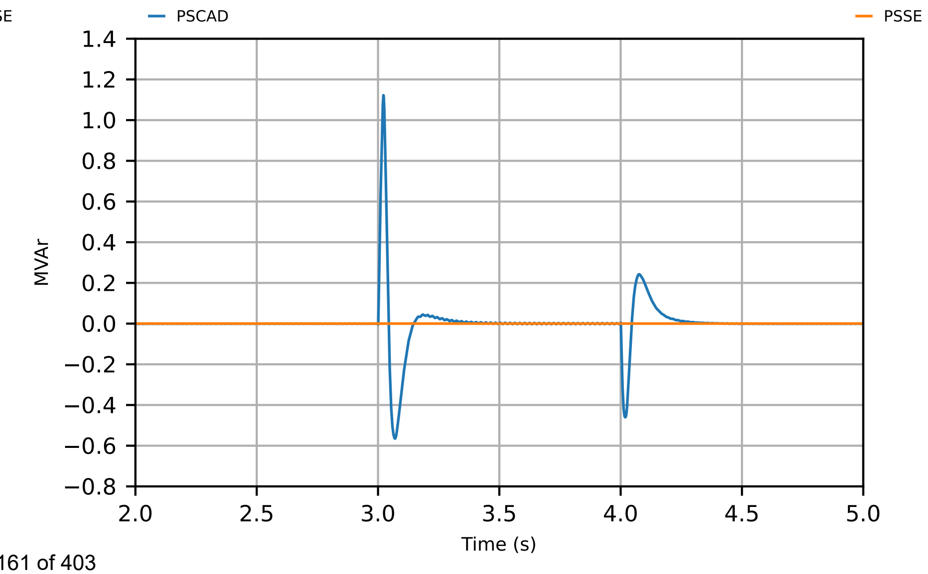
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



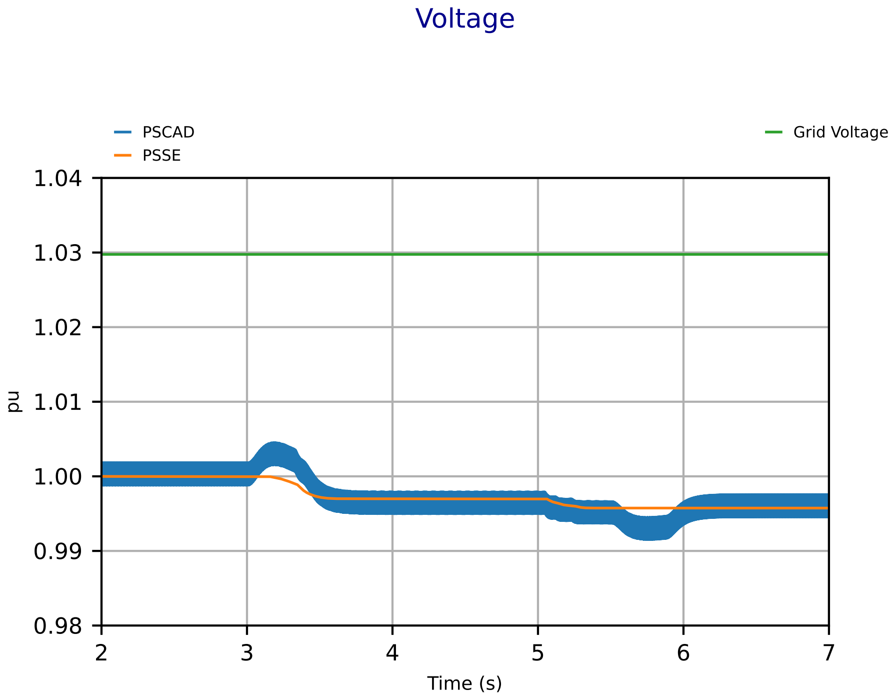
DER SMIB

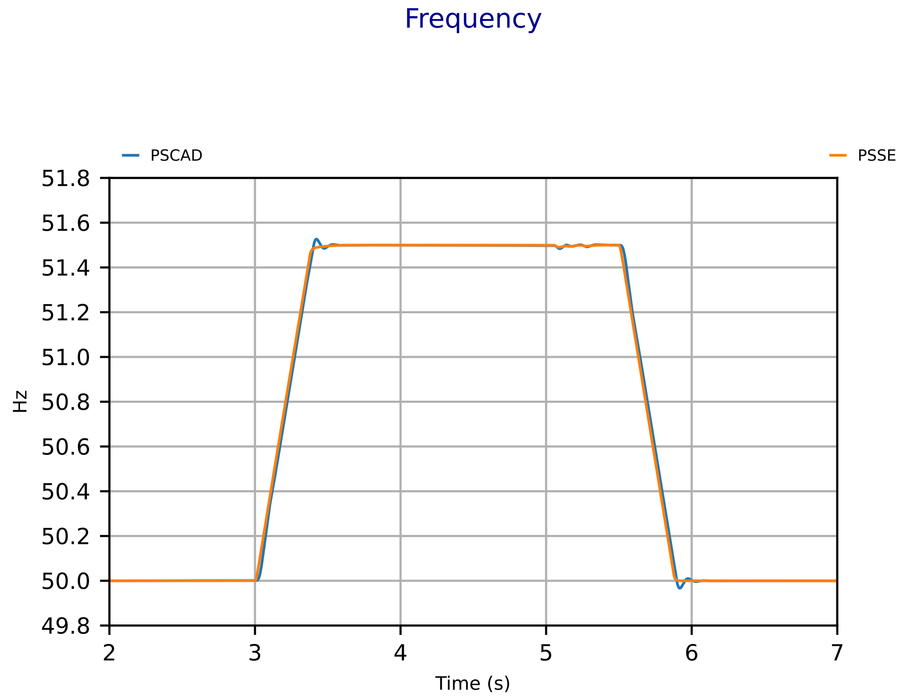
SCR = 10, X/R = 14

Test #7:

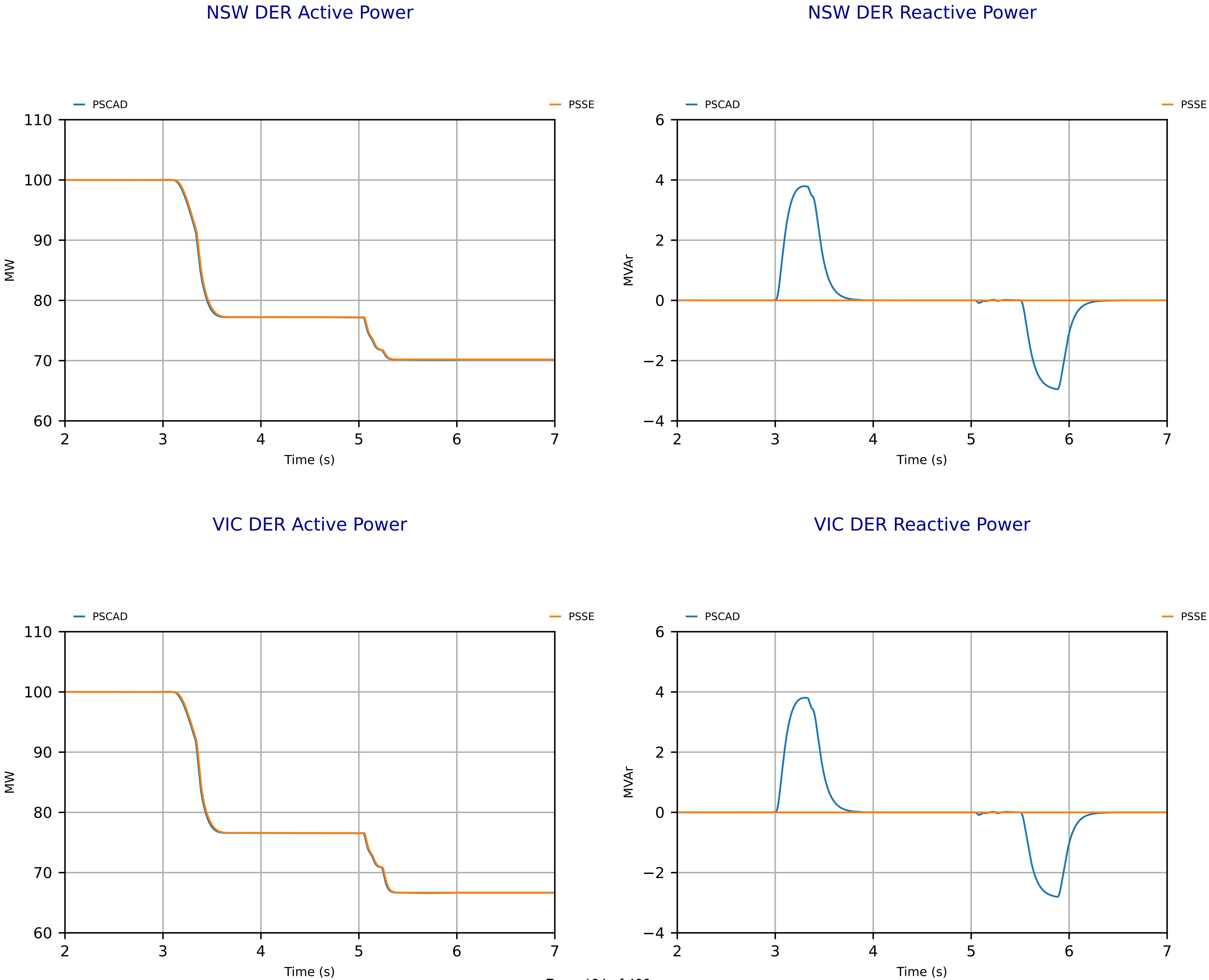
51.5 Hz frequency step for 2.5 sec (4 Hz/s)

DER_SMIB_SCR_10_XR_14_T7_1



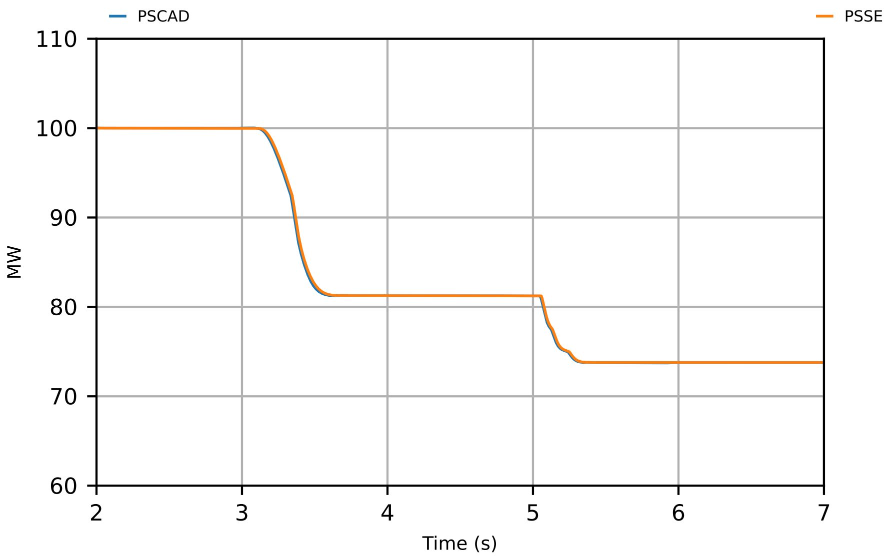


DER_SMIB_SCR_10_XR_14_T7_2

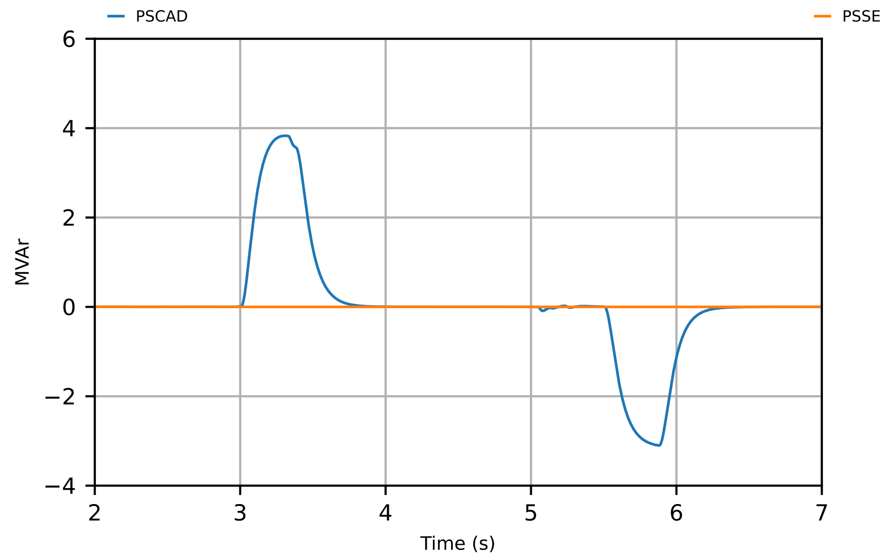


DER_SMIB_SCR_10_XR_14_T7_3

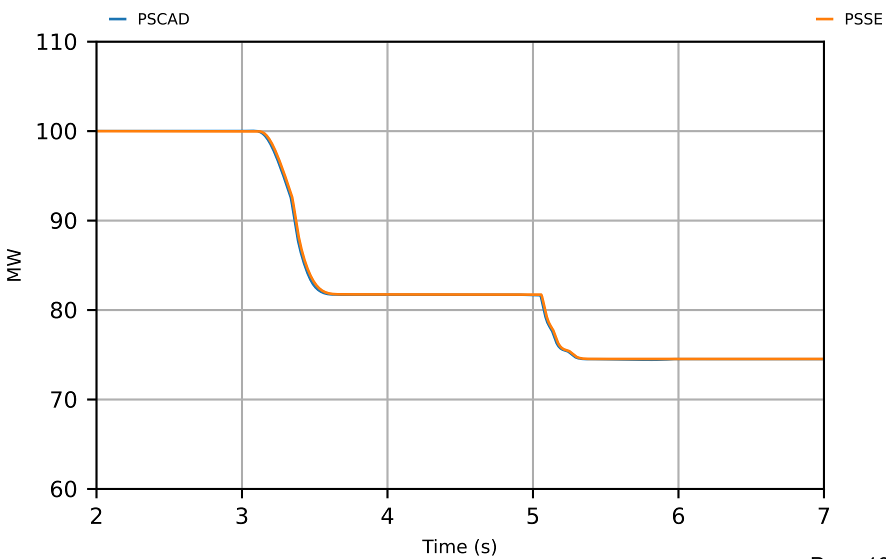
QLD DER Active Power



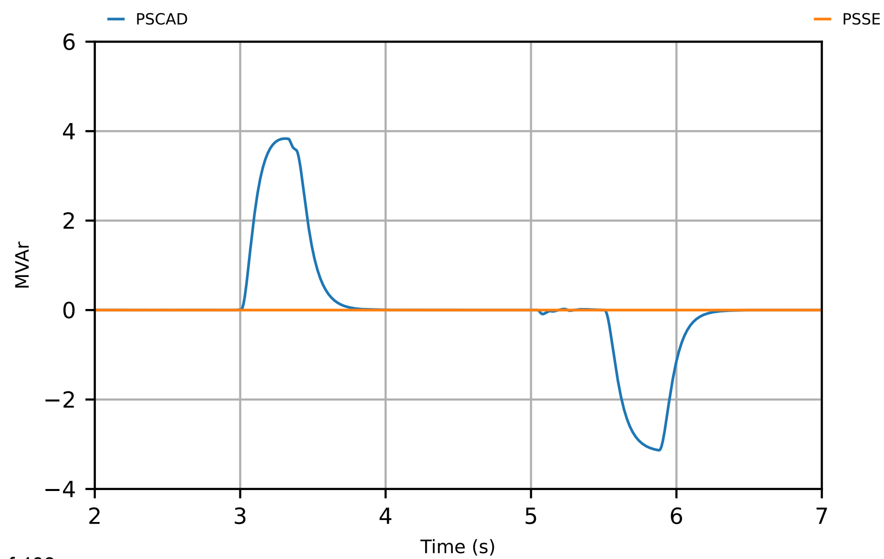
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



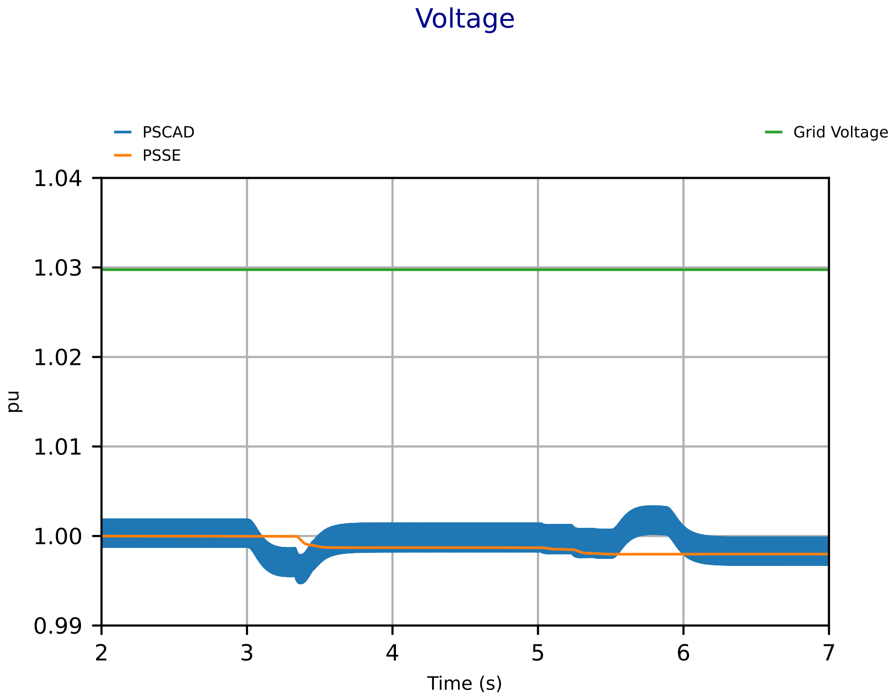
DER SMIB

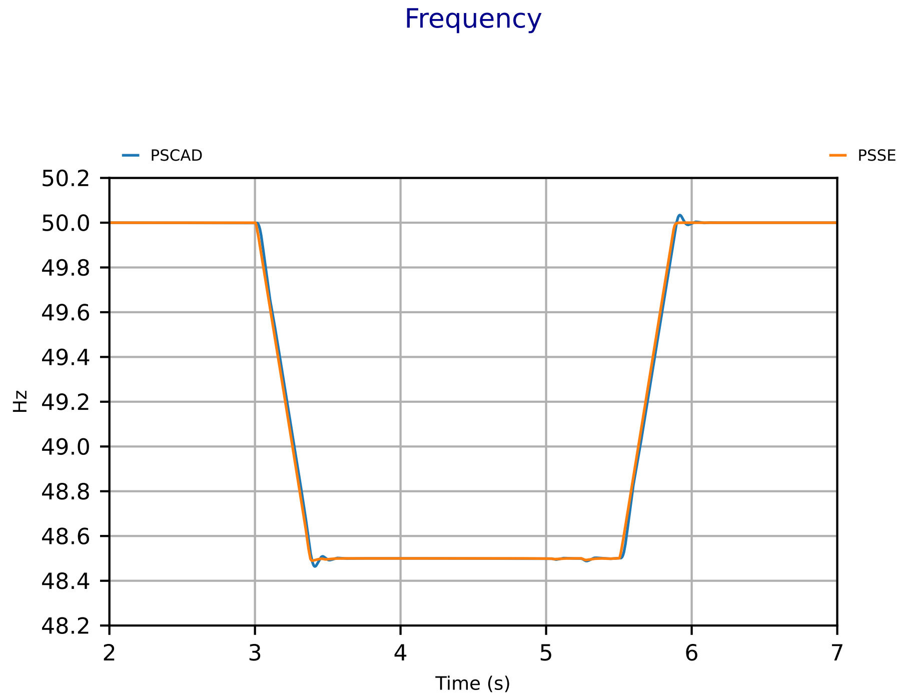
SCR = 10, X/R = 14

Test #8:

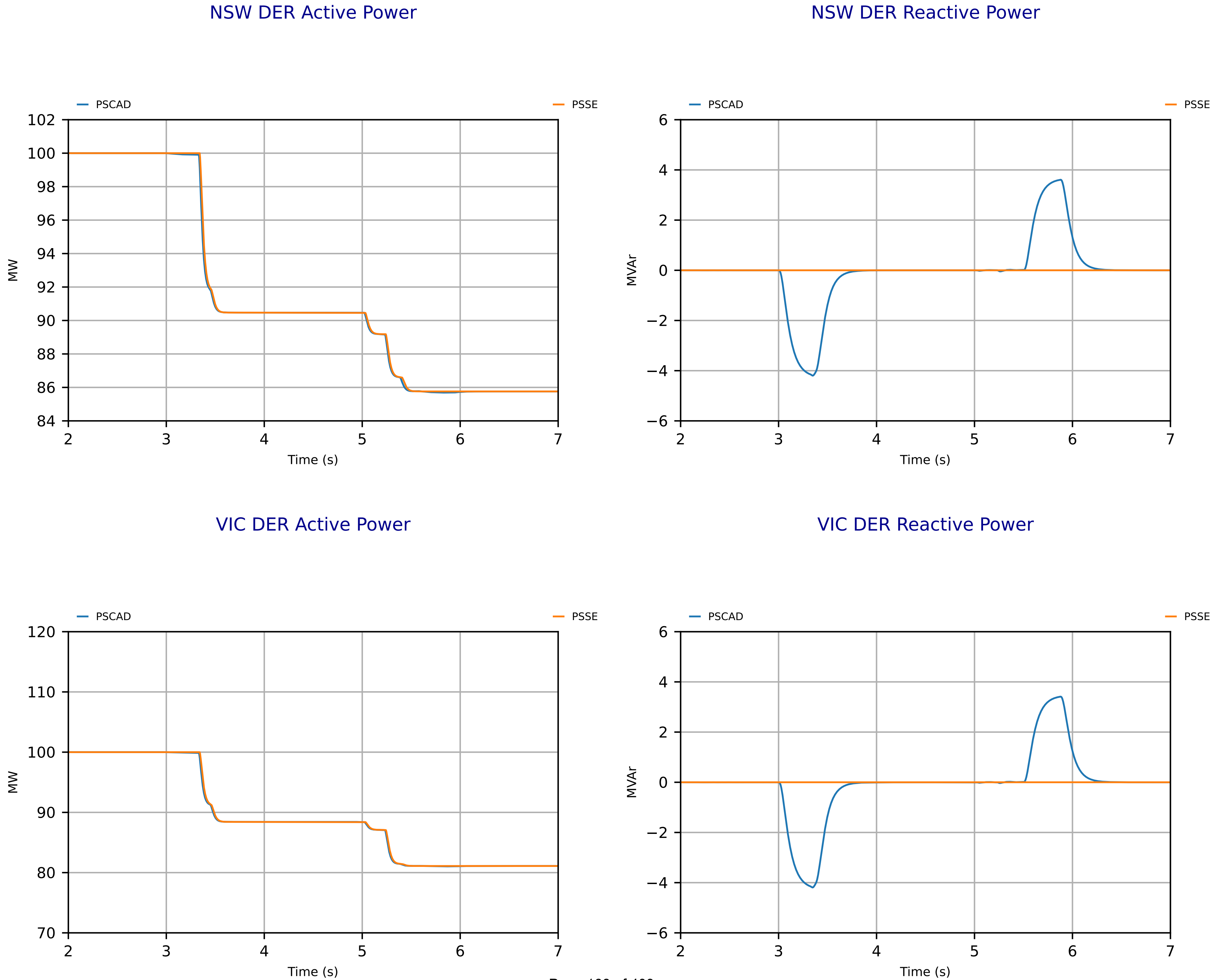
48.5 Hz frequency step for 2.5 sec (4 Hz/s)

DER_SMIB_SCR_10_XR_14_T8_1



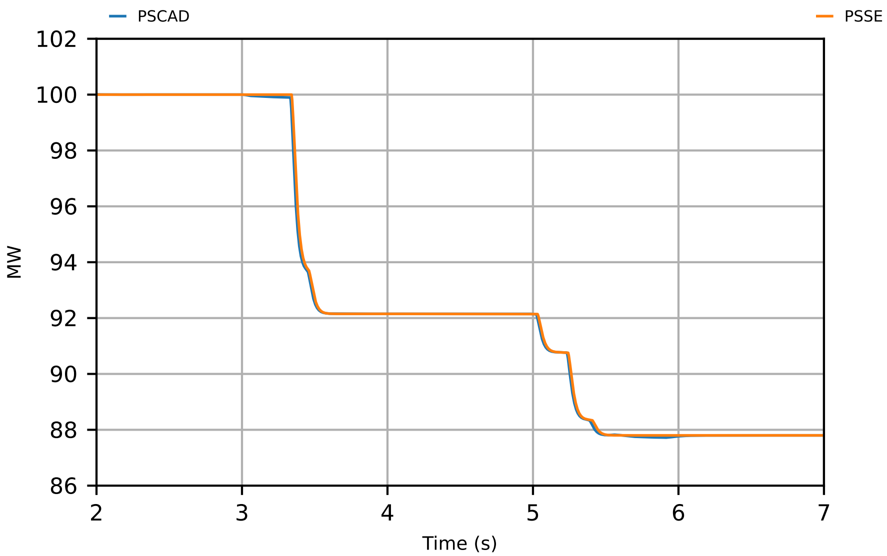


DER_SMIB_SCR_10_XR_14_T8_2

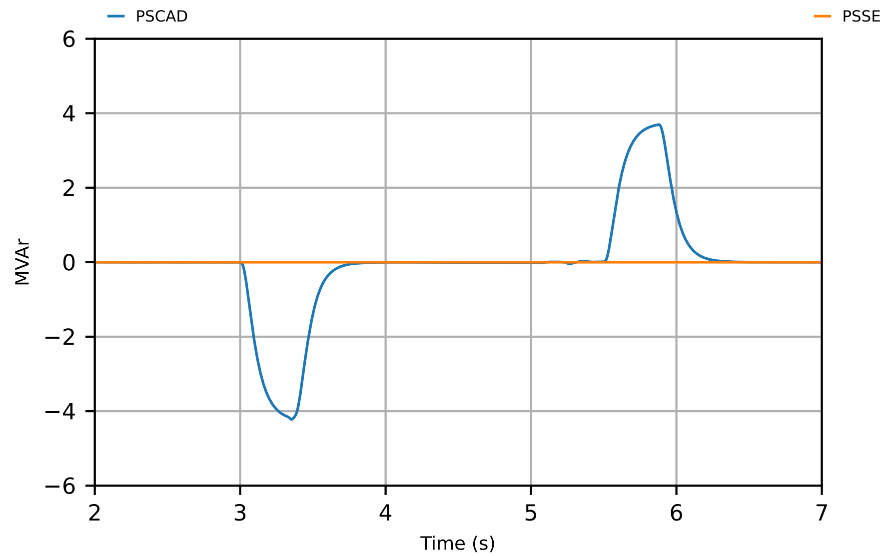


DER_SMIB_SCR_10_XR_14_T8_3

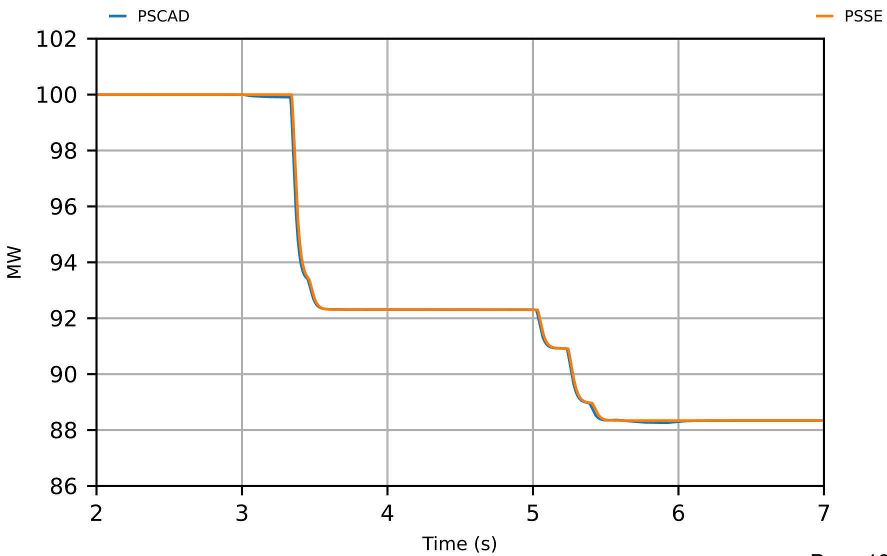
QLD DER Active Power



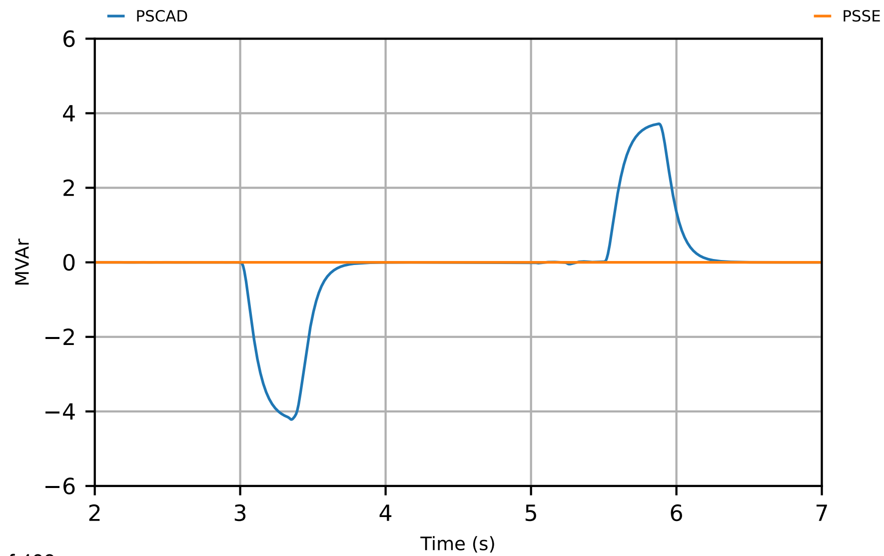
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



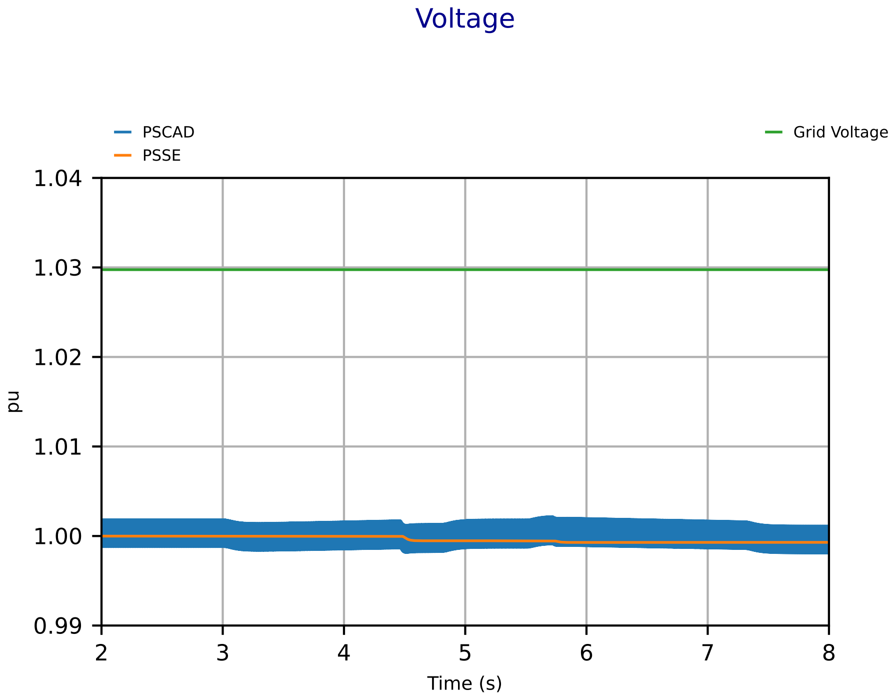
DER SMIB

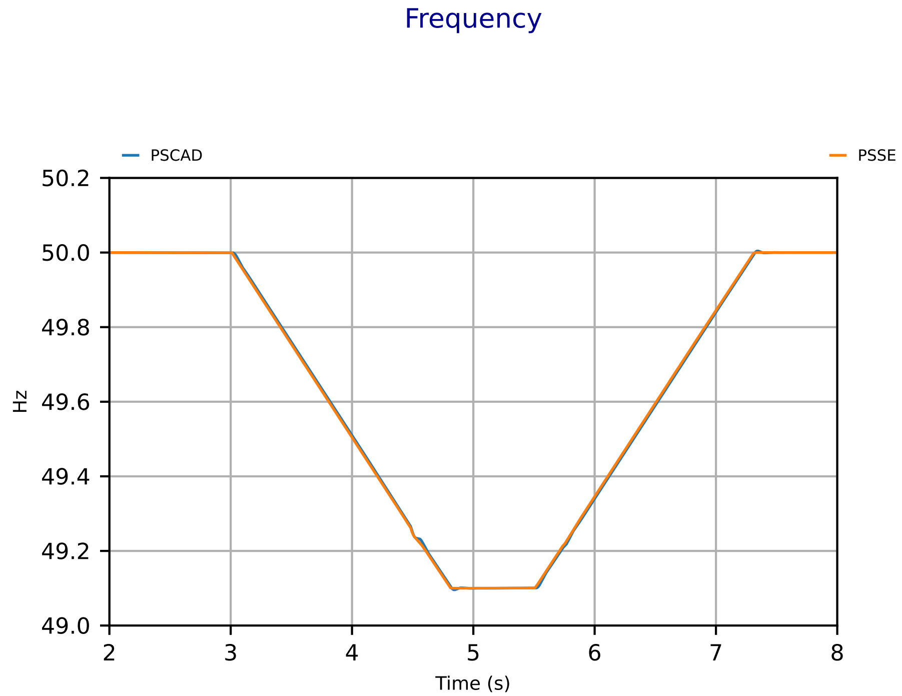
SCR = 10, X/R = 14

Test #9:

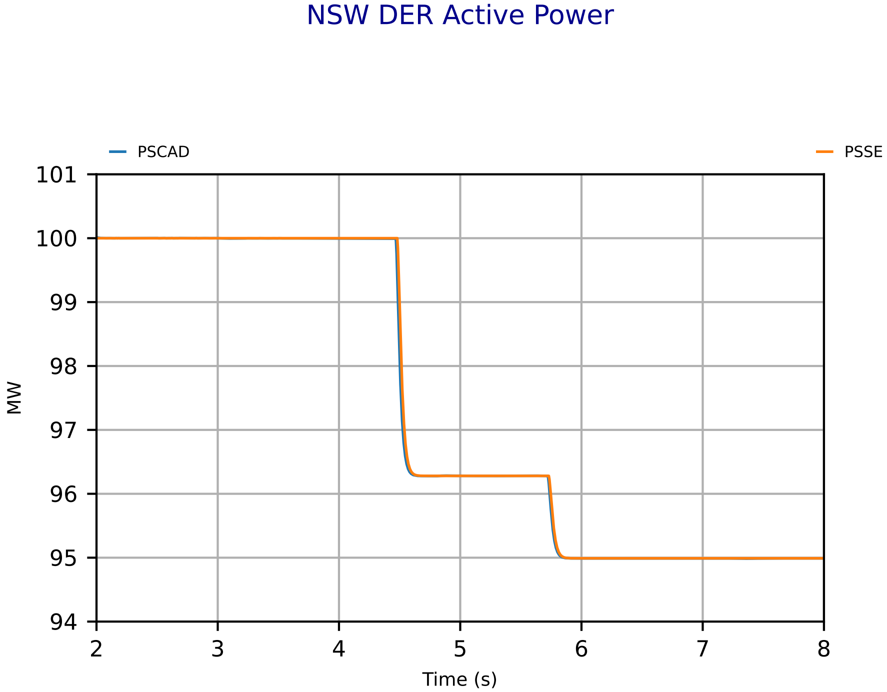
49.1 Hz slow frequency ramp (0.5 Hz/s)

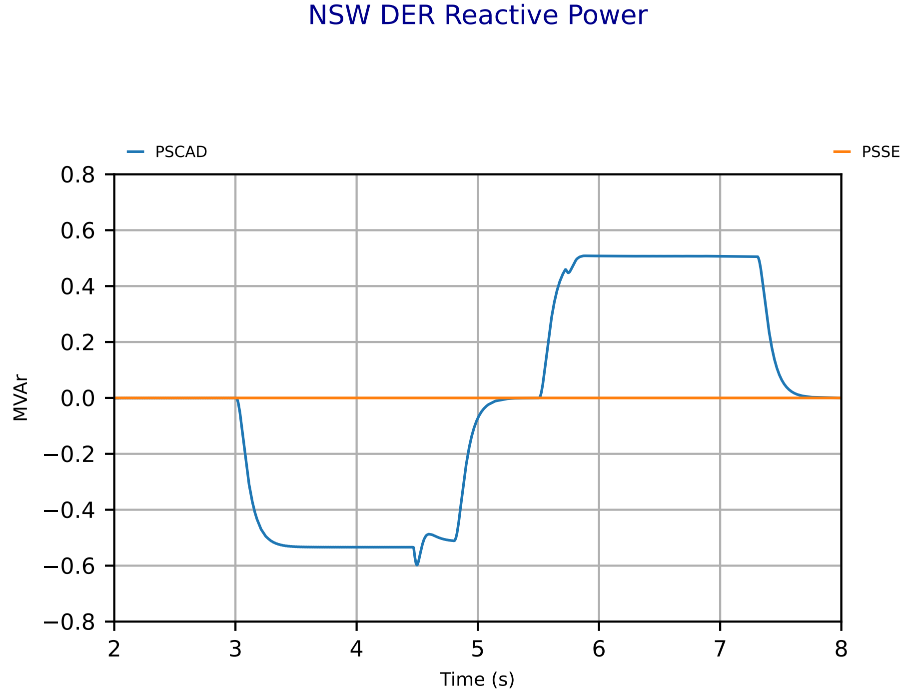
DER_SMIB_SCR_10_XR_14_T9_1

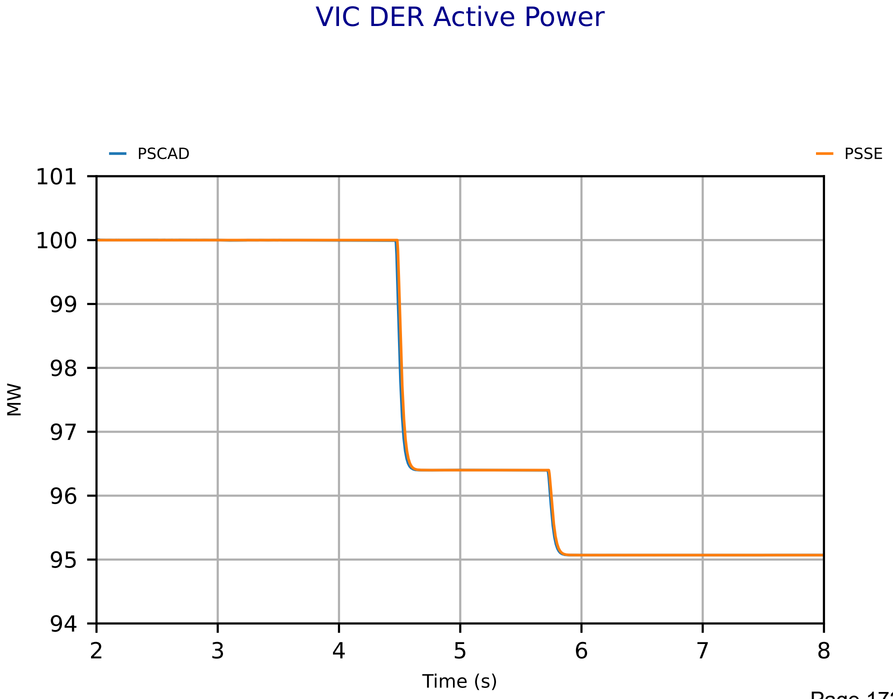


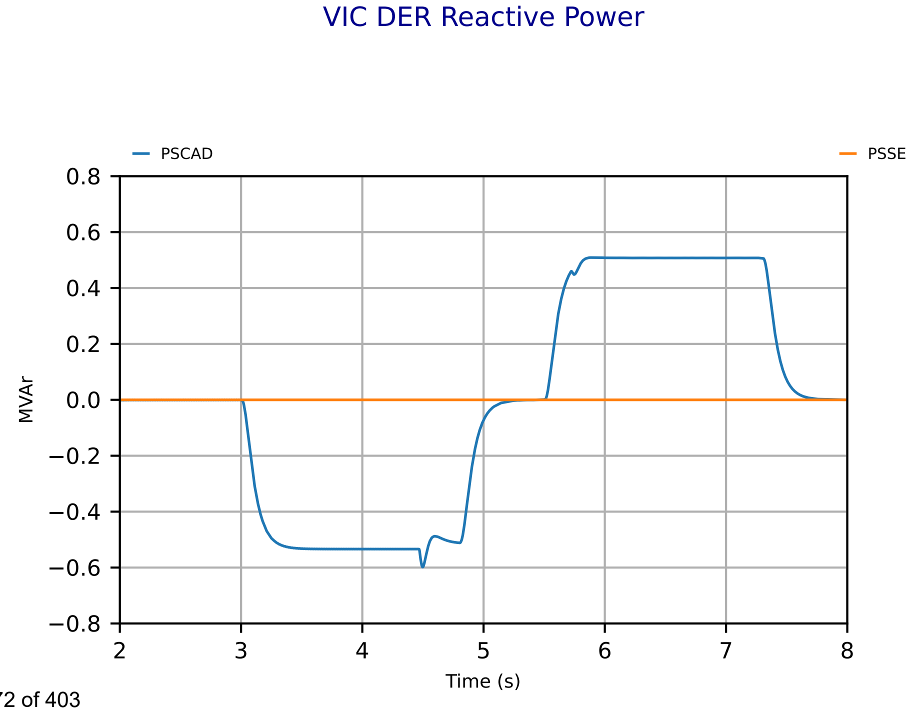


DER_SMIB_SCR_10_XR_14_T9_2

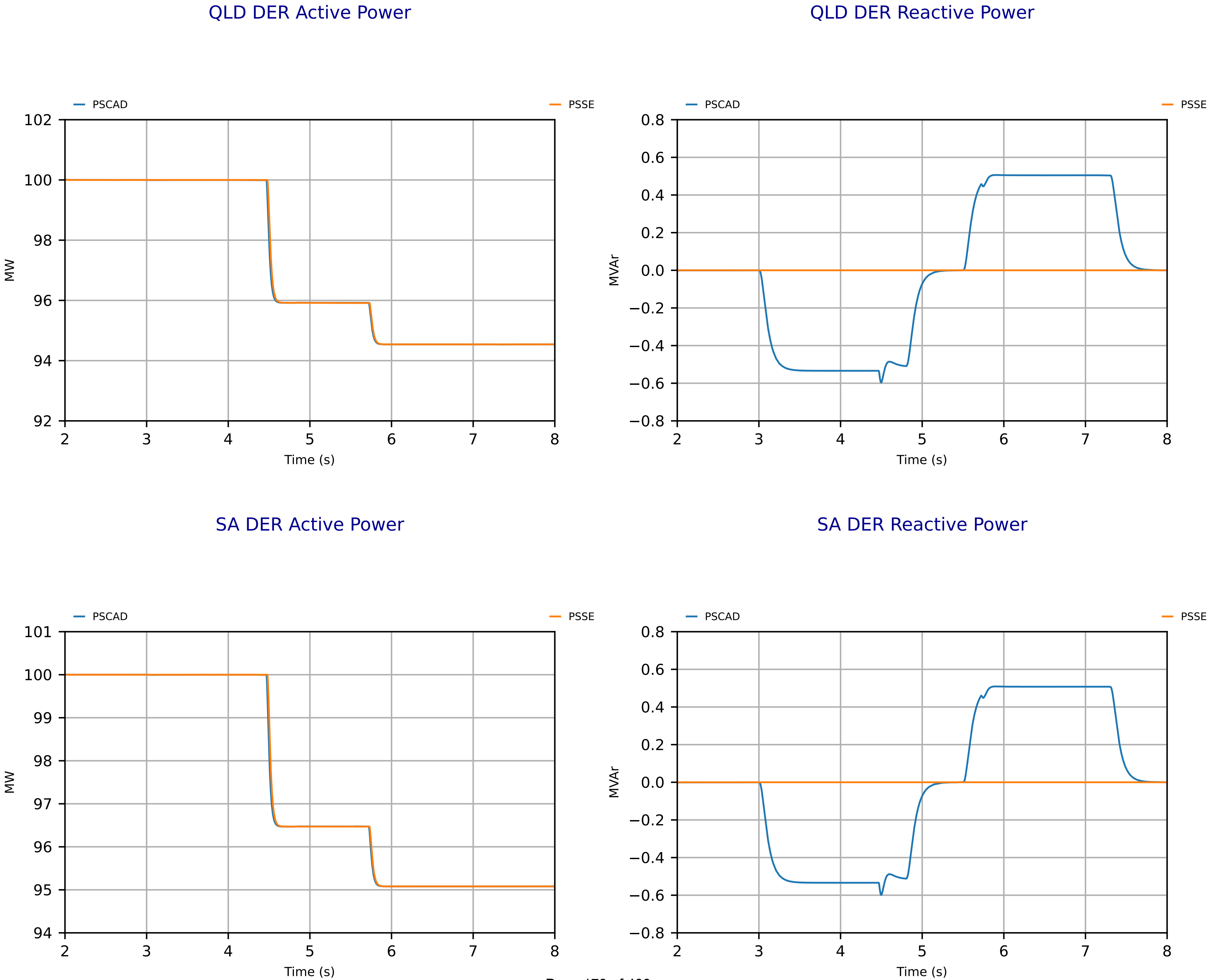








DER_SMIB_SCR_10_XR_14_T9_3



7.2 DER test results with phase angle trip logic enabled

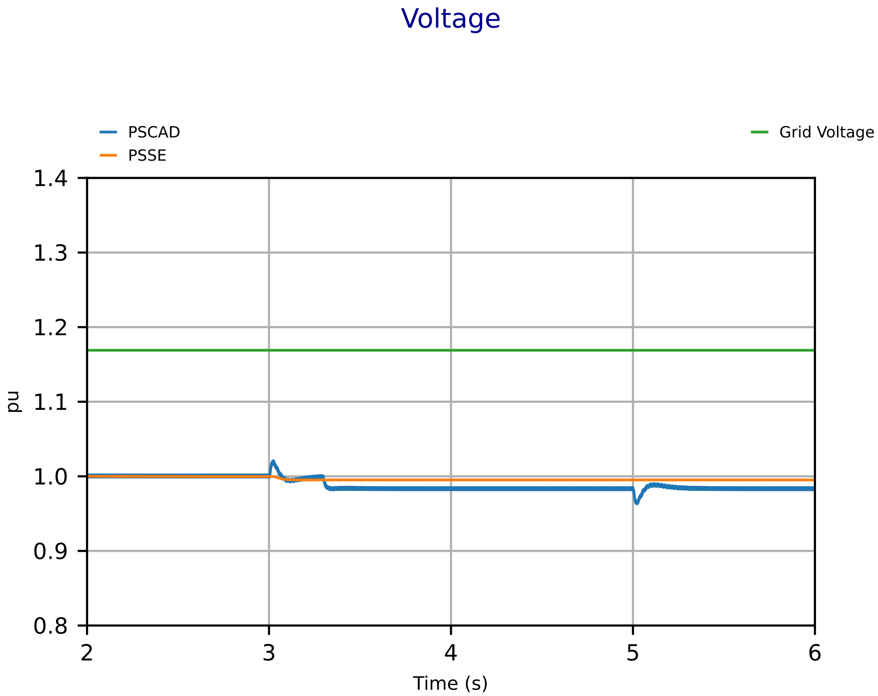
DER SMIB

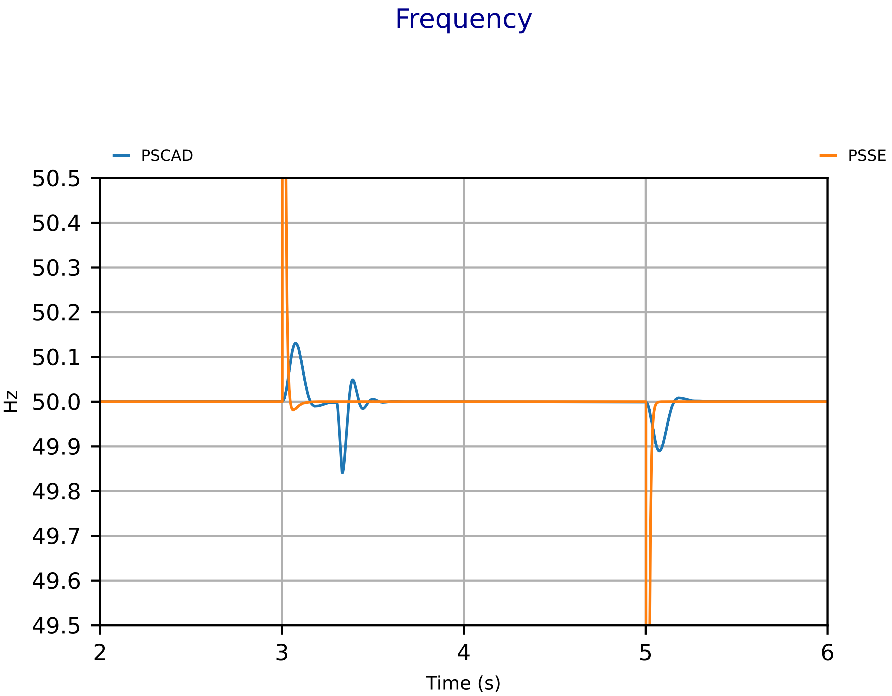
SCR = 3, X/R = 3

Test #10:

20° phase angle step

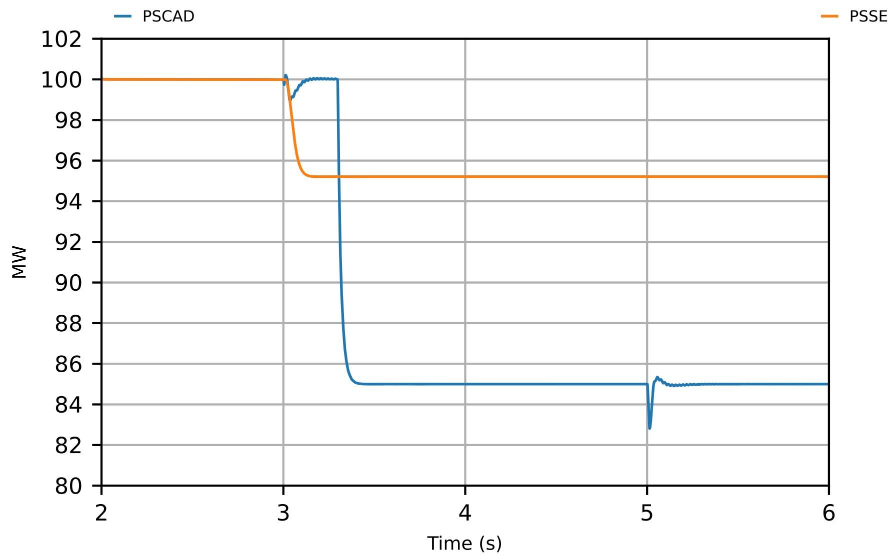
DER_SMIB_SCR_3_XR_3_T10_1



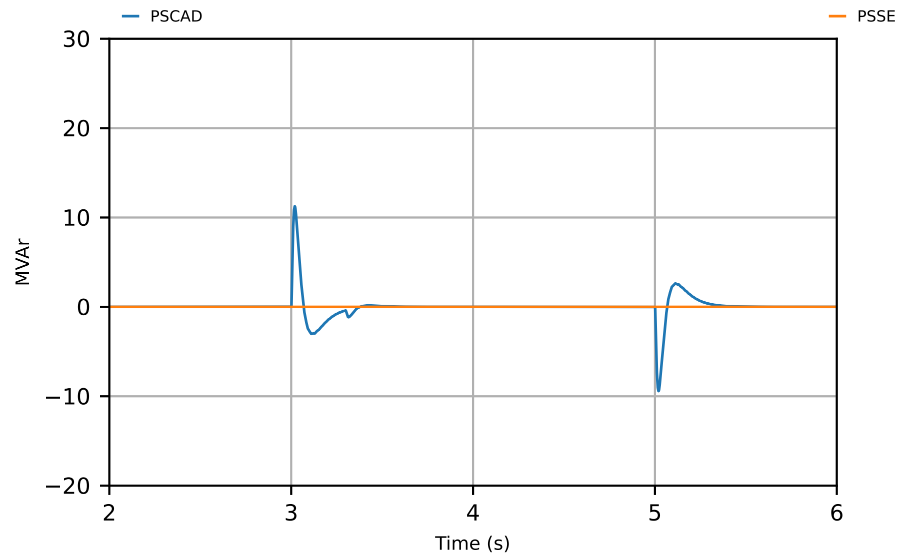


DER_SMIB_SCR_3_XR_3_T10_2

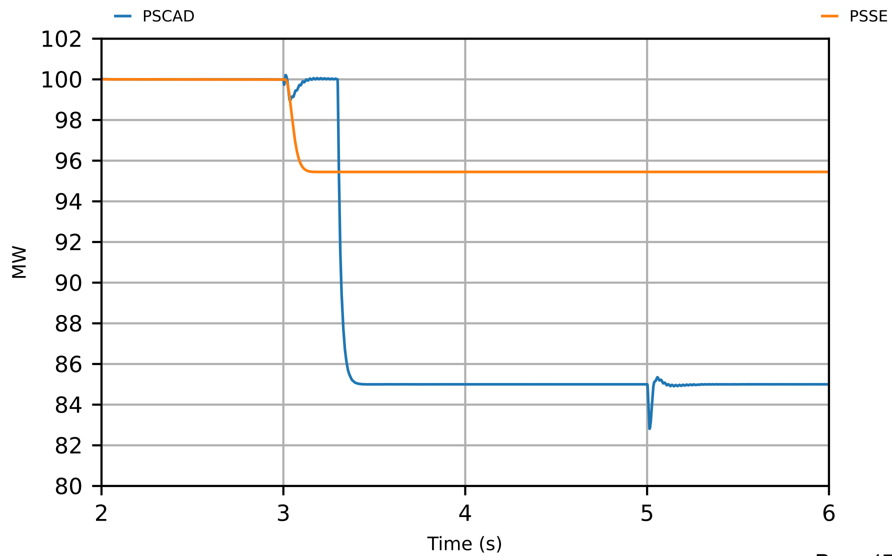
NSW DER Active Power



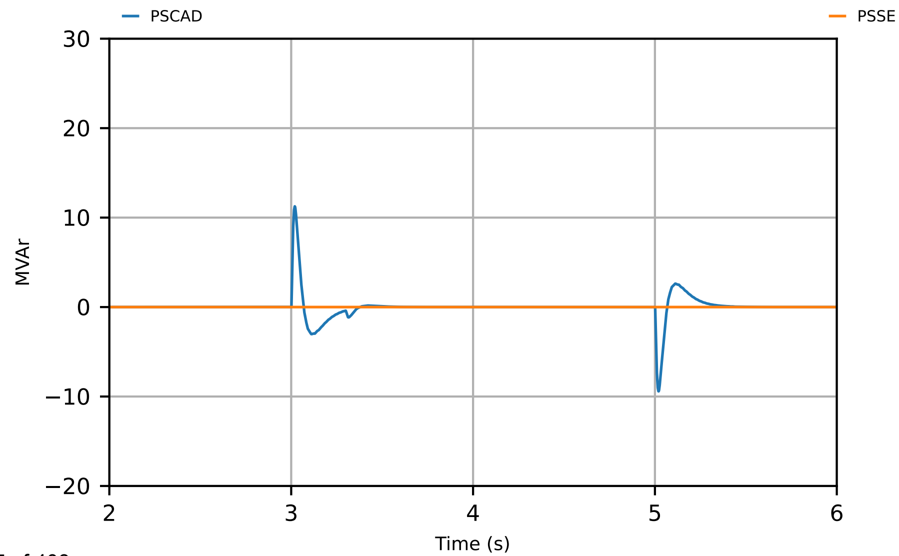
NSW DER Reactive Power



VIC DER Active Power

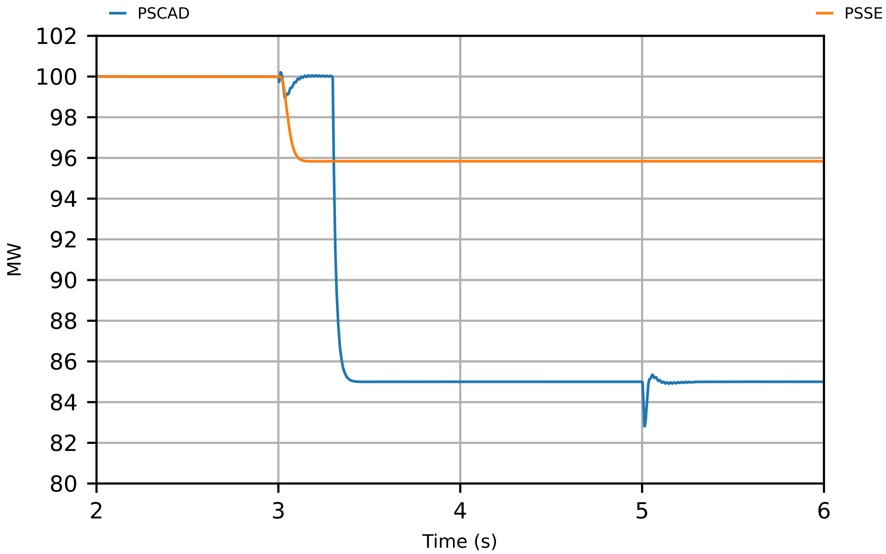


VIC DER Reactive Power

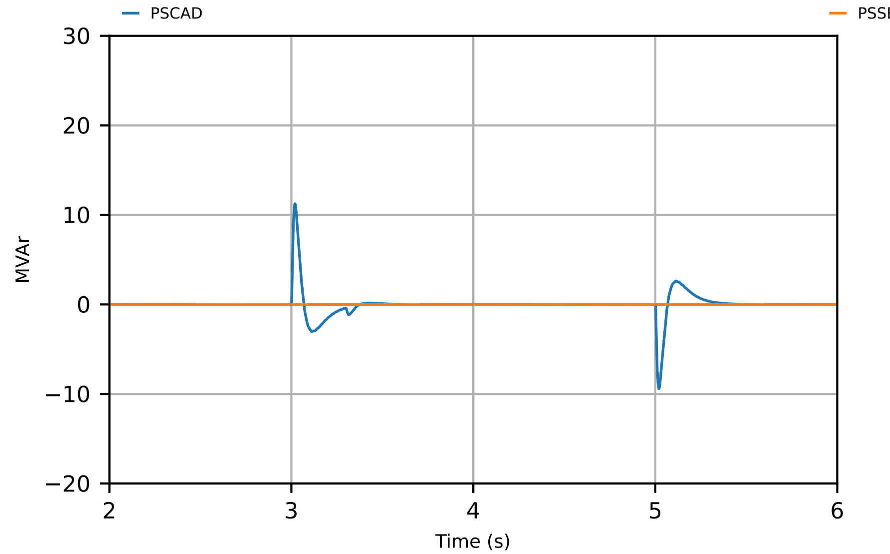


DER_SMIB_SCR_3_XR_3_T10_3

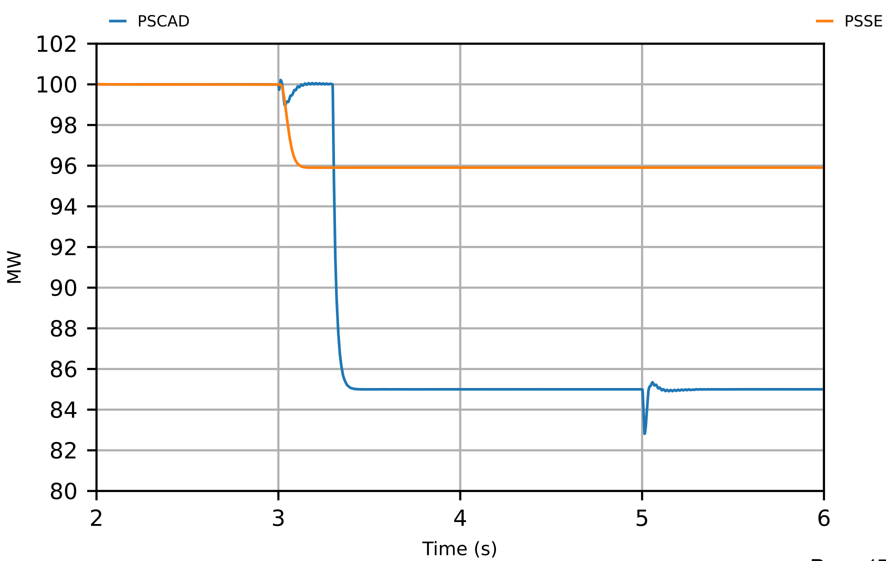
QLD DER Active Power



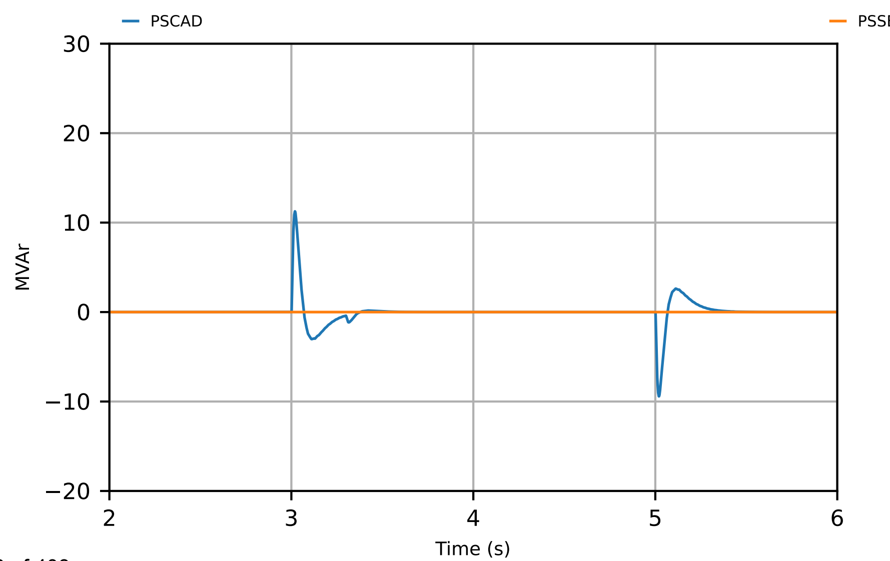
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



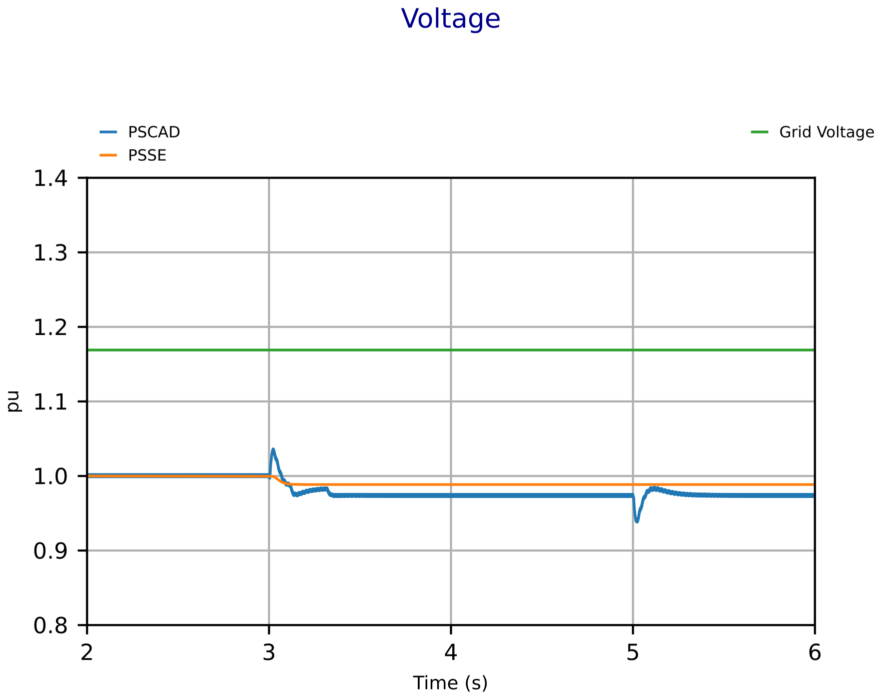
DER SMIB

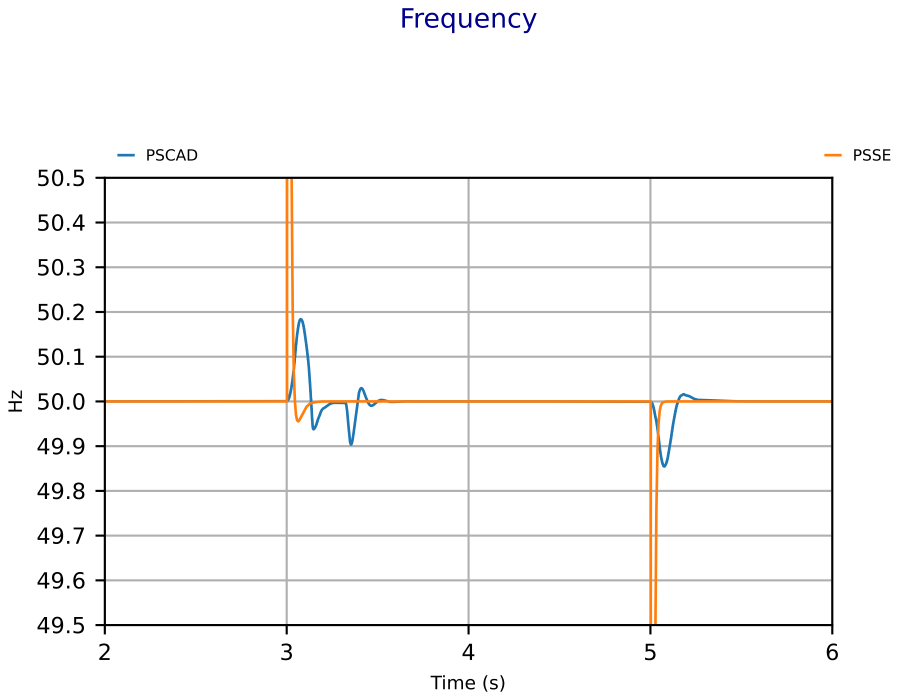
SCR = 3, X/R = 3

Test #11:

40° phase angle step

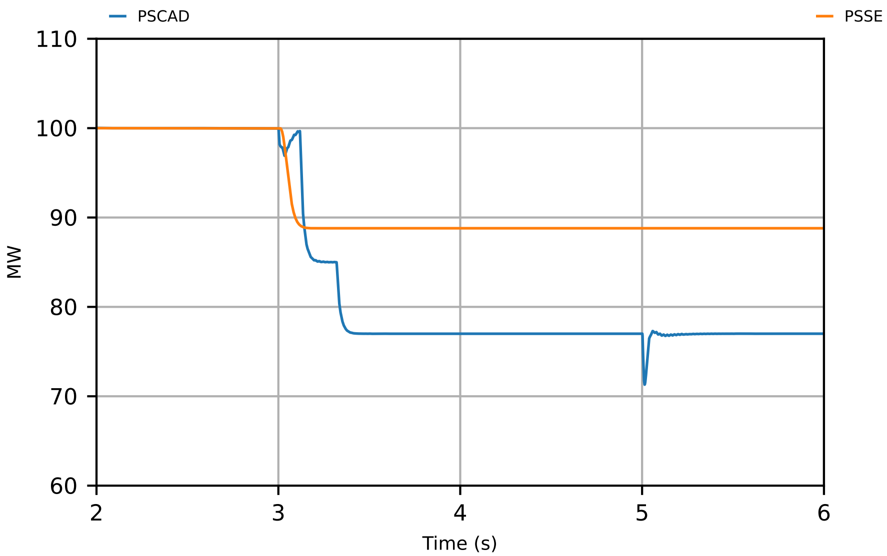
DER_SMIB_SCR_3_XR_3_T11_1



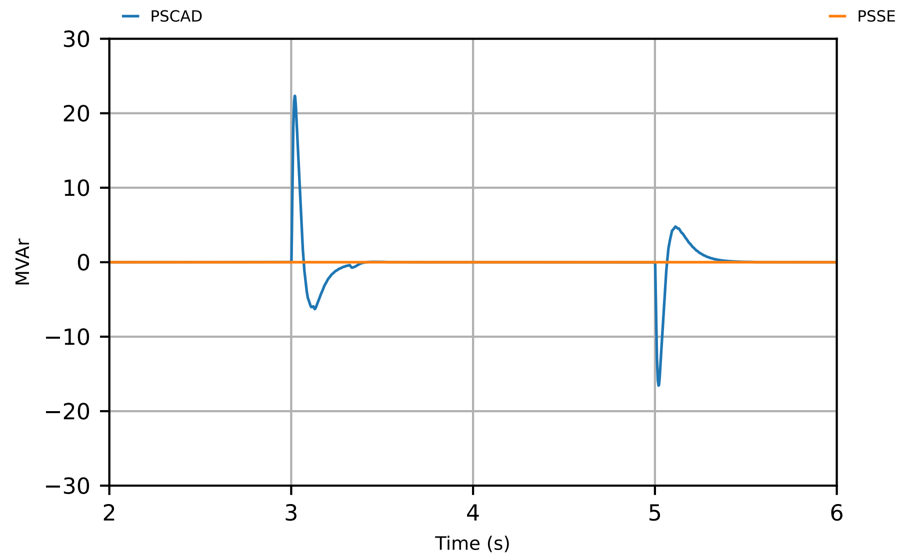


DER_SMIB_SCR_3_XR_3_T11_2

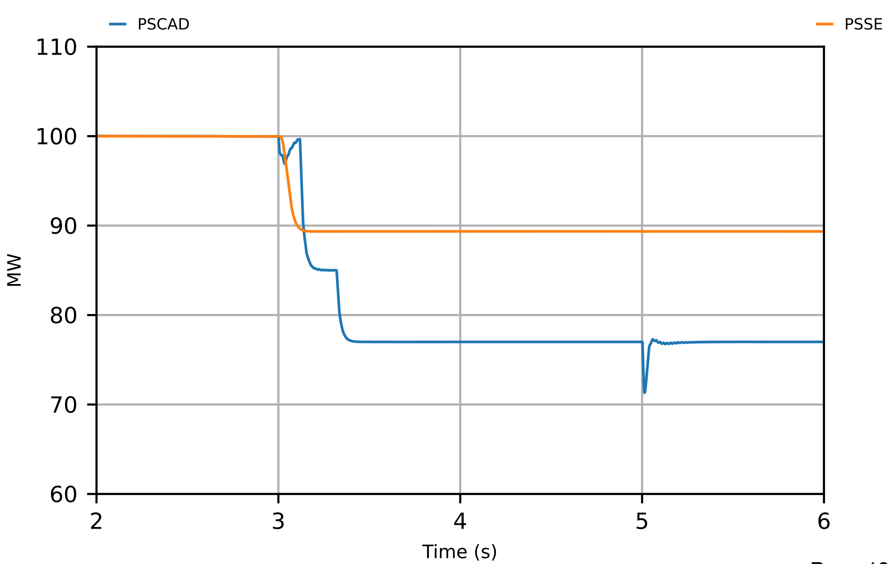
NSW DER Active Power



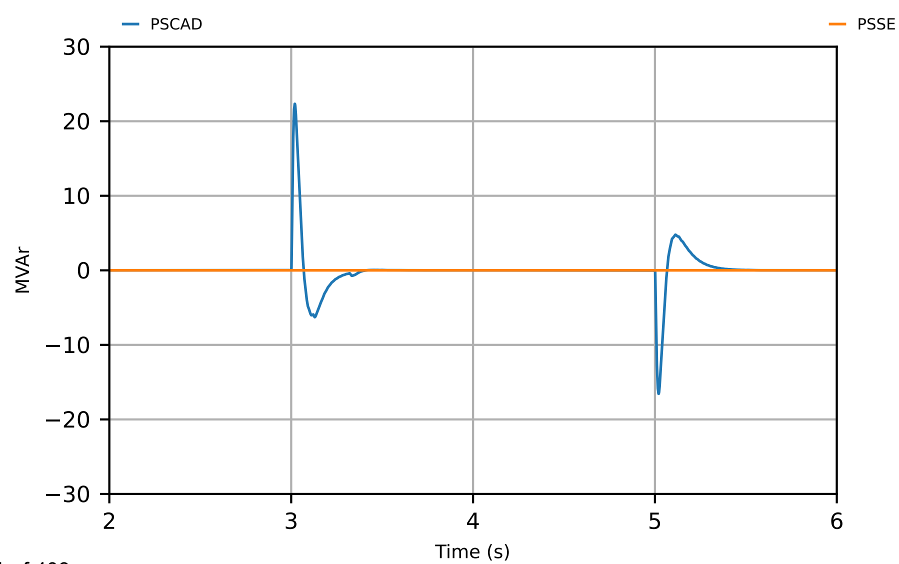
NSW DER Reactive Power



VIC DER Active Power

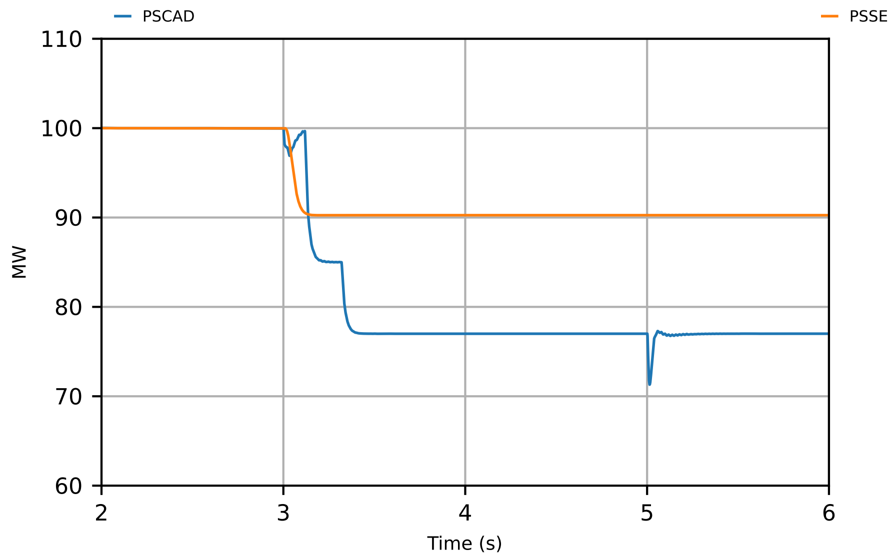


VIC DER Reactive Power

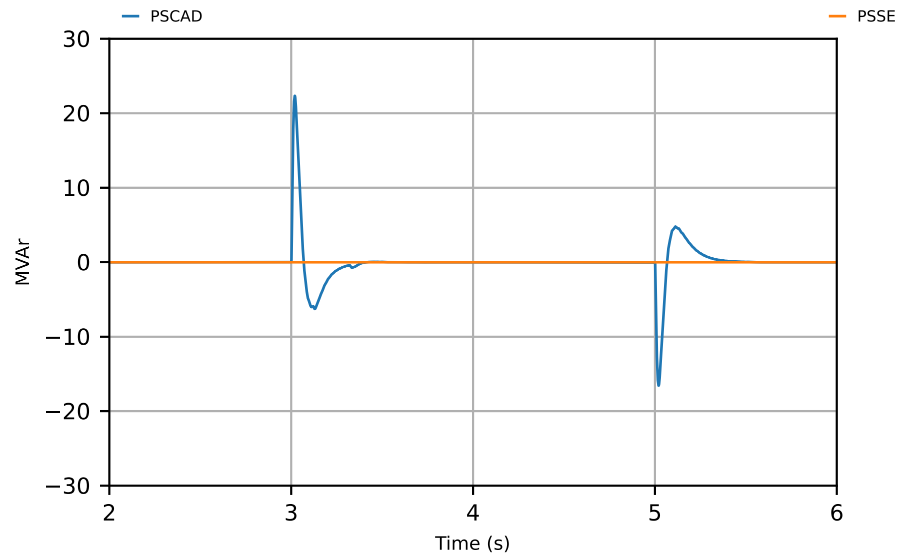


DER_SMIB_SCR_3_XR_3_T11_3

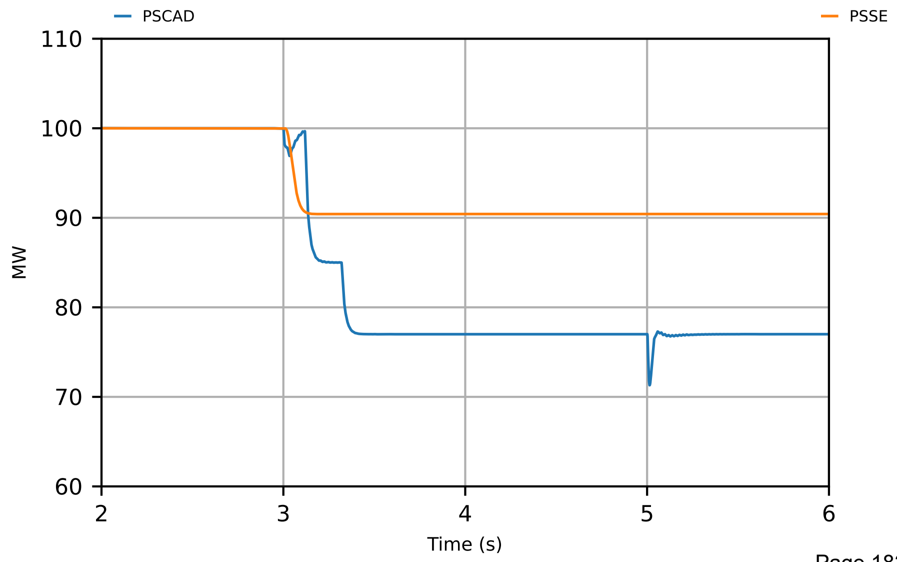
QLD DER Active Power



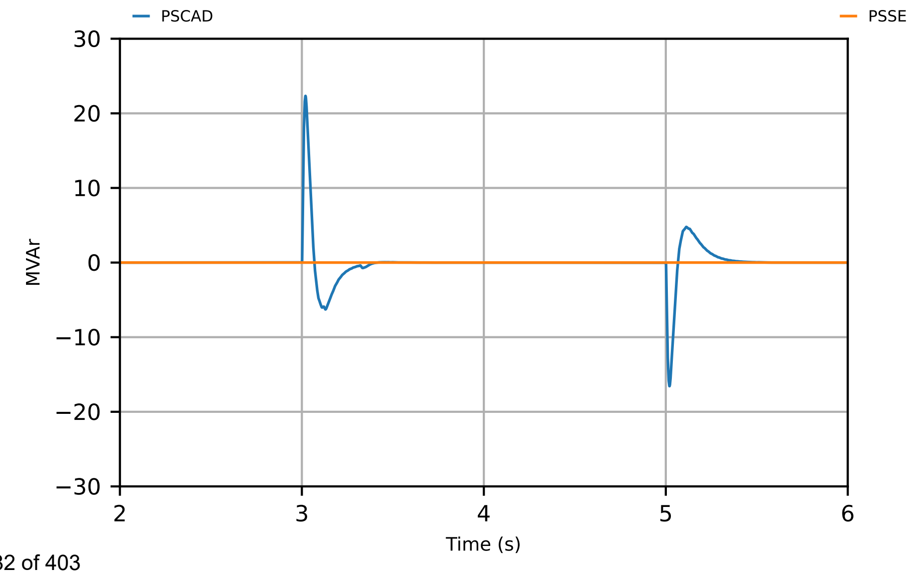
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power

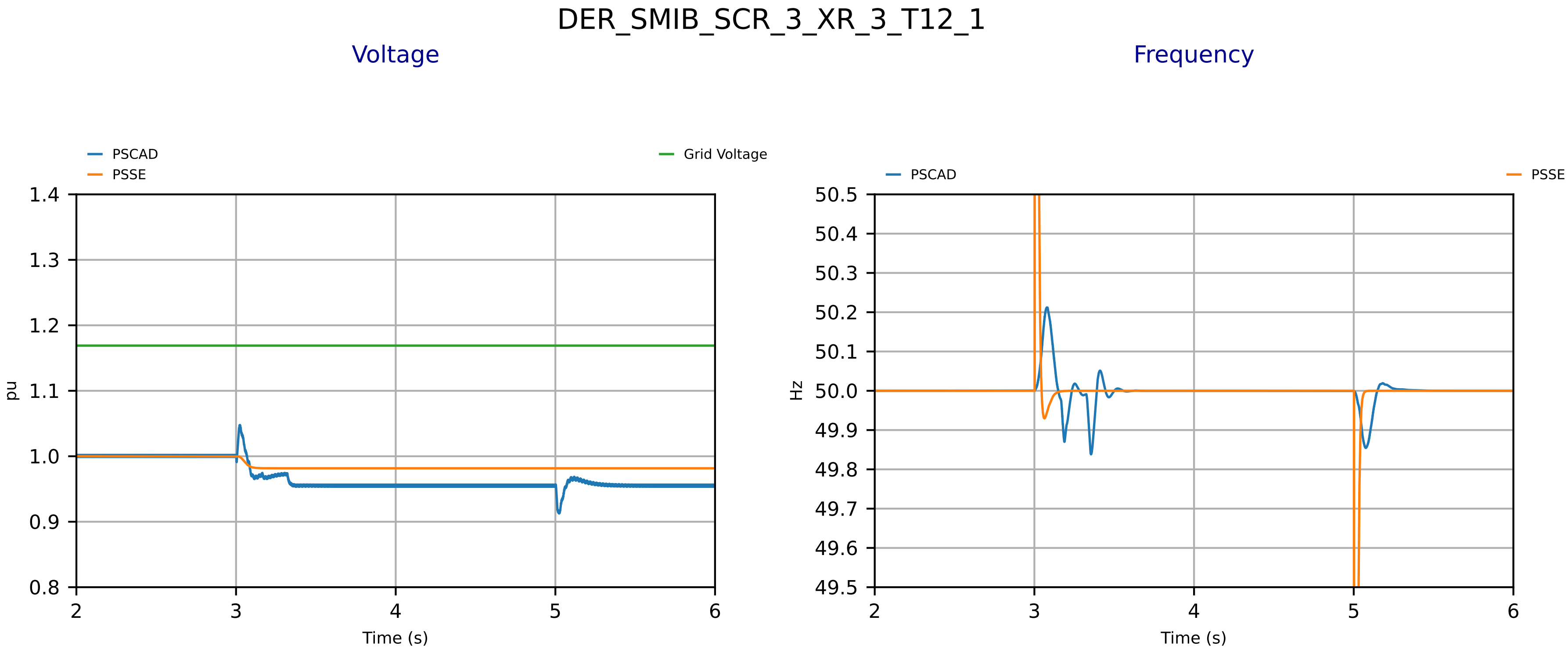


DER SMIB

SCR = 3, X/R = 3

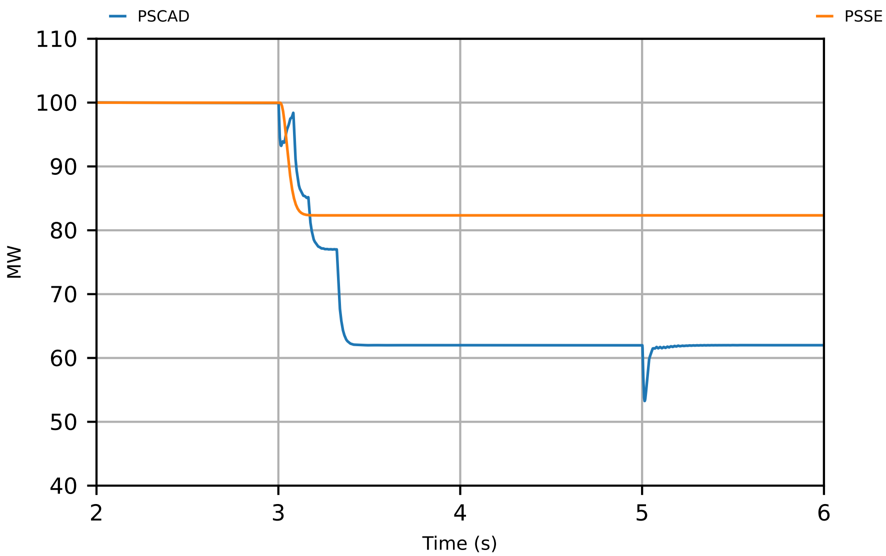
Test #12:

60° phase angle step

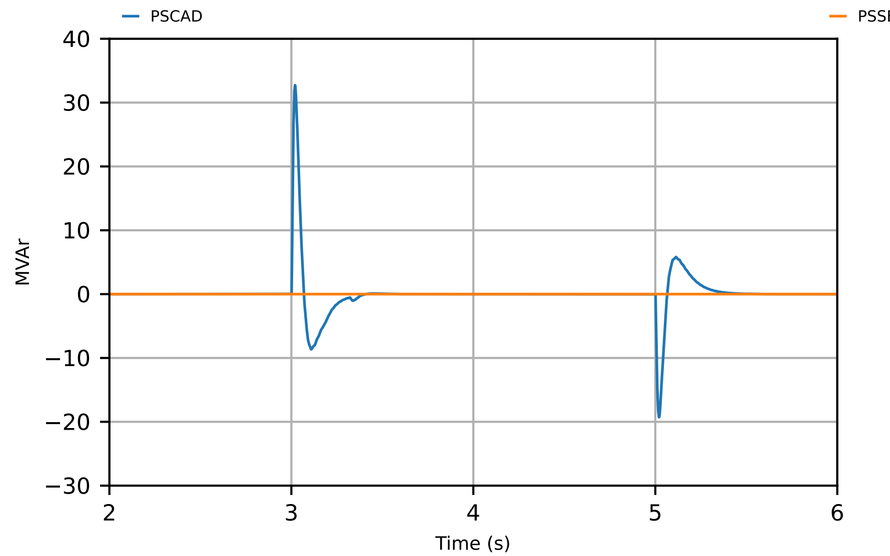

DER_SMIB_SCR_3_XR_3_T12_1
Voltage
PSCAD
PSSE
Grid Voltage
pu
1.4
1.3
1.2
1.1
1.0
0.9
0.8
2
3
4
5
6
Time (s)
Frequency
PSCAD
PSSE
Hz
50.5
50.4
50.3
50.2
50.1
50.0
49.9
49.8
49.7
49.6
49.5
2
3
4
5
6
Time (s)

DER_SMIB_SCR_3_XR_3_T12_2

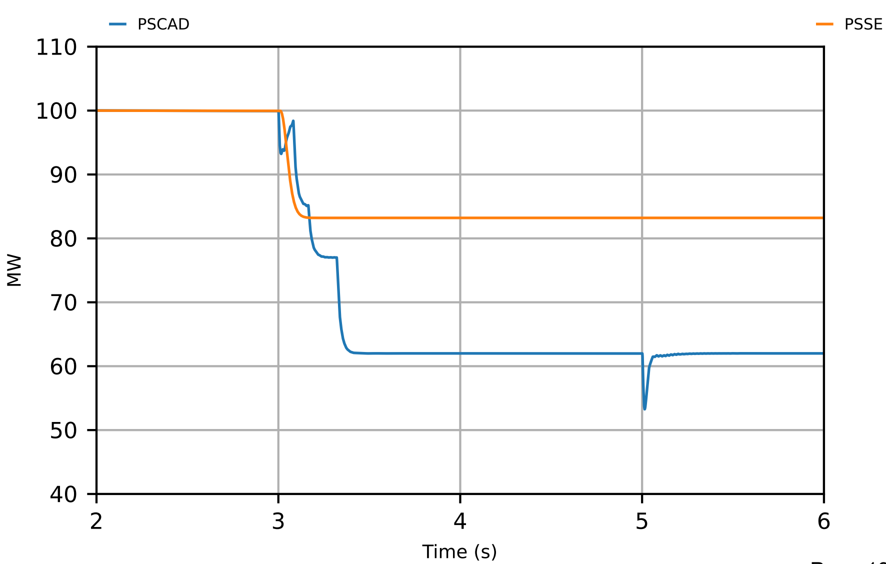
NSW DER Active Power



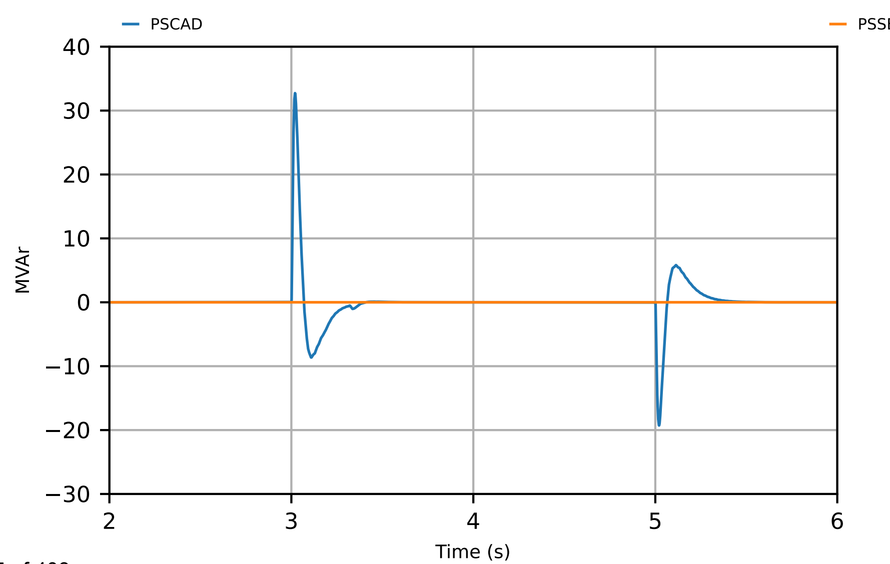
NSW DER Reactive Power



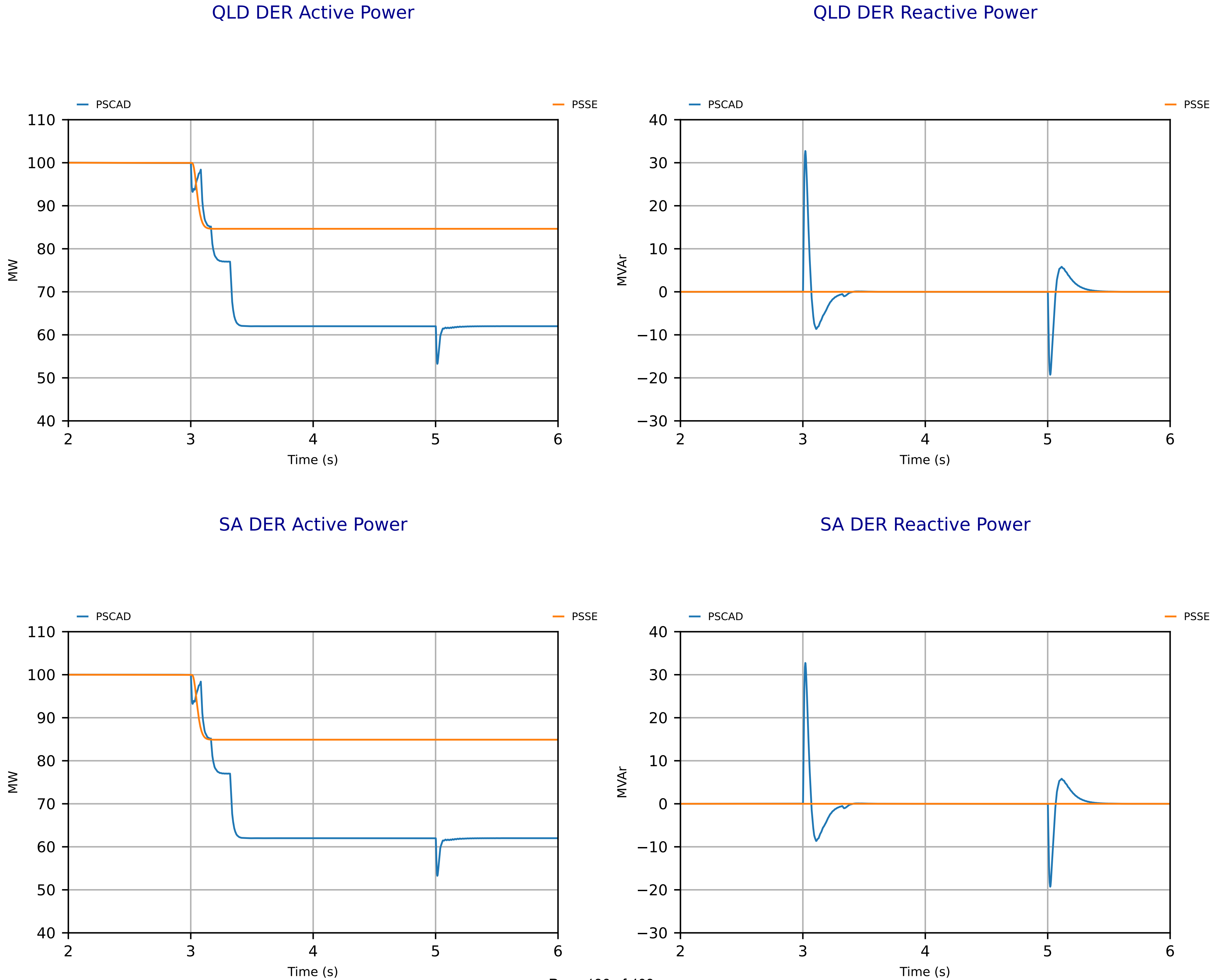
VIC DER Active Power



VIC DER Reactive Power



DER_SMIB_SCR_3_XR_3_T12_3



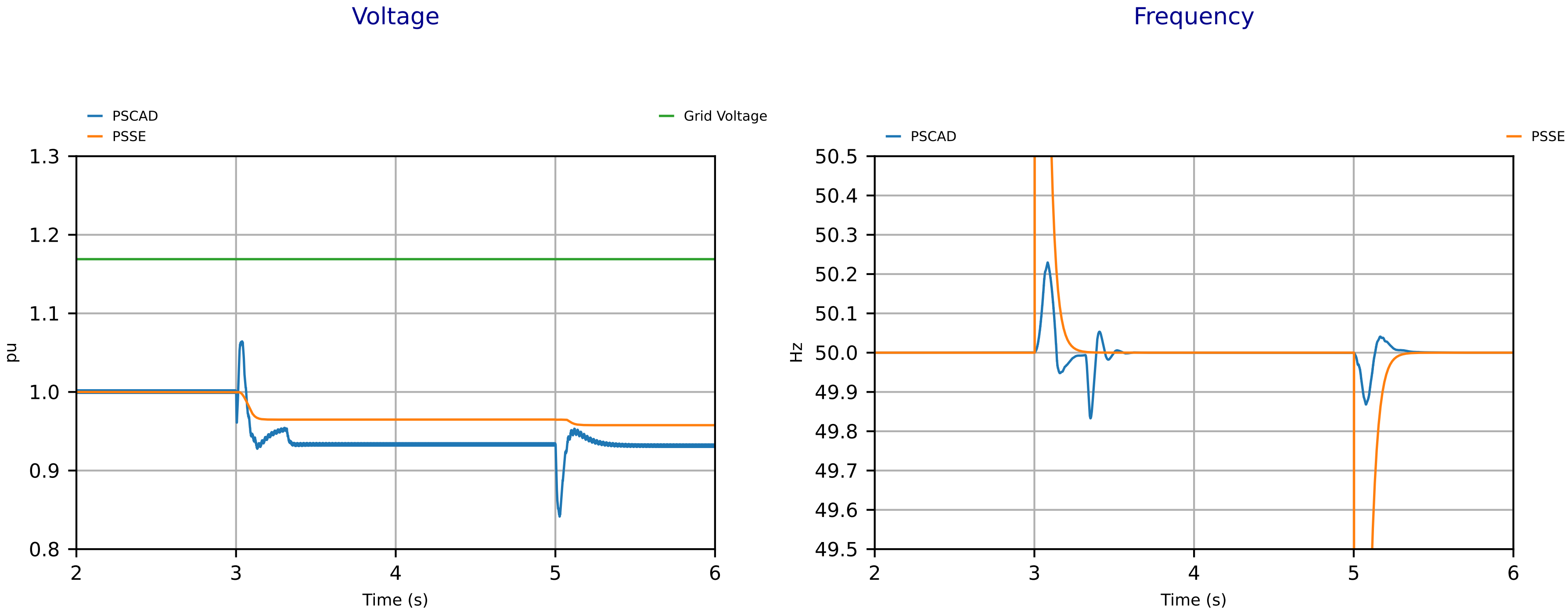
DER SMIB

SCR = 3, X/R = 3

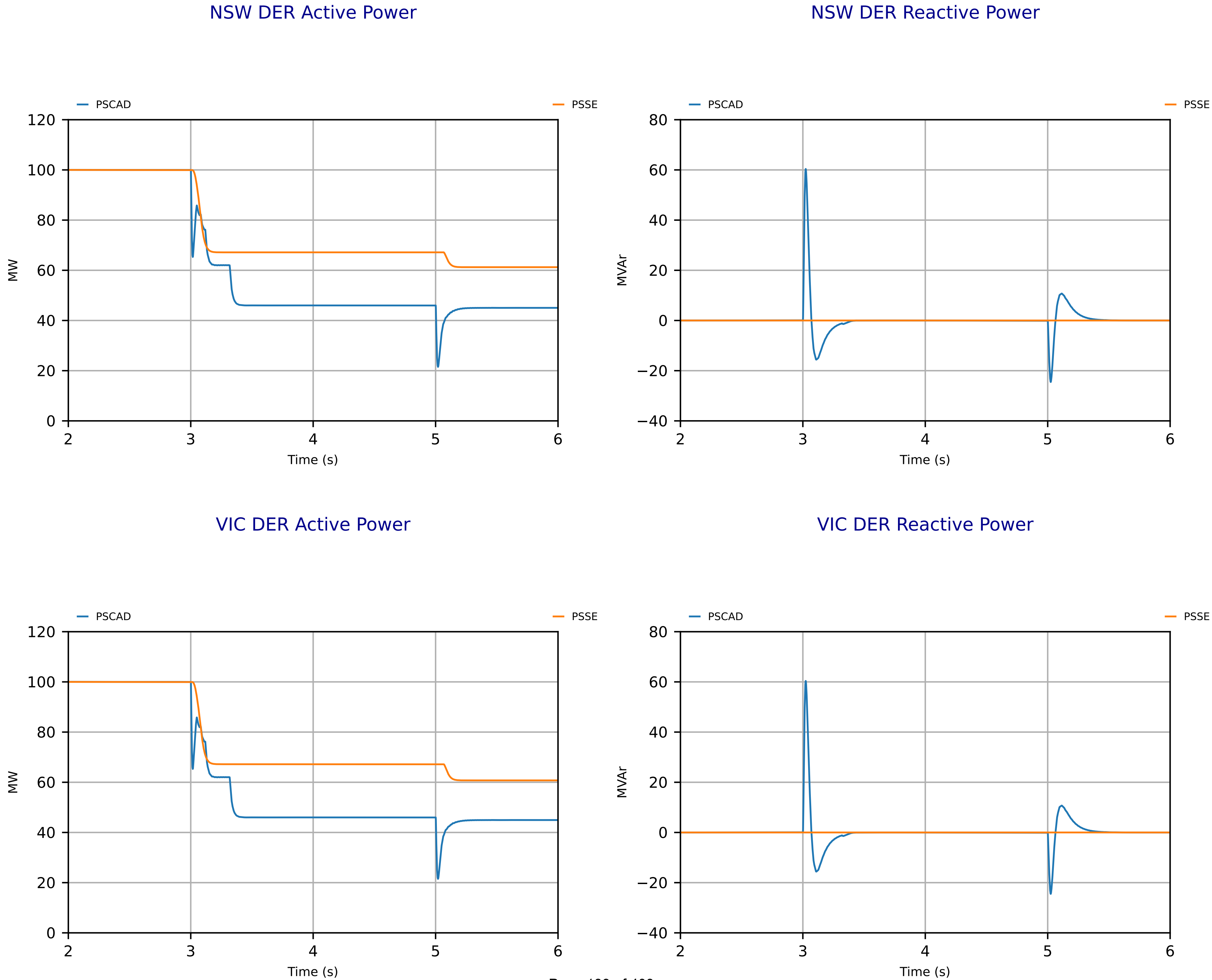
Test #13:

120° phase angle step

DER_SMIB_SCR_3_XR_3_T13_1

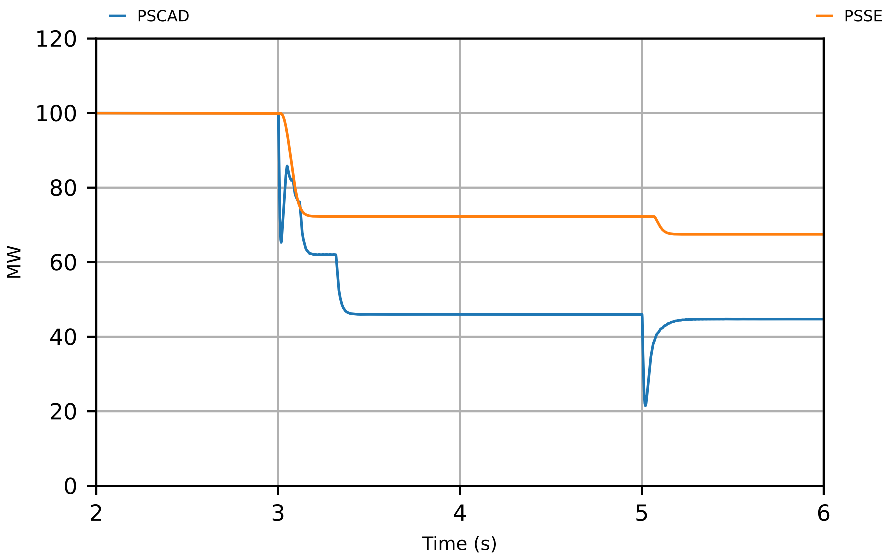


DER_SMIB_SCR_3_XR_3_T13_2

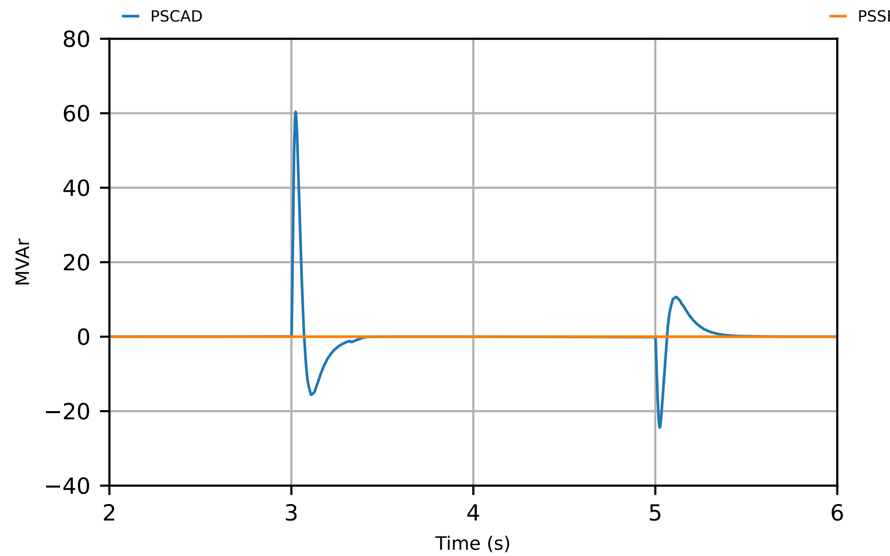


DER_SMIB_SCR_3_XR_3_T13_3

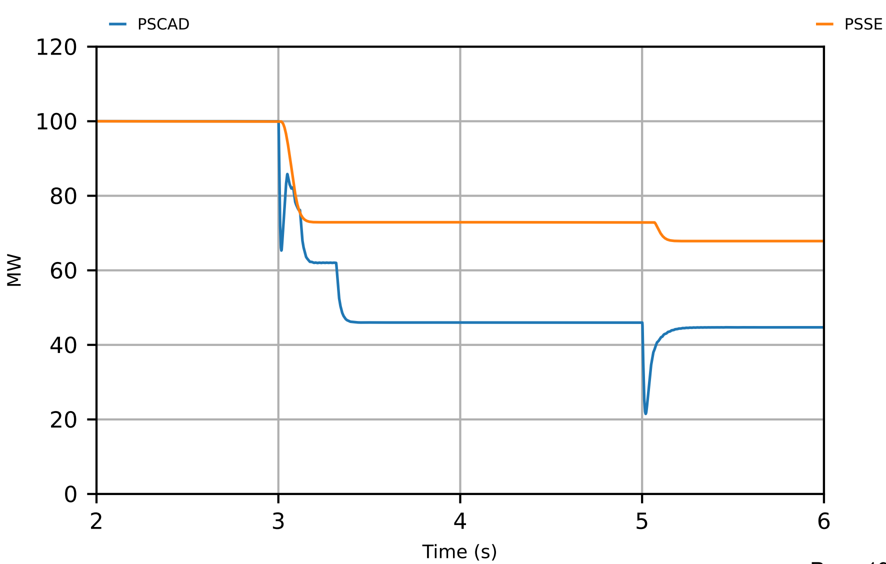
QLD DER Active Power



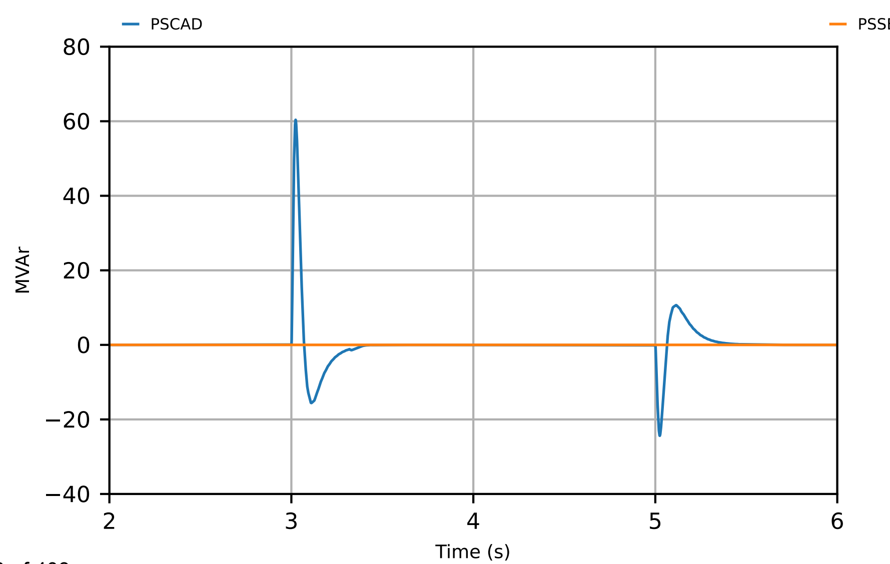
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



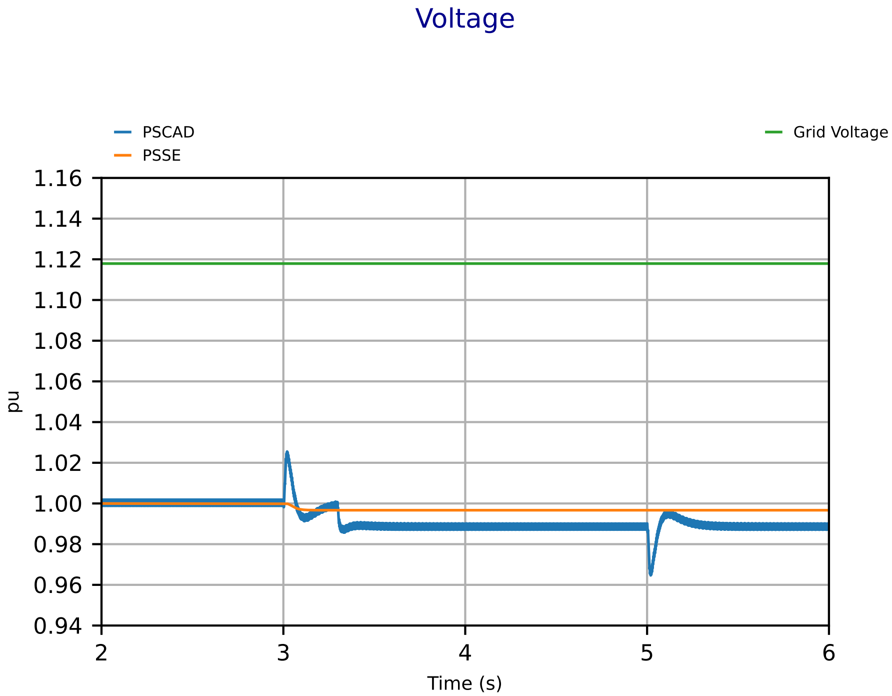
DER SMIB

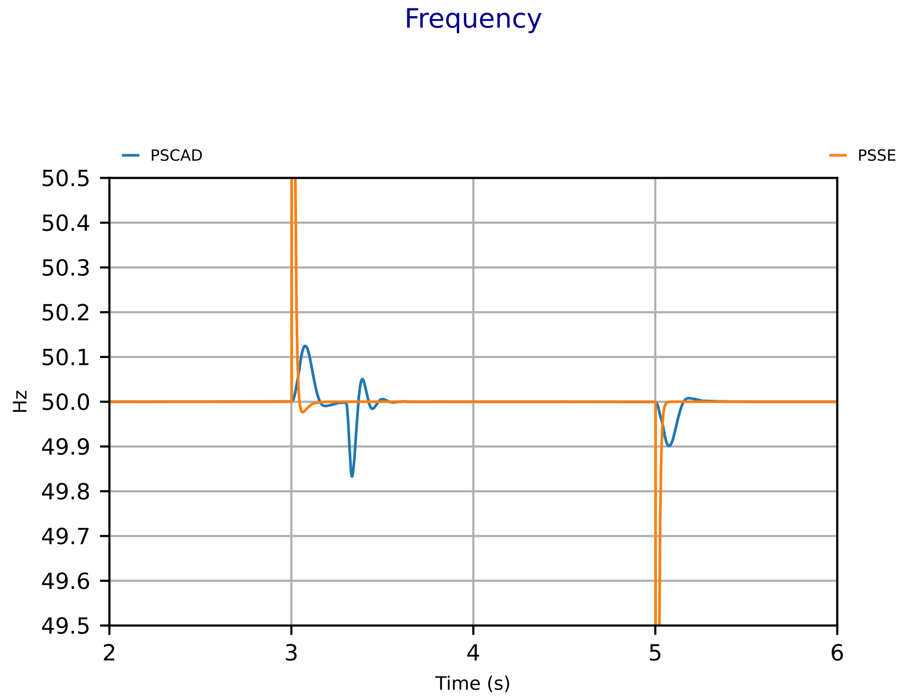
SCR = 3, X/R = 14

Test #10:

20° phase angle step

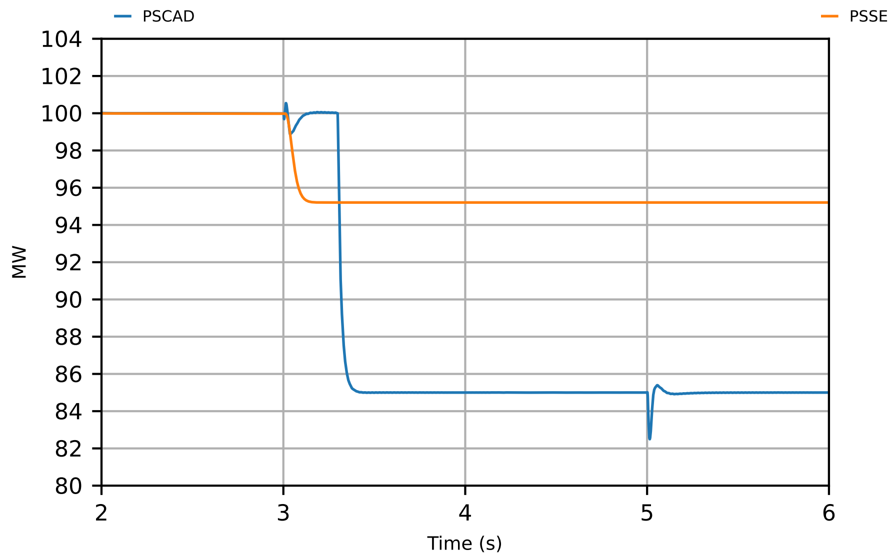
DER_SMIB_SCR_3_XR_14_T10_1



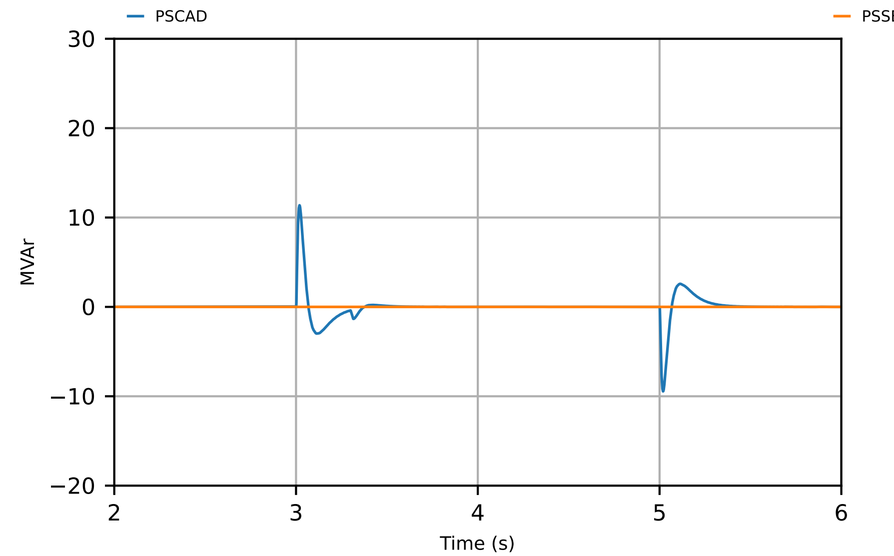


DER_SMIB_SCR_3_XR_14_T10_2

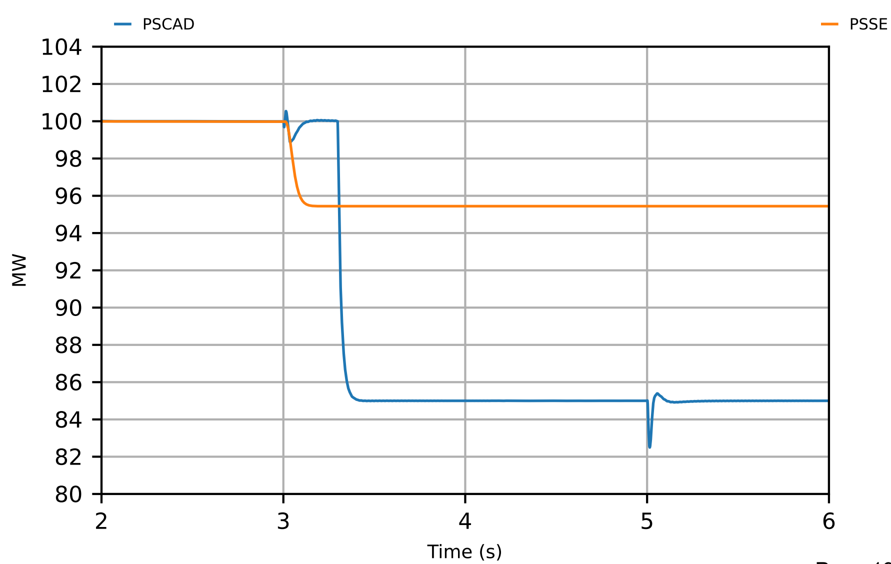
NSW DER Active Power



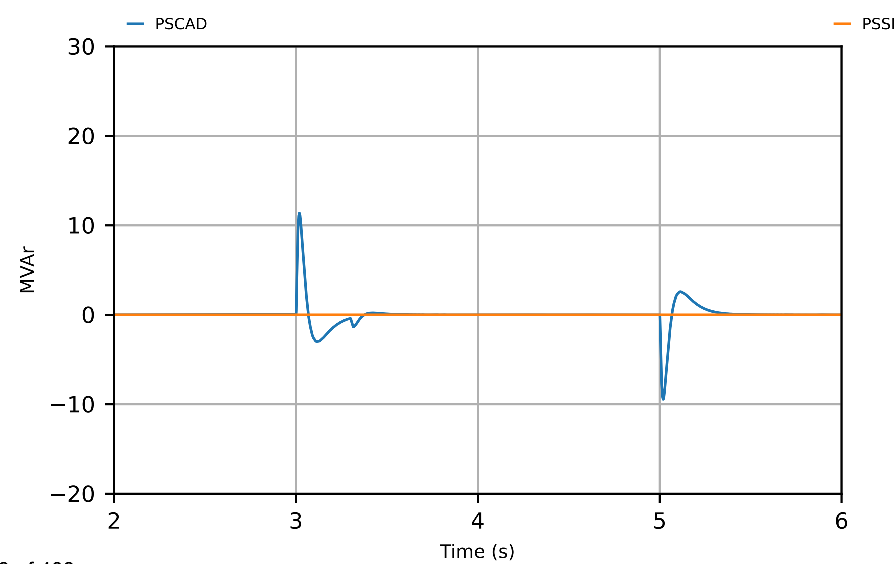
NSW DER Reactive Power



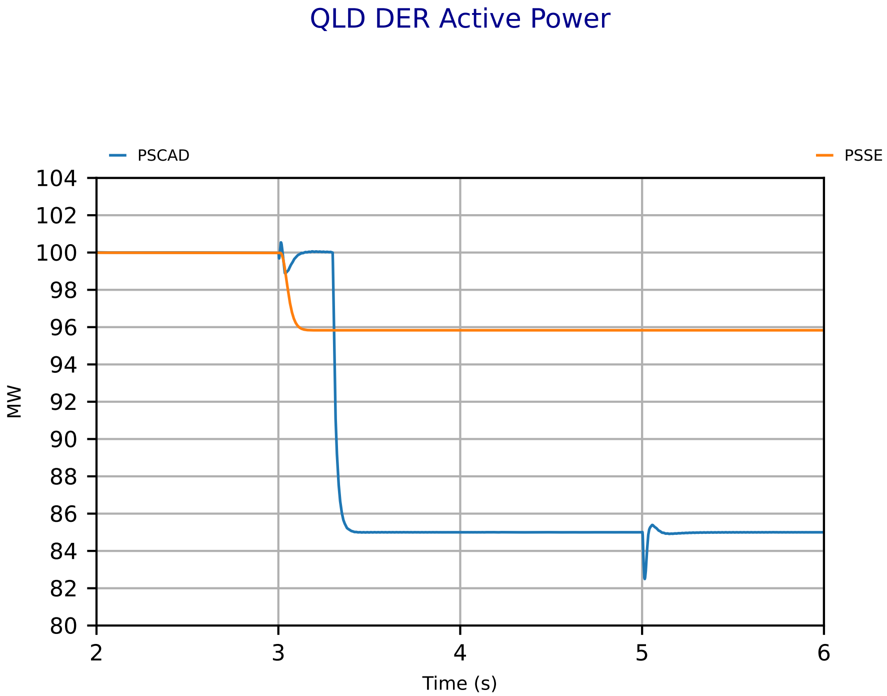
VIC DER Active Power

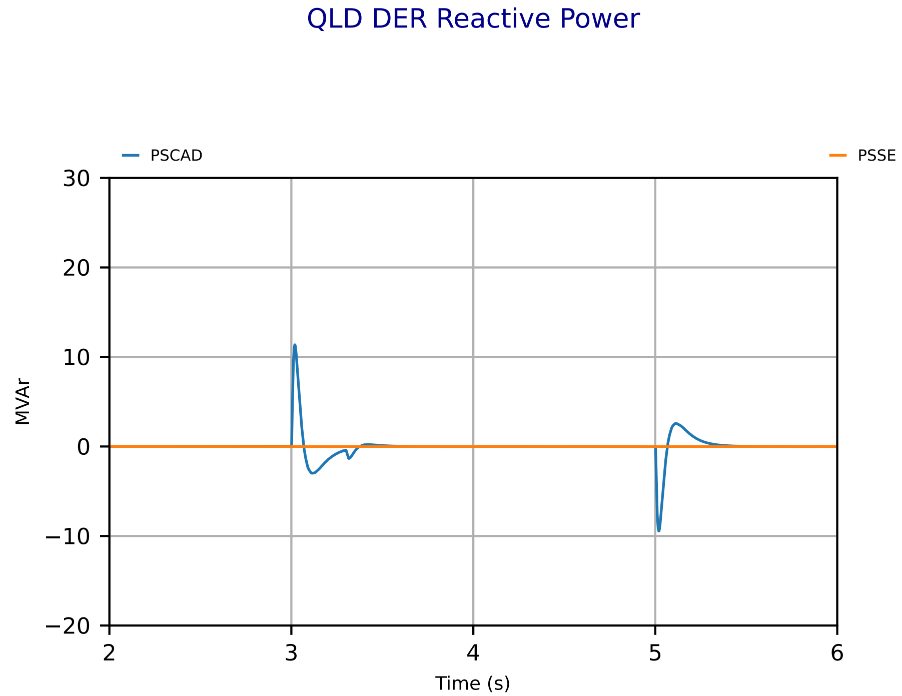


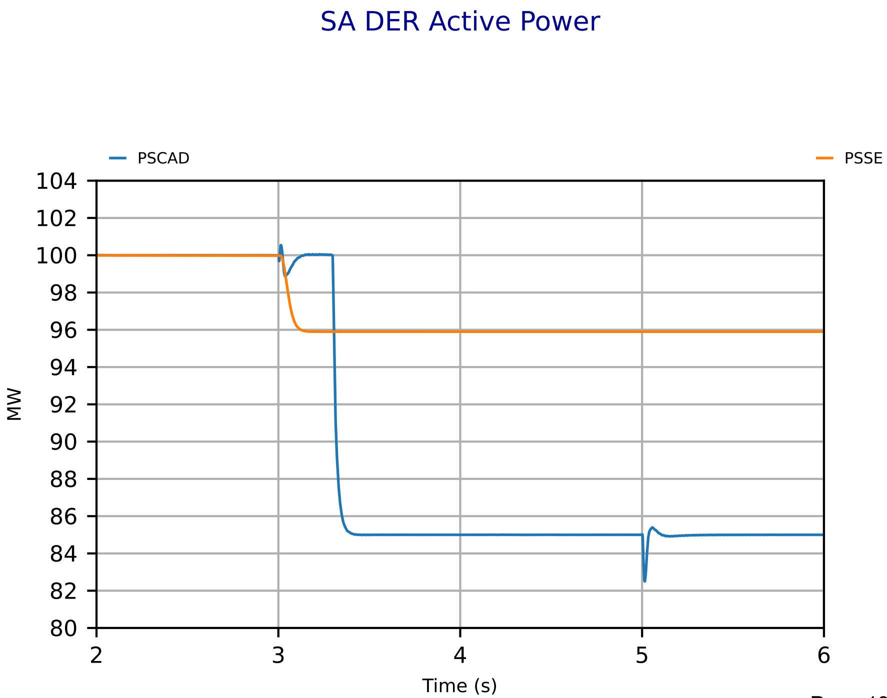
VIC DER Reactive Power

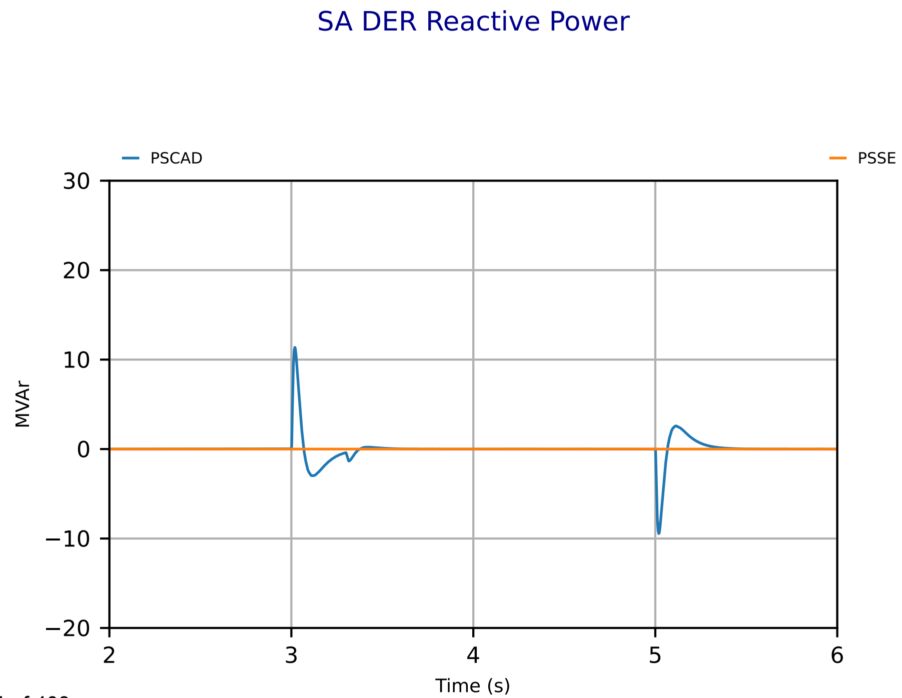


DER_SMIB_SCR_3_XR_14_T10_3









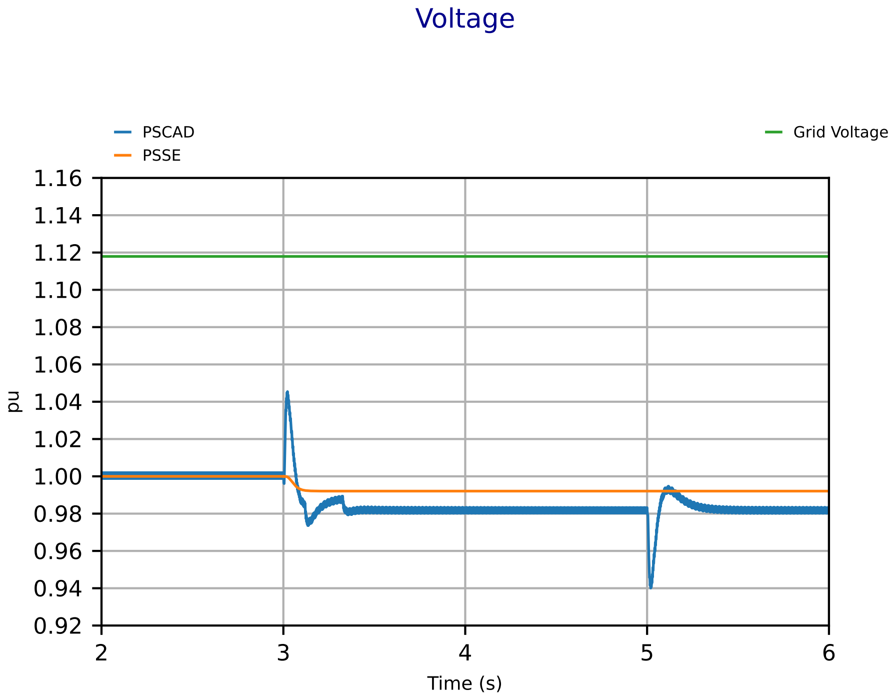
DER SMIB

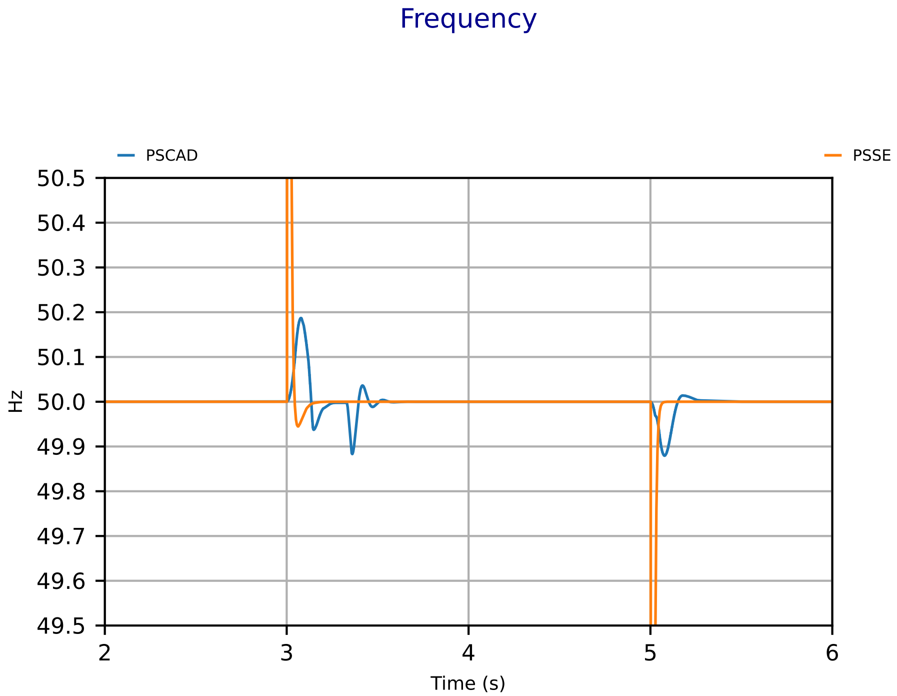
SCR = 3, X/R = 14

Test #11:

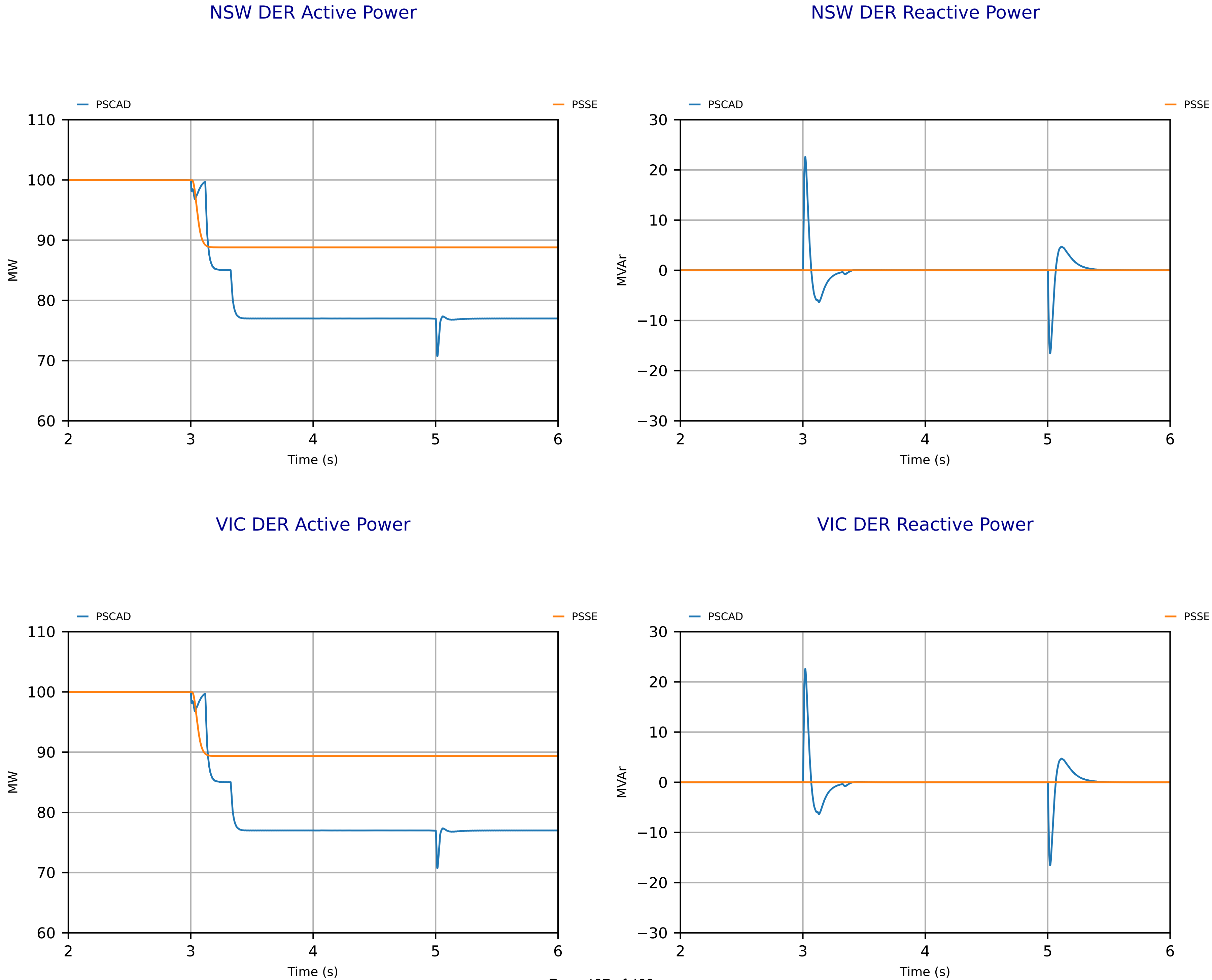
40° phase angle step

DER_SMIB_SCR_3_XR_14_T11_1

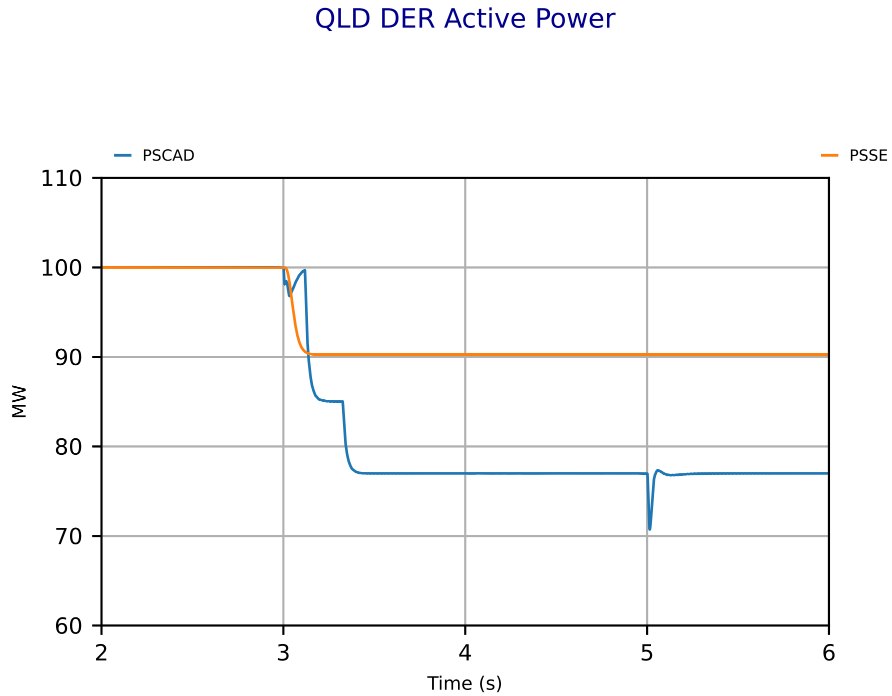


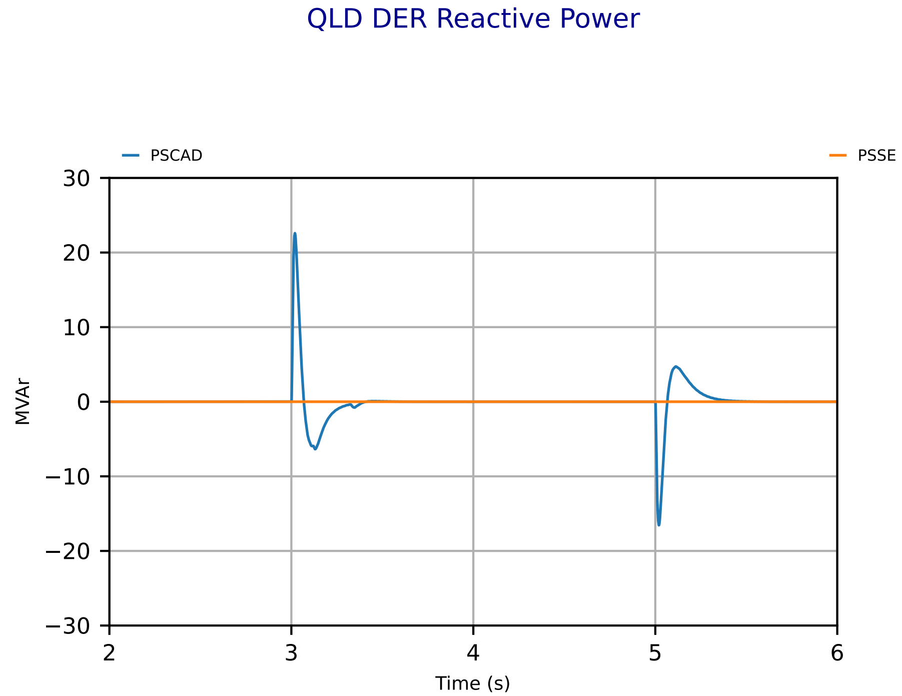


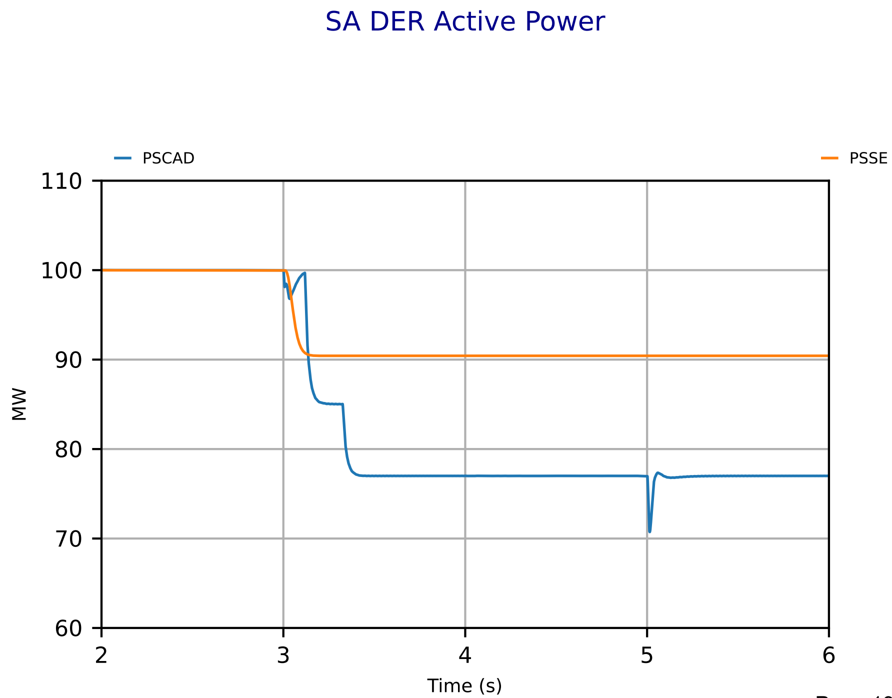
DER_SMIB_SCR_3_XR_14_T11_2

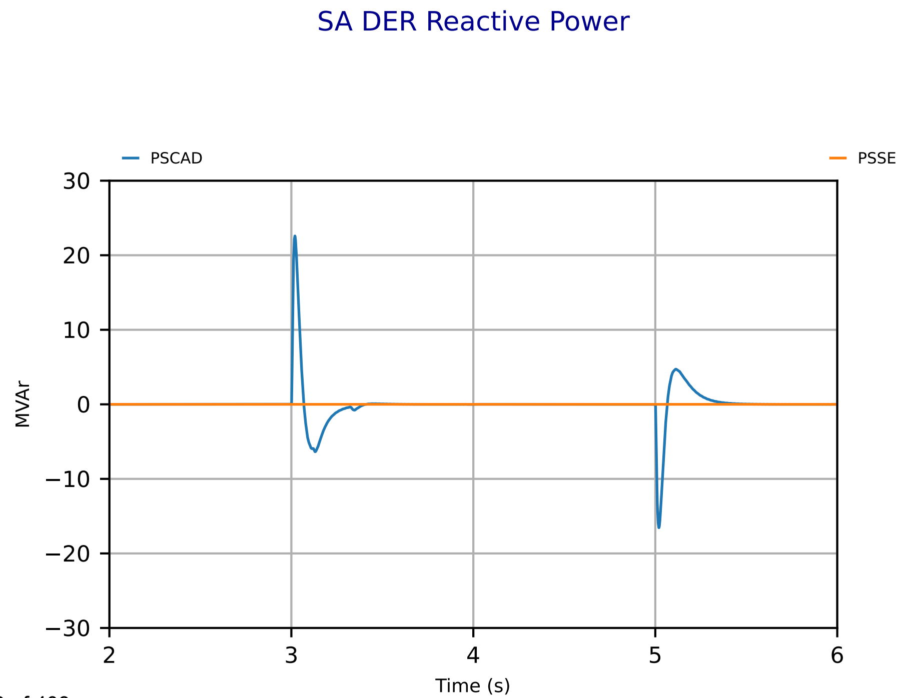


DER_SMIB_SCR_3_XR_14_T11_3









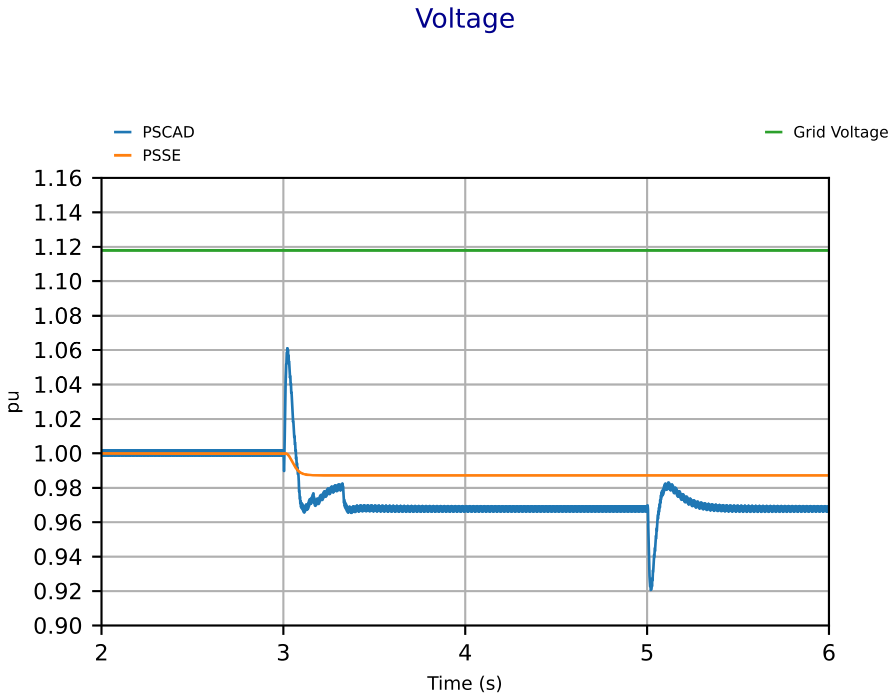
DER SMIB

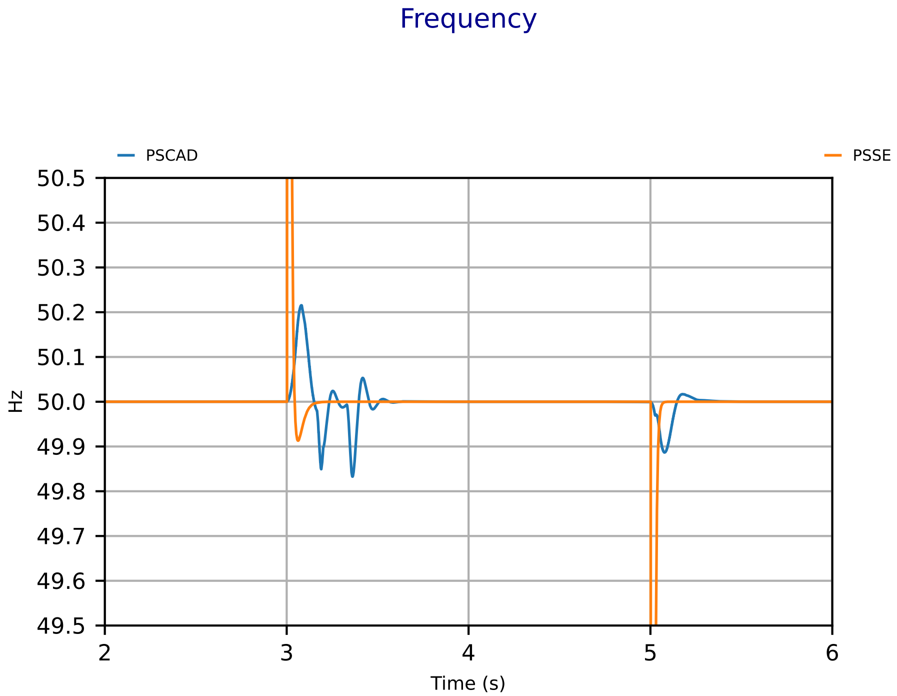
SCR = 3, X/R = 14

Test #12:

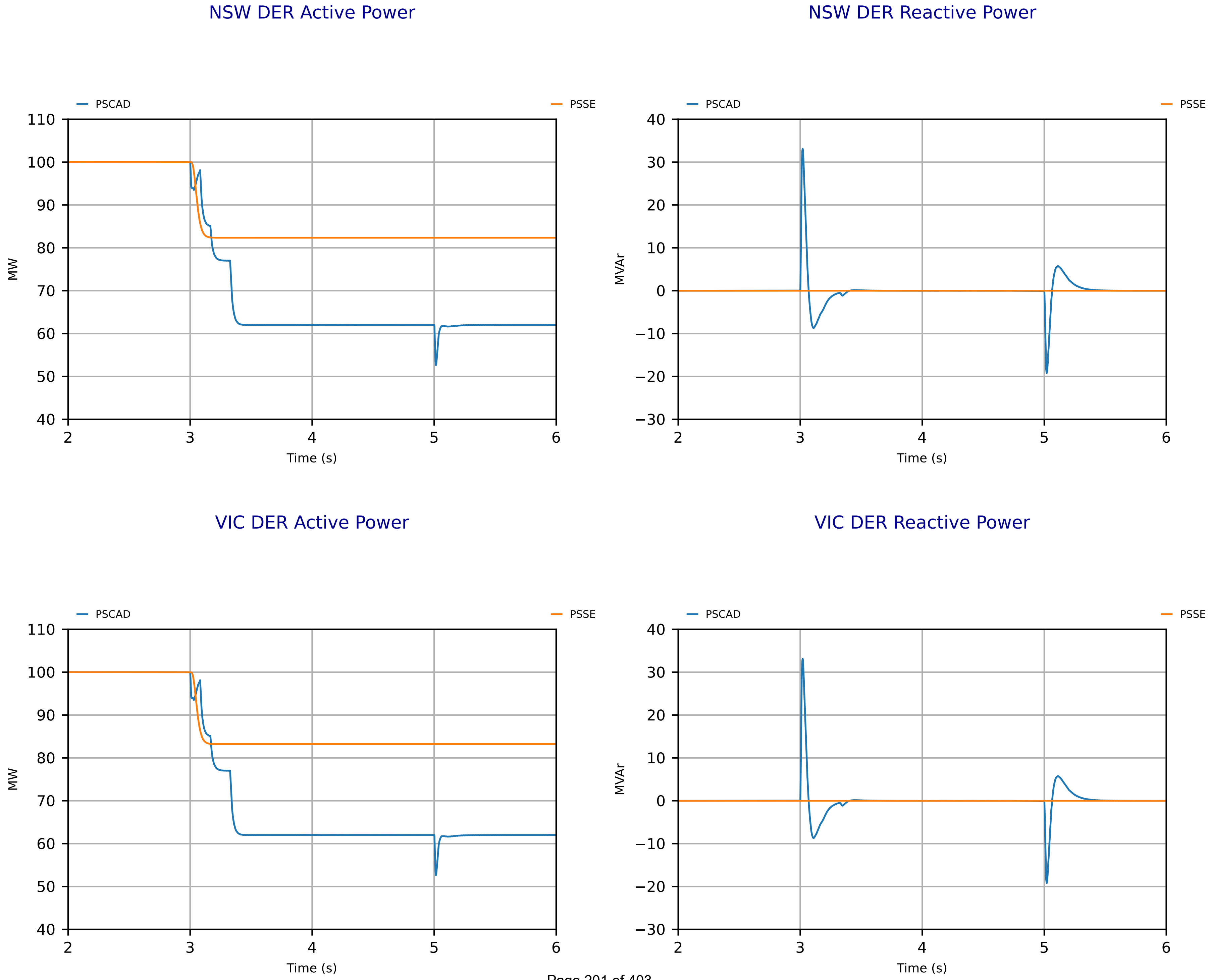
60° phase angle step

DER_SMIB_SCR_3_XR_14_T12_1

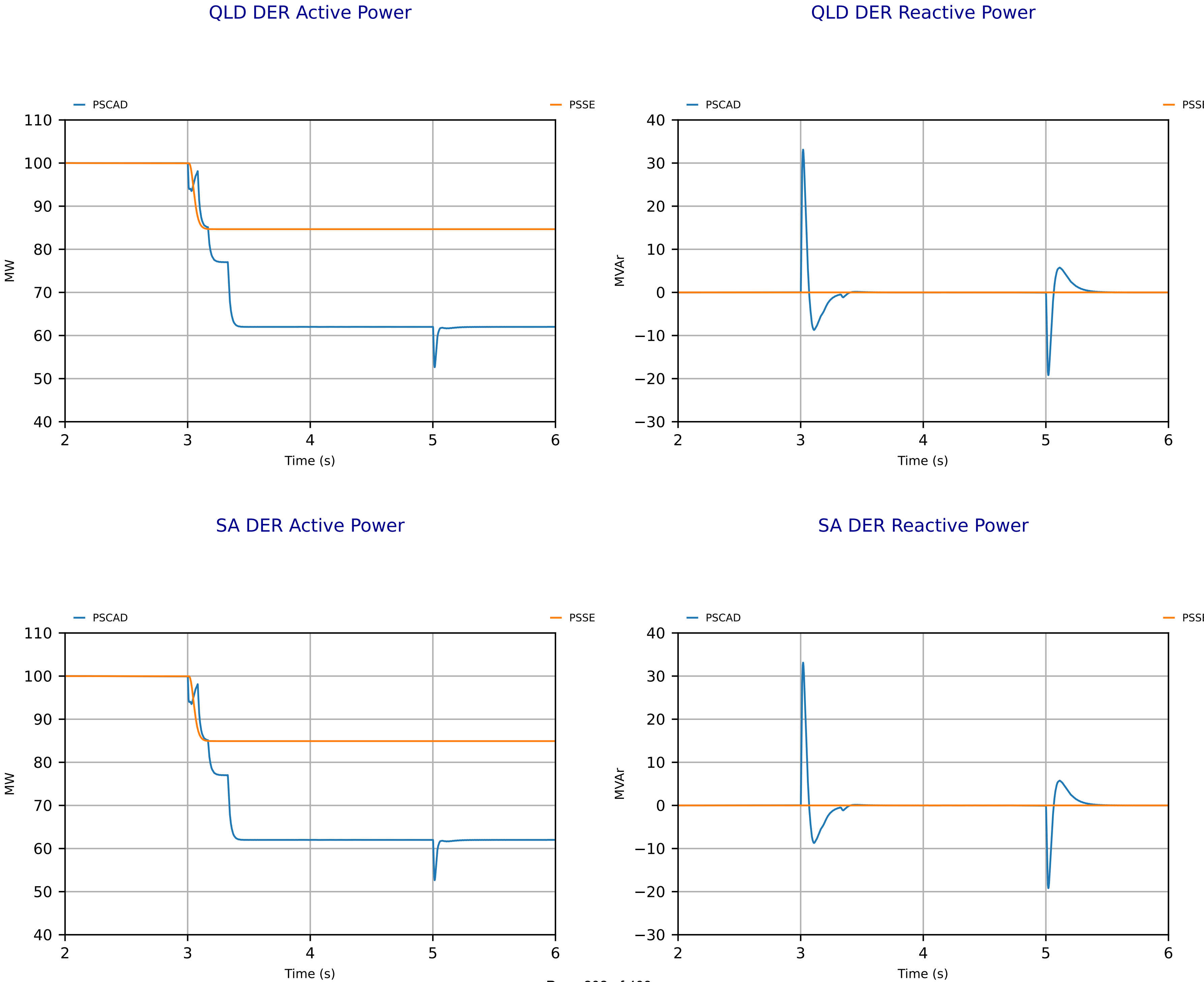




DER_SMIB_SCR_3_XR_14_T12_2



DER_SMIB_SCR_3_XR_14_T12_3



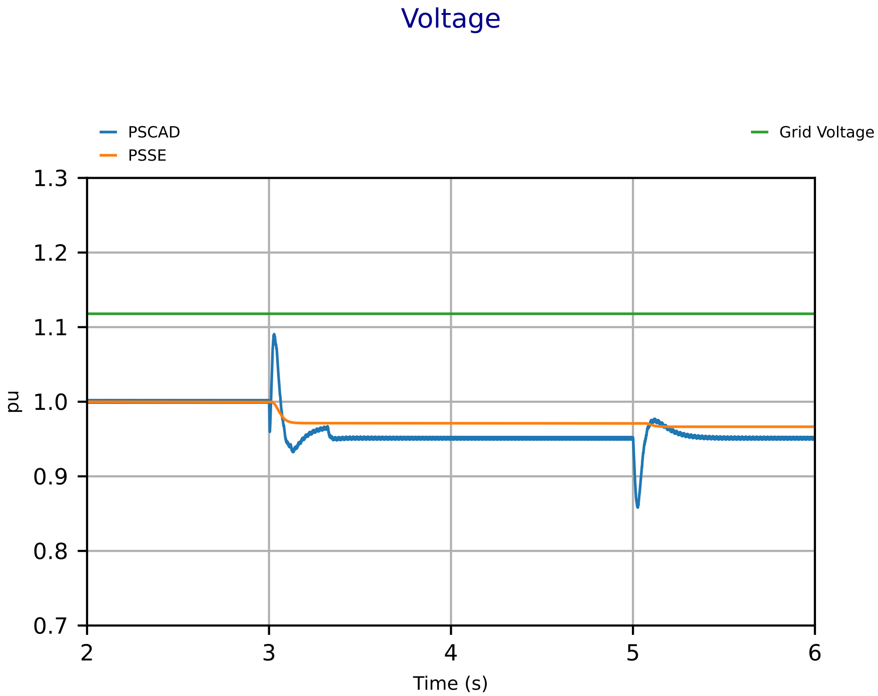
DER SMIB

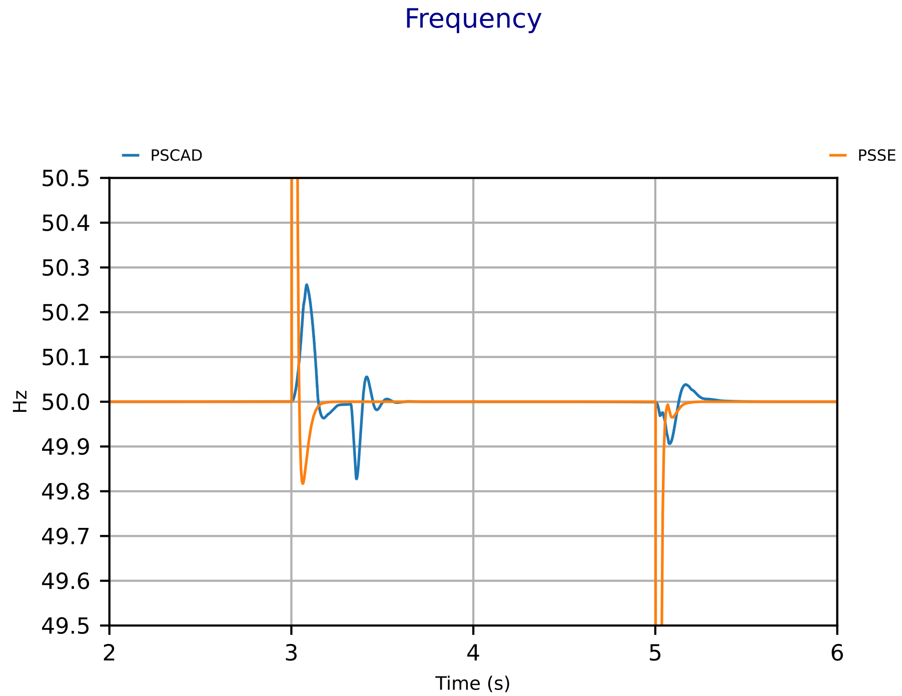
SCR = 3, X/R = 14

Test #13:

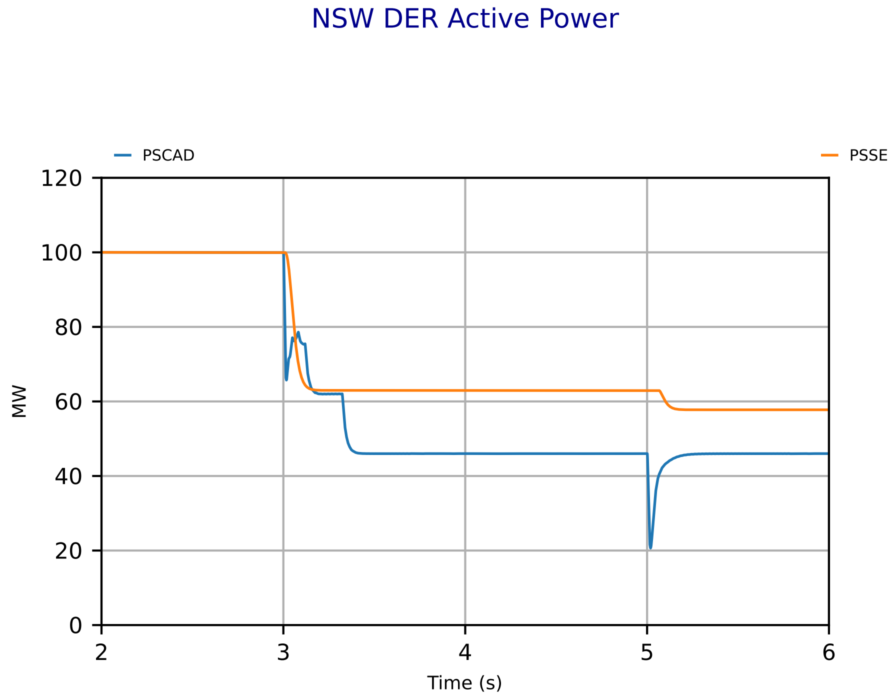
120° phase angle step

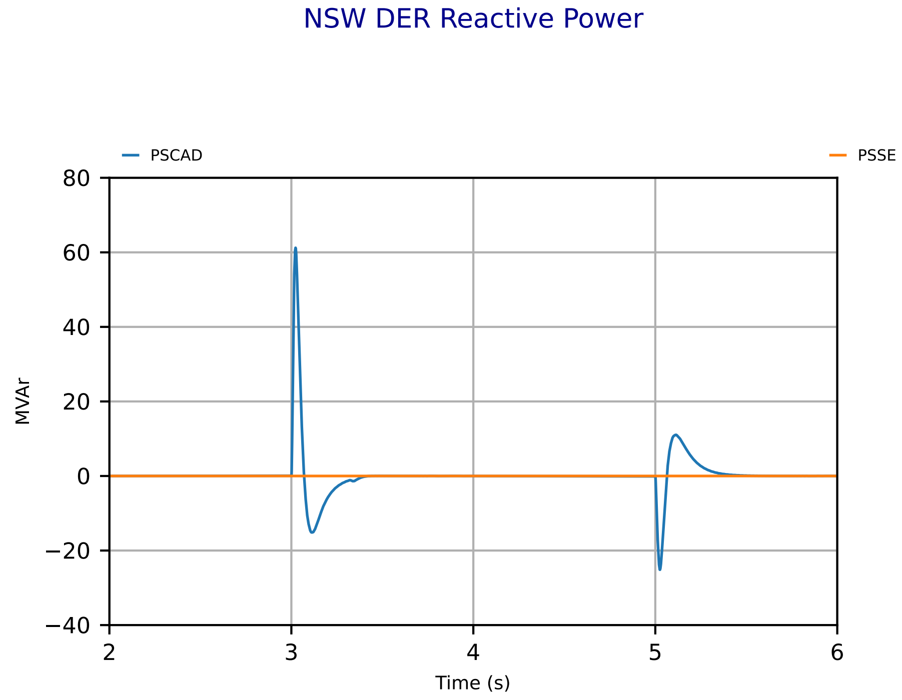
DER_SMIB_SCR_3_XR_14_T13_1

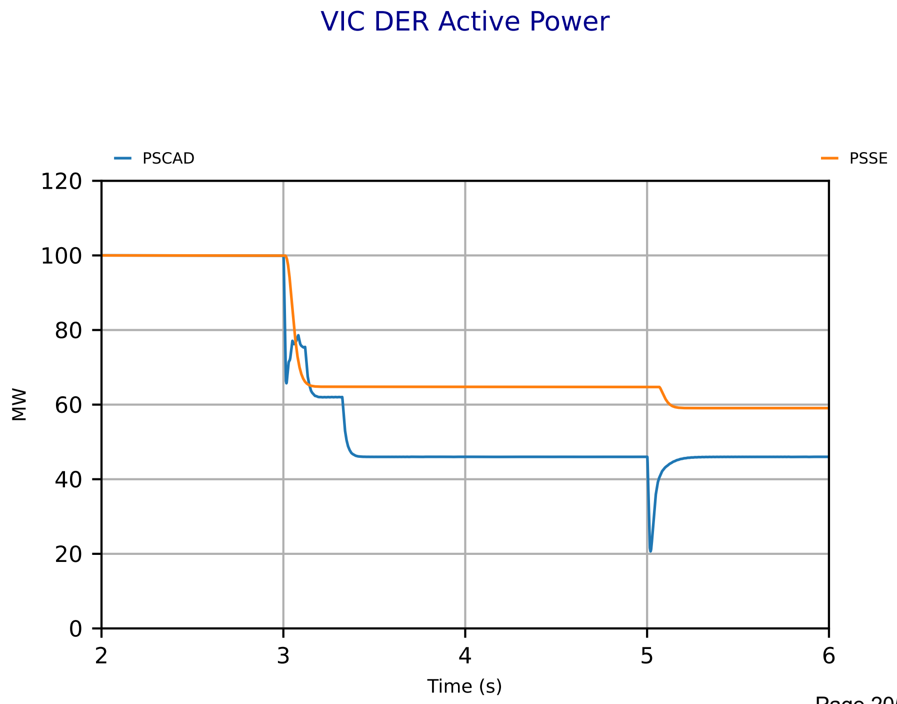


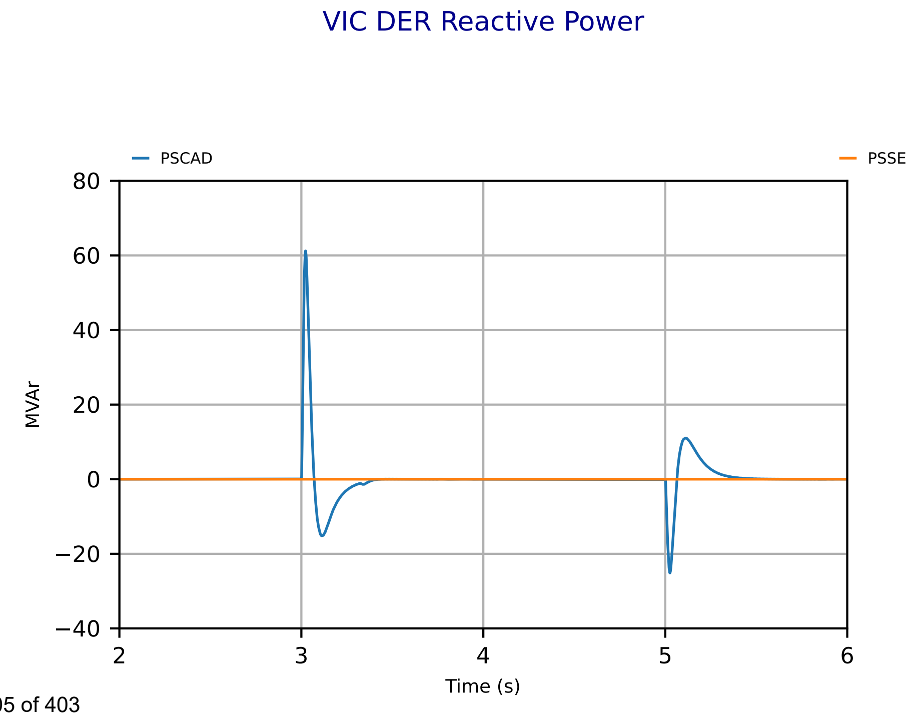


DER_SMIB_SCR_3_XR_14_T13_2

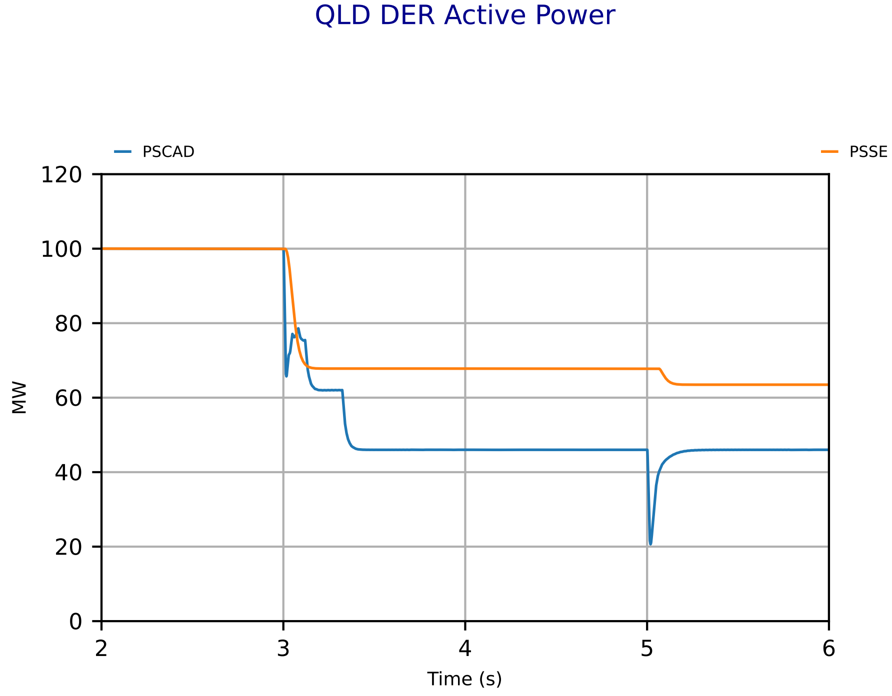


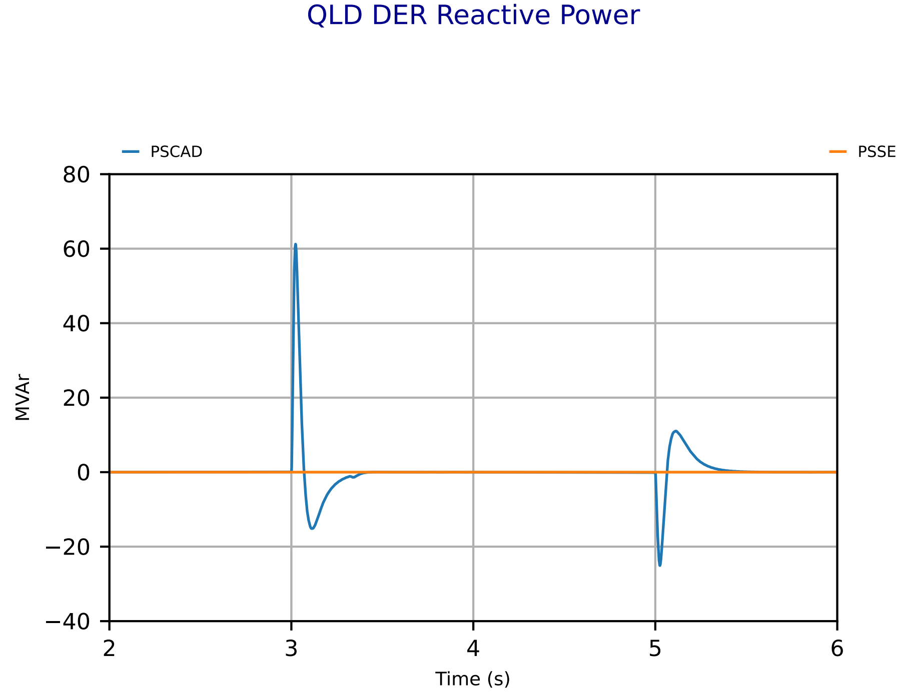


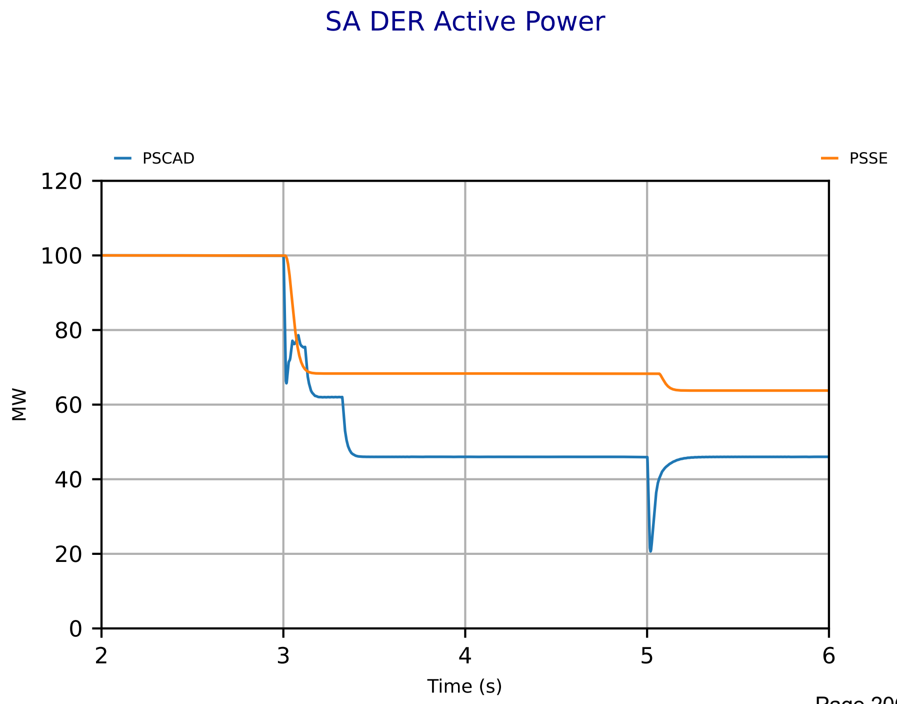


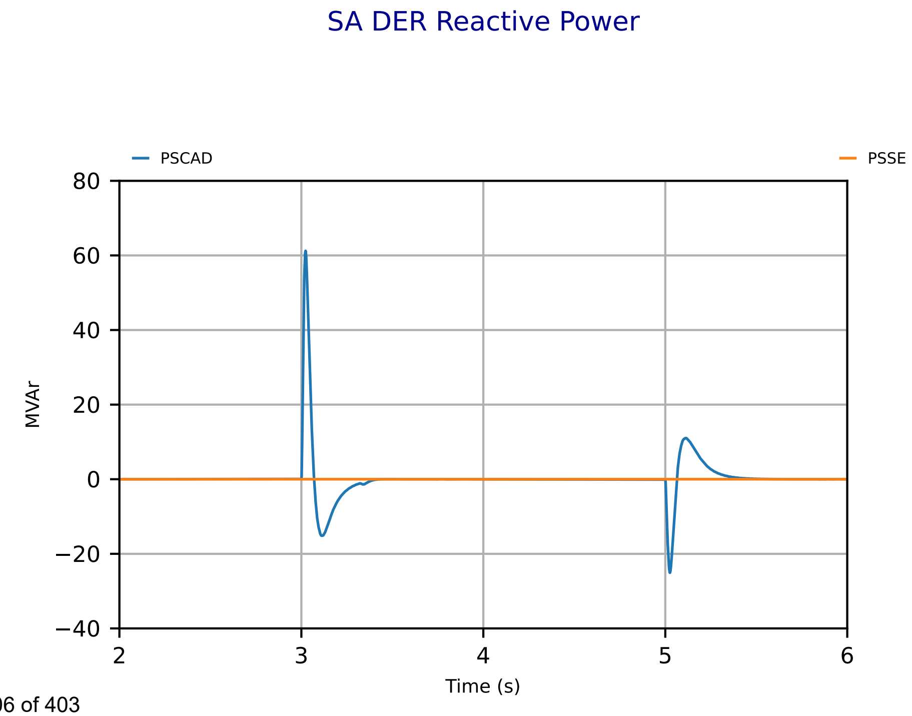


DER_SMIB_SCR_3_XR_14_T13_3









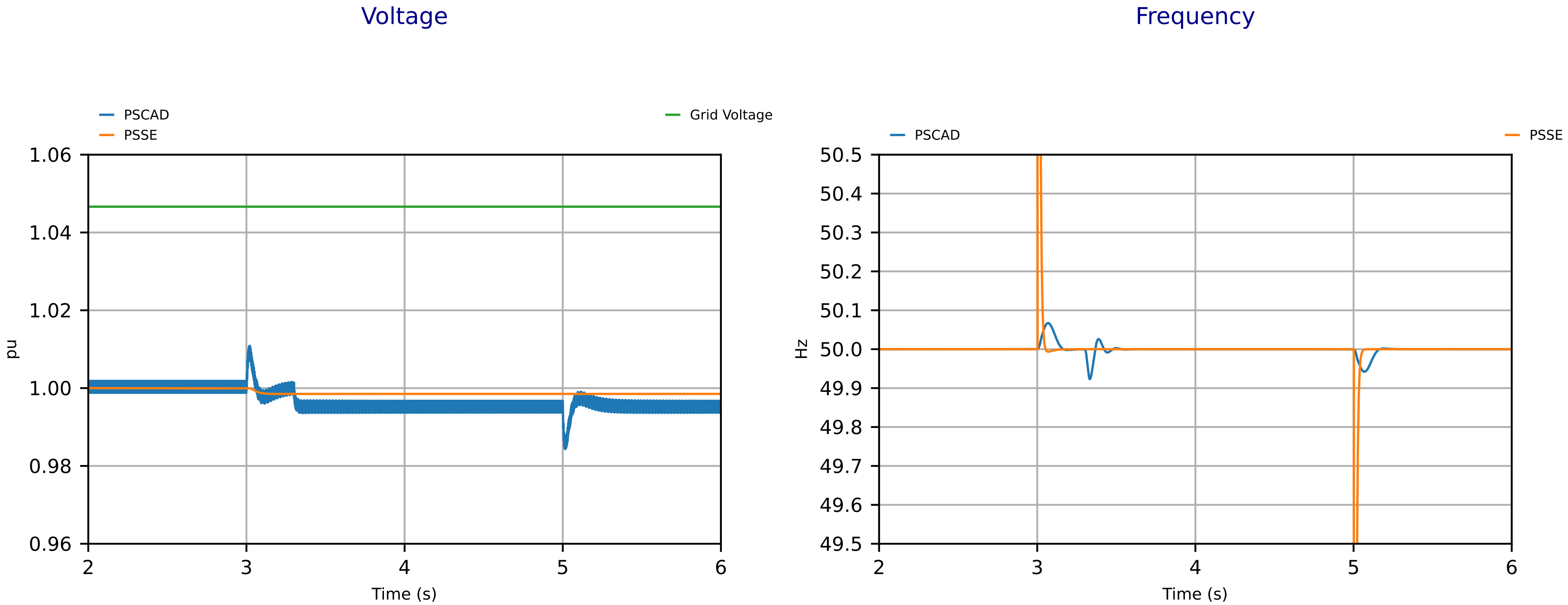
DER SMIB

SCR = 10, X/R = 3

Test #10:

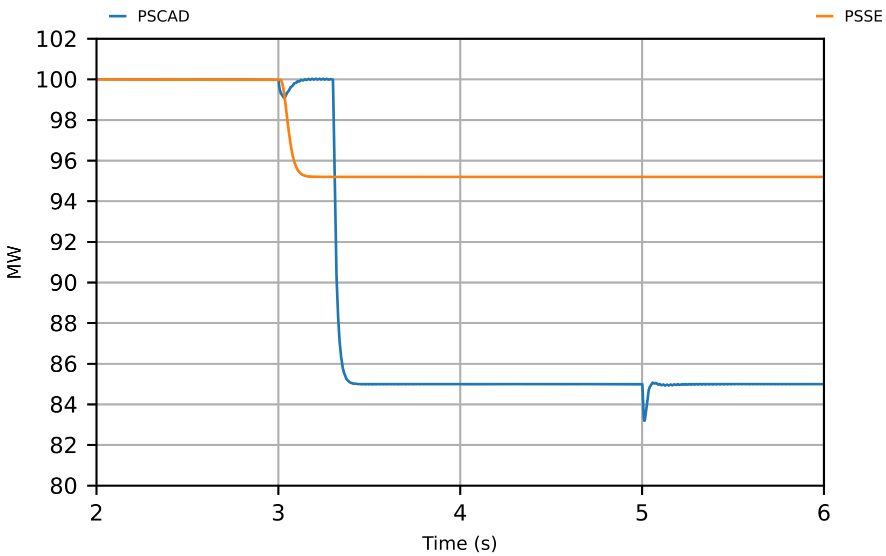
20° phase angle step

DER_SMIB_SCR_10_XR_3_T10_1

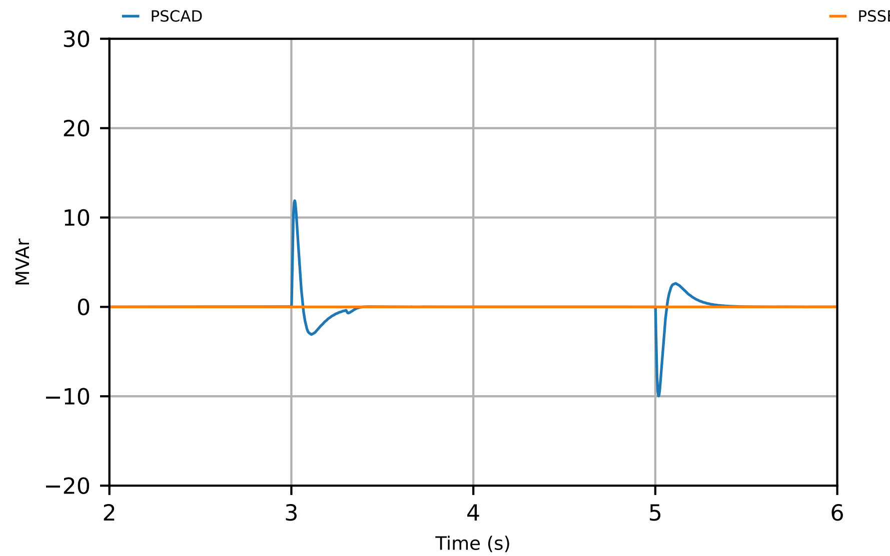


DER_SMIB_SCR_10_XR_3_T10_2

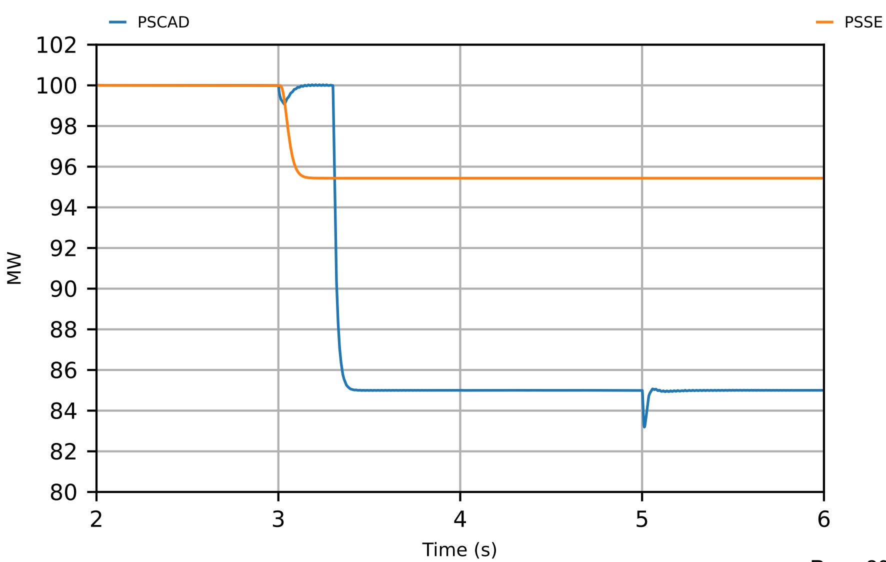
NSW DER Active Power



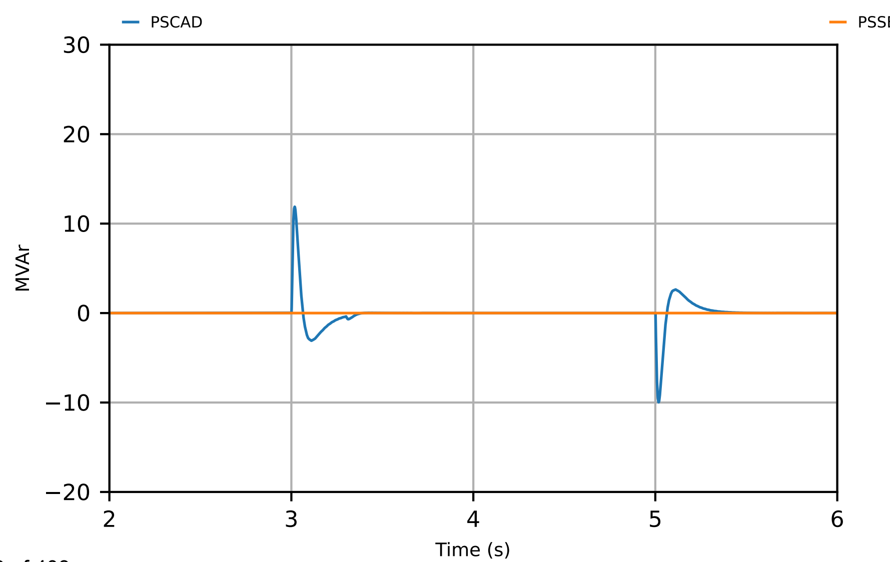
NSW DER Reactive Power



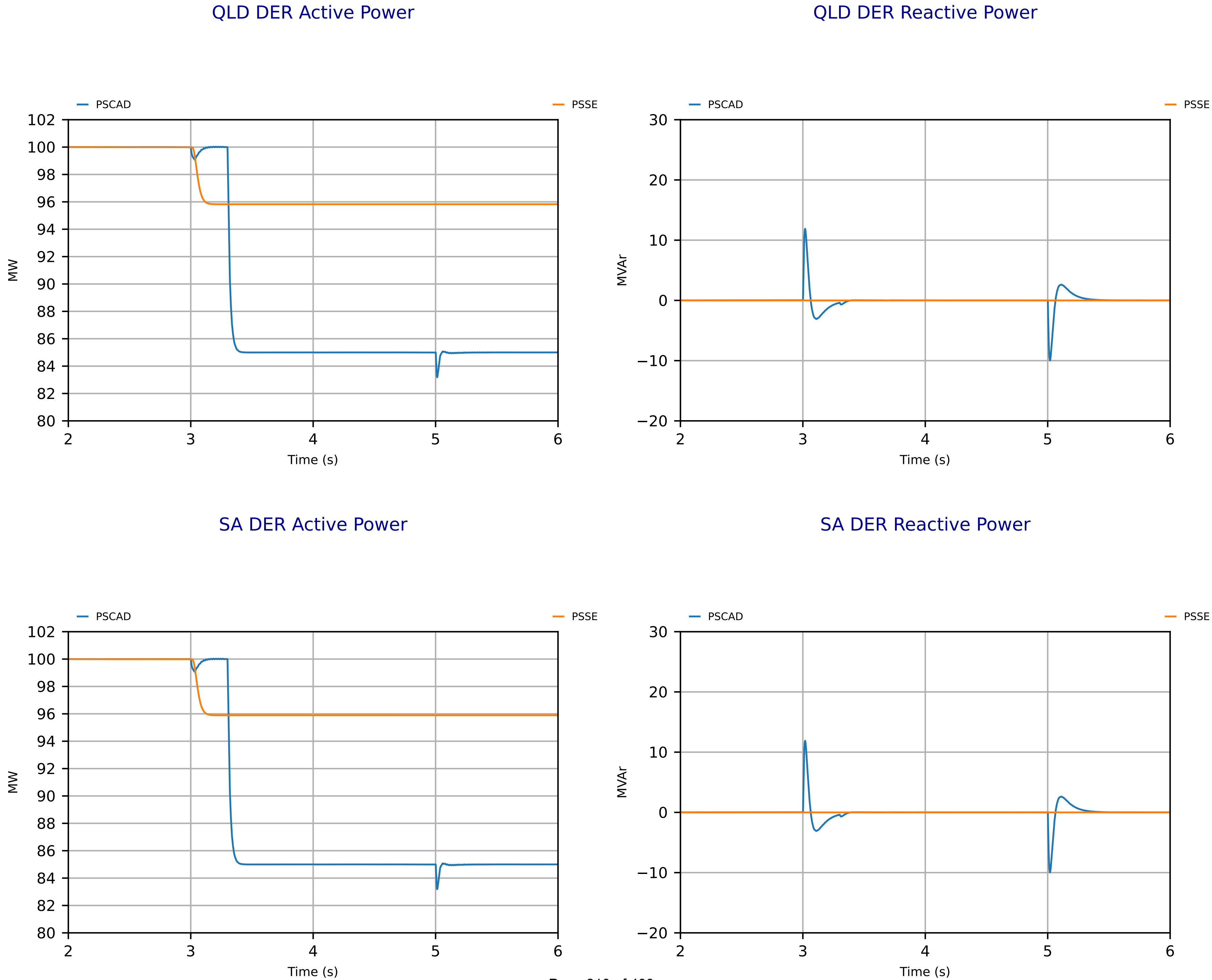
VIC DER Active Power



VIC DER Reactive Power



DER_SMIB_SCR_10_XR_3_T10_3



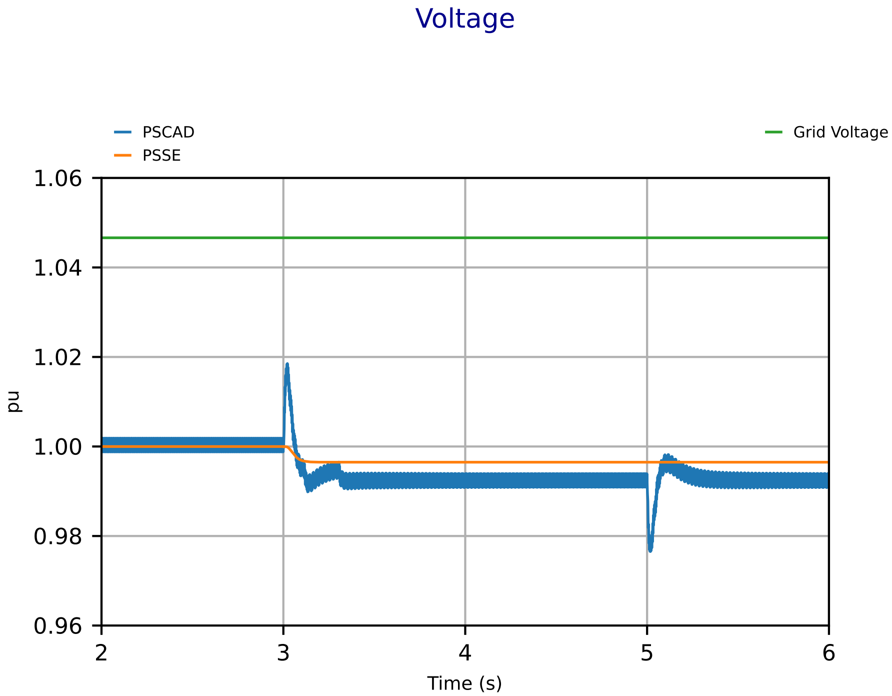
DER SMIB

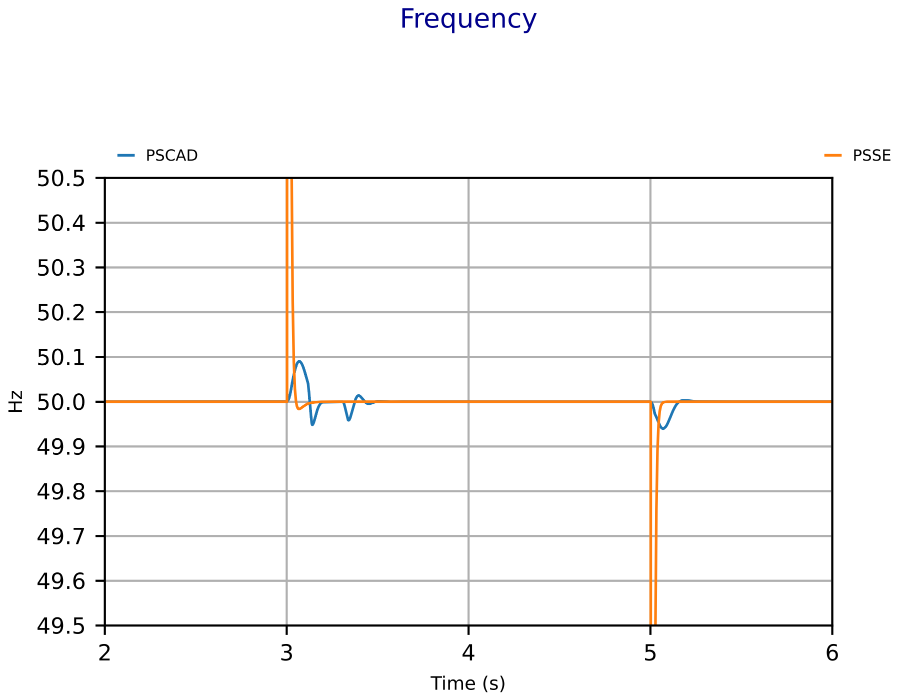
SCR = 10, X/R = 3

Test #11:

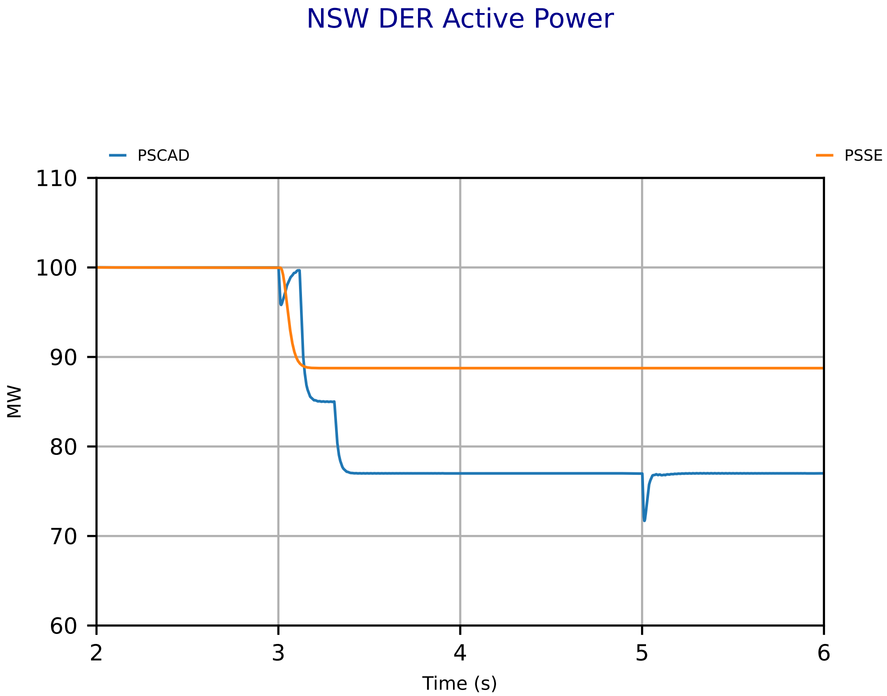
40° phase angle step

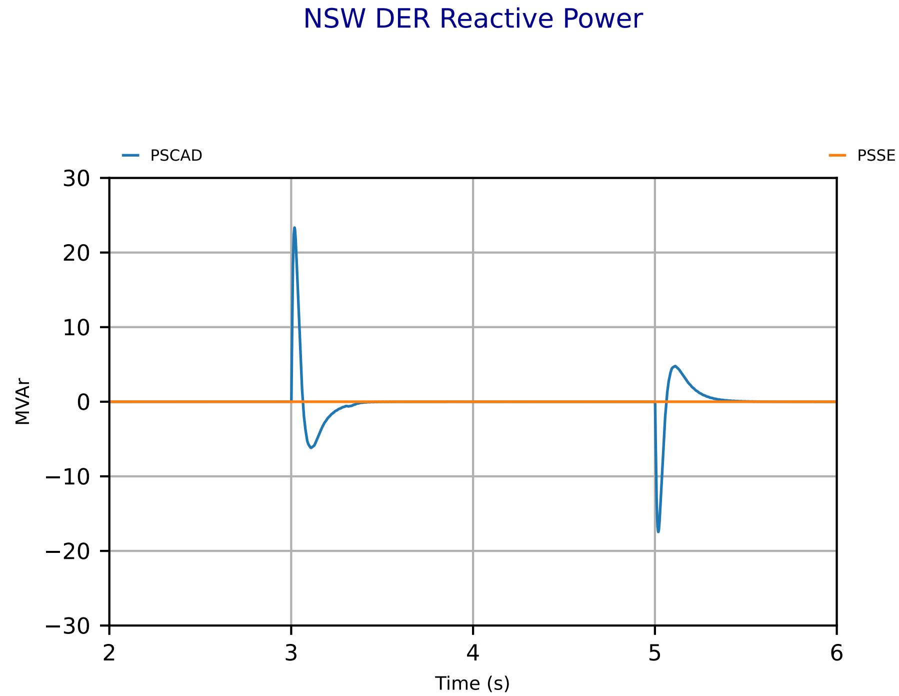
DER_SMIB_SCR_10_XR_3_T11_1

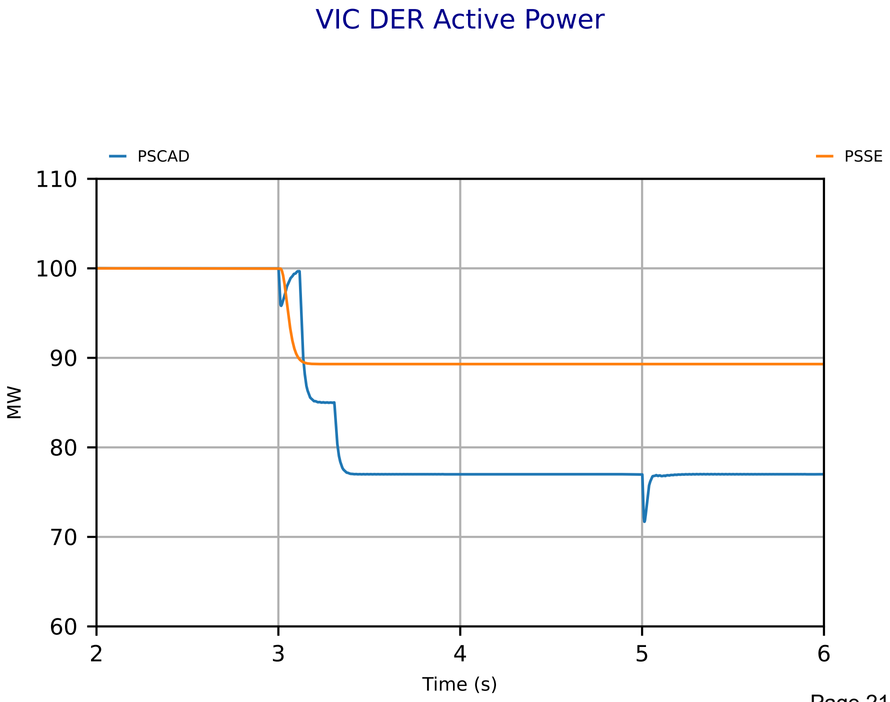


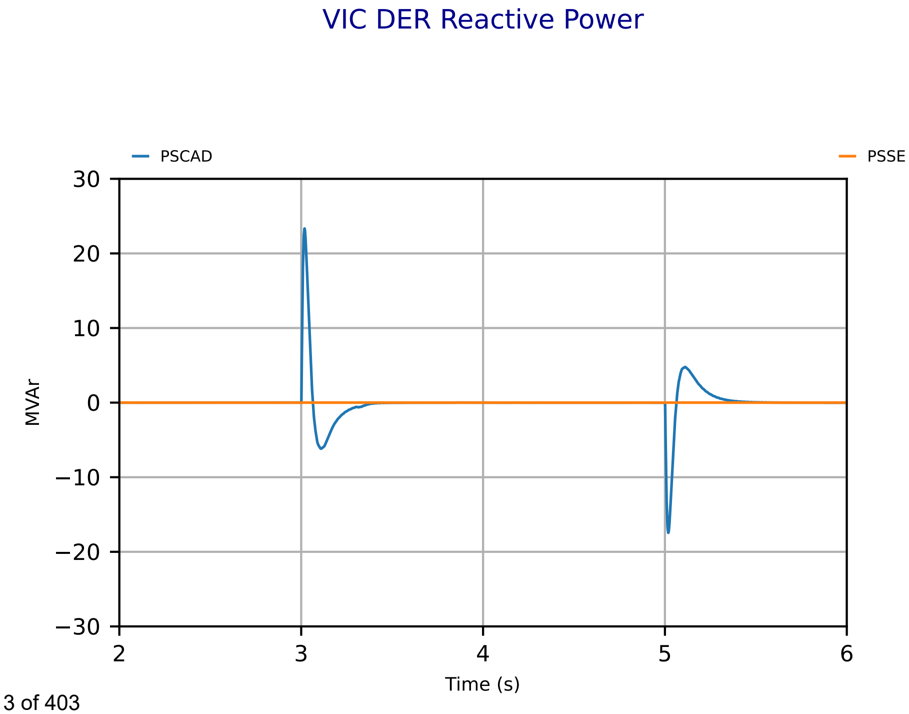


DER_SMIB_SCR_10_XR_3_T11_2



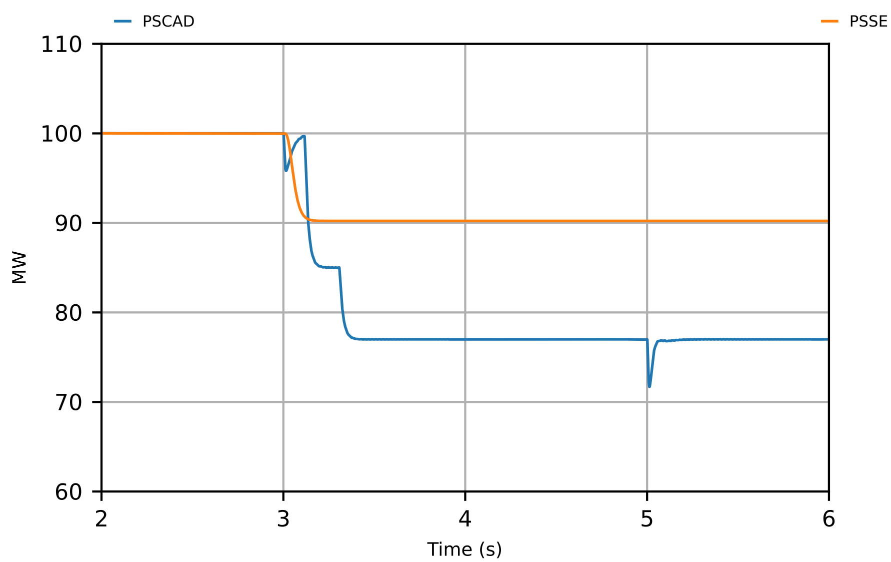




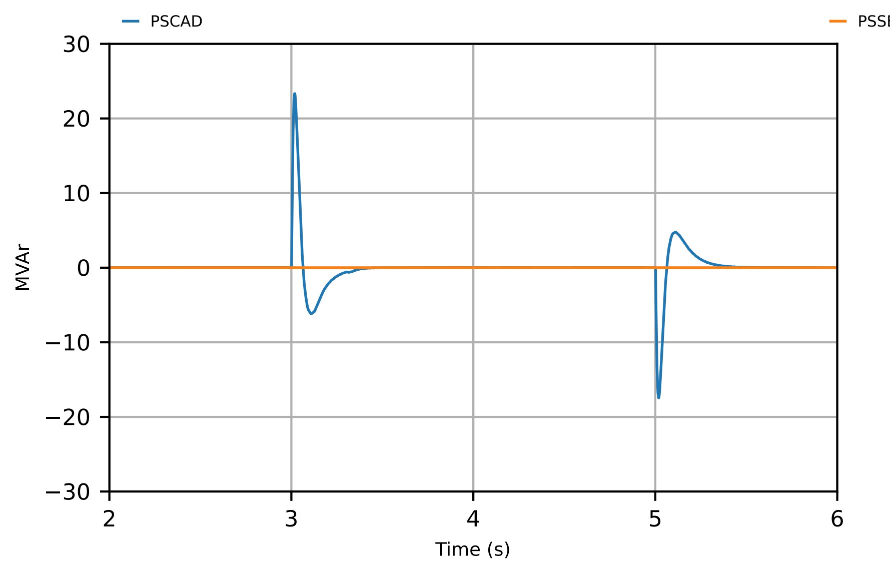


DER_SMIB_SCR_10_XR_3_T11_3

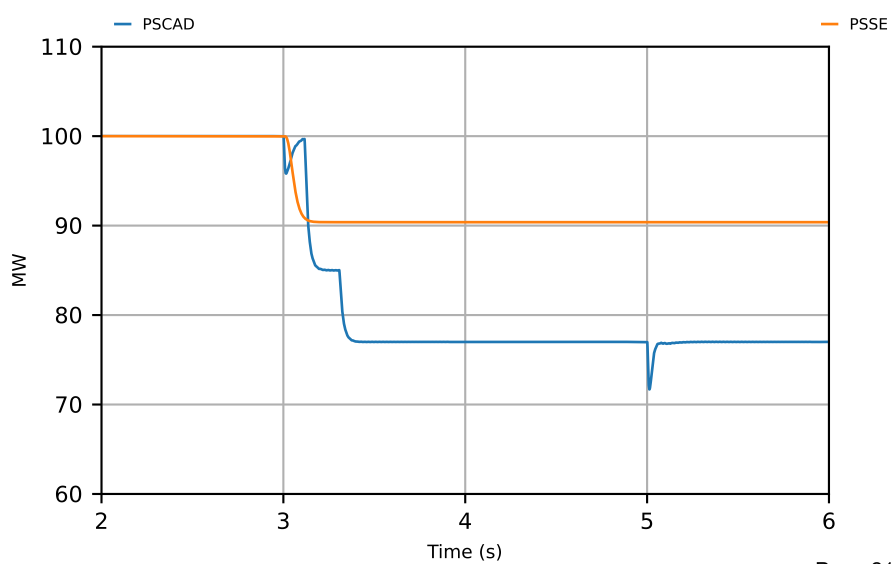
QLD DER Active Power



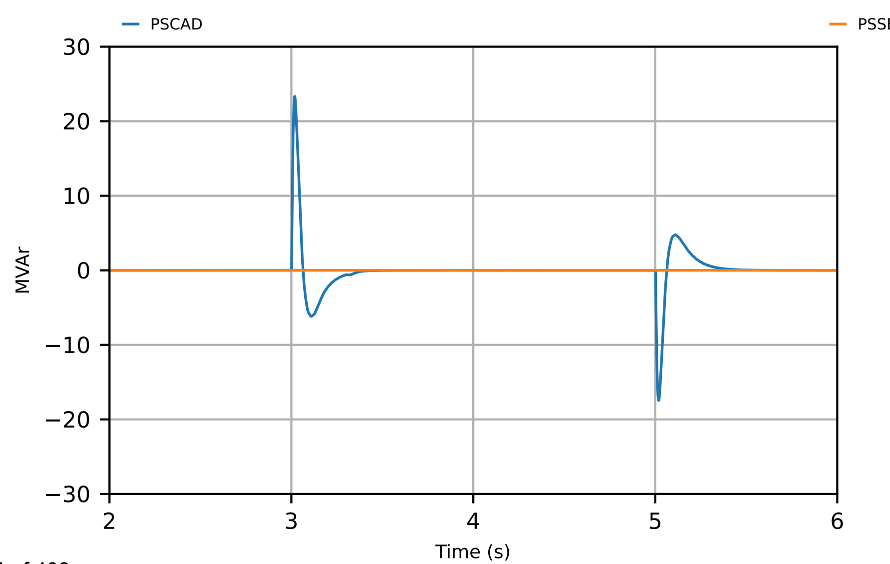
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



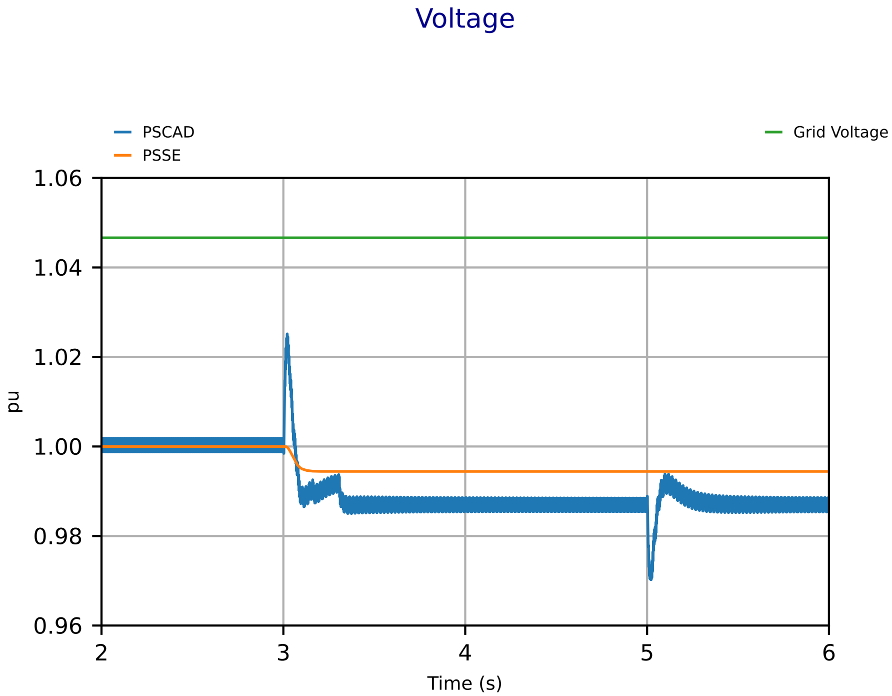
DER SMIB

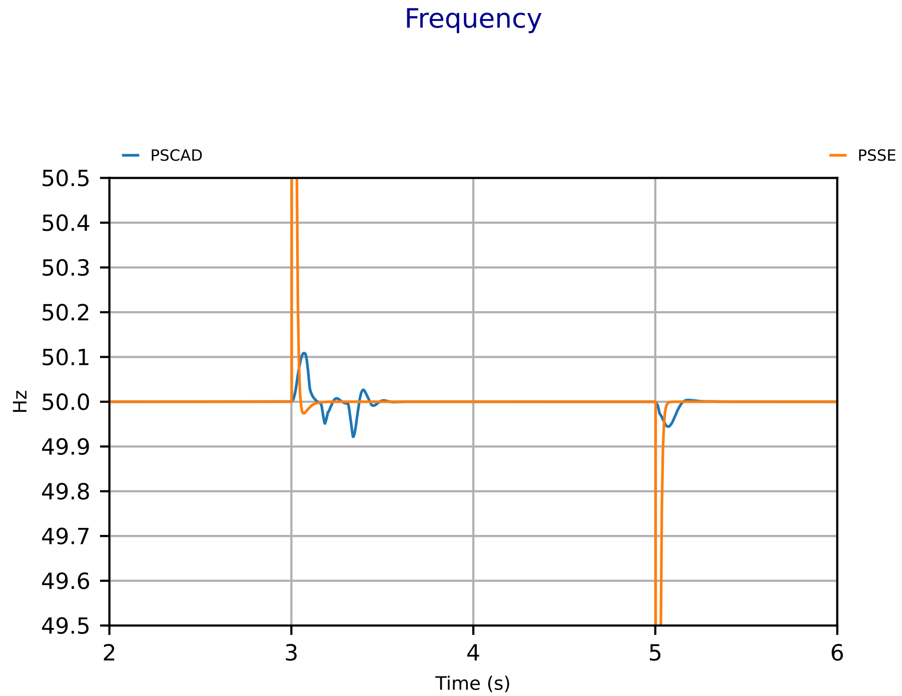
SCR = 10, X/R = 3

Test #12:

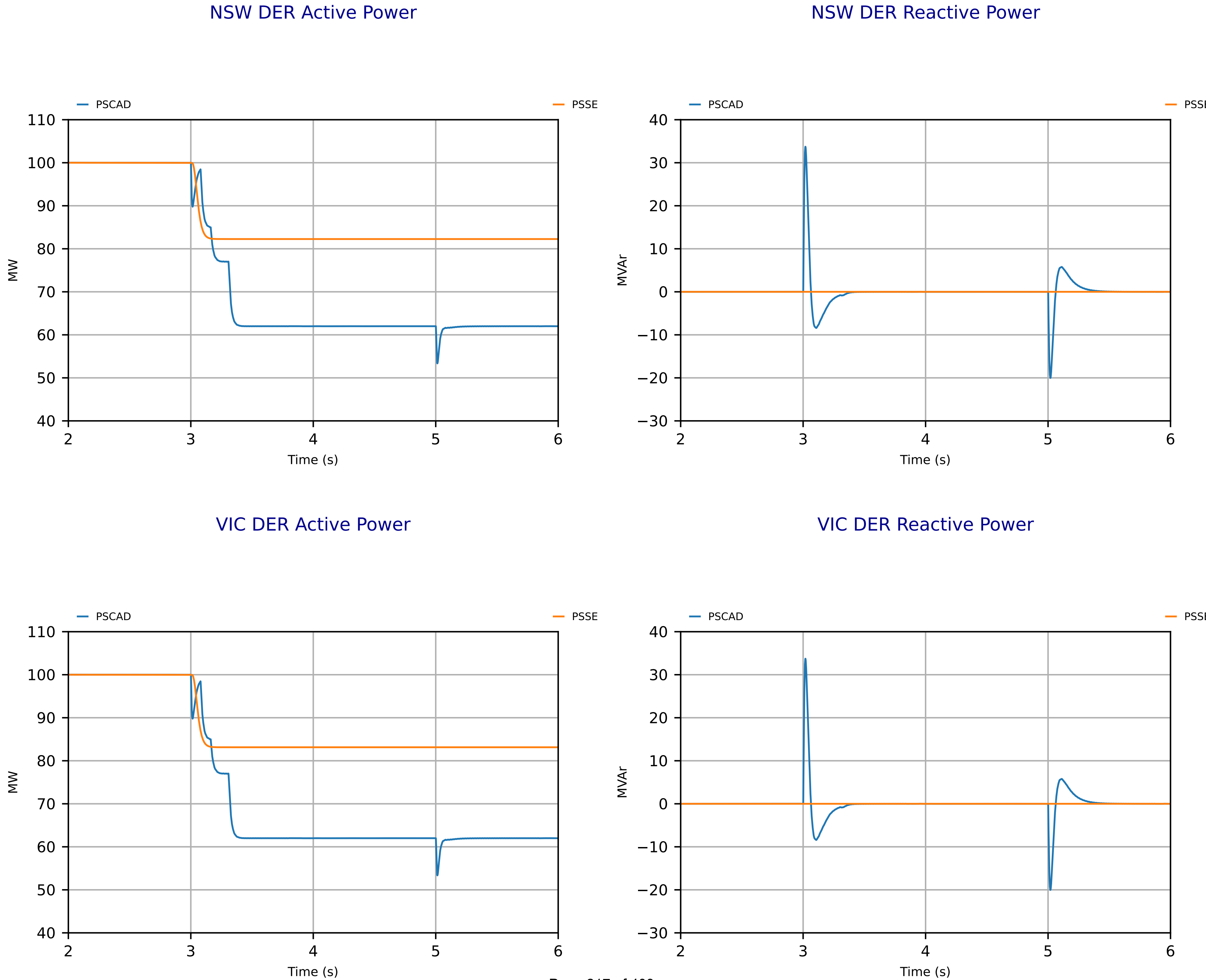
60° phase angle step

DER_SMIB_SCR_10_XR_3_T12_1



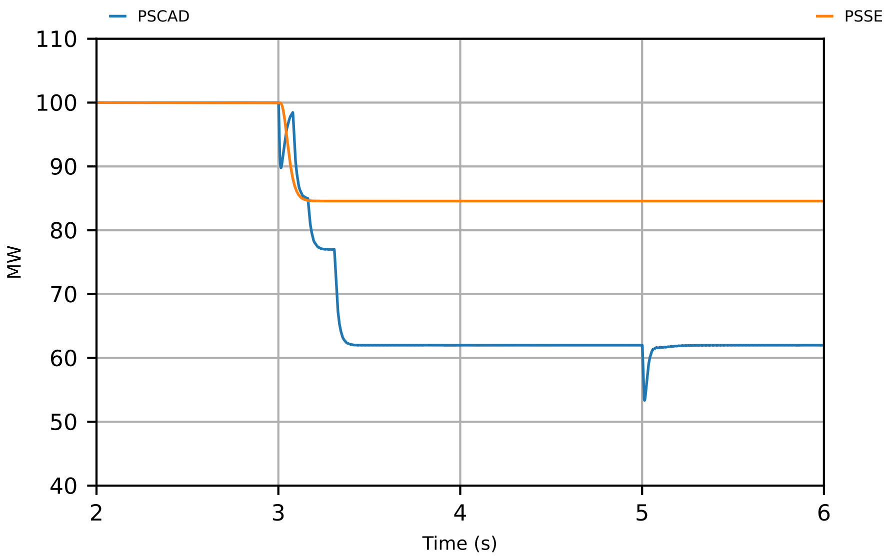


DER_SMIB_SCR_10_XR_3_T12_2

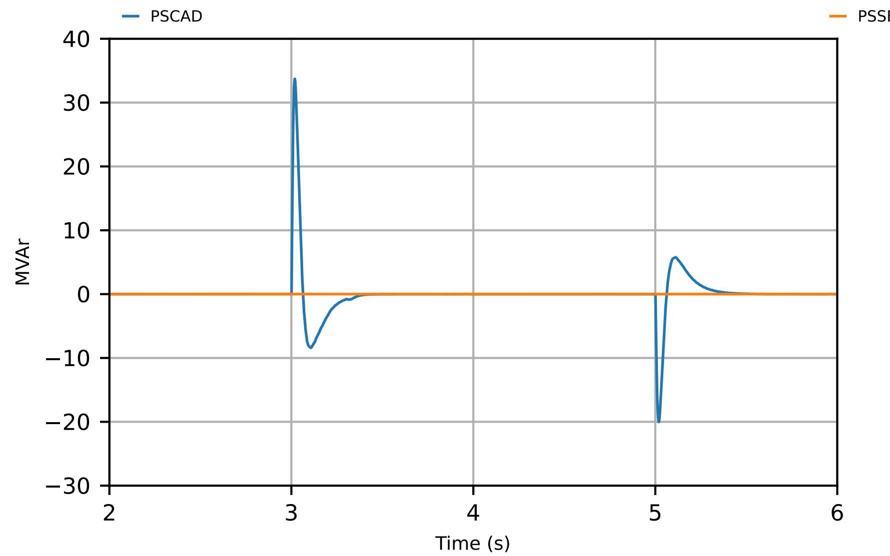


DER_SMIB_SCR_10_XR_3_T12_3

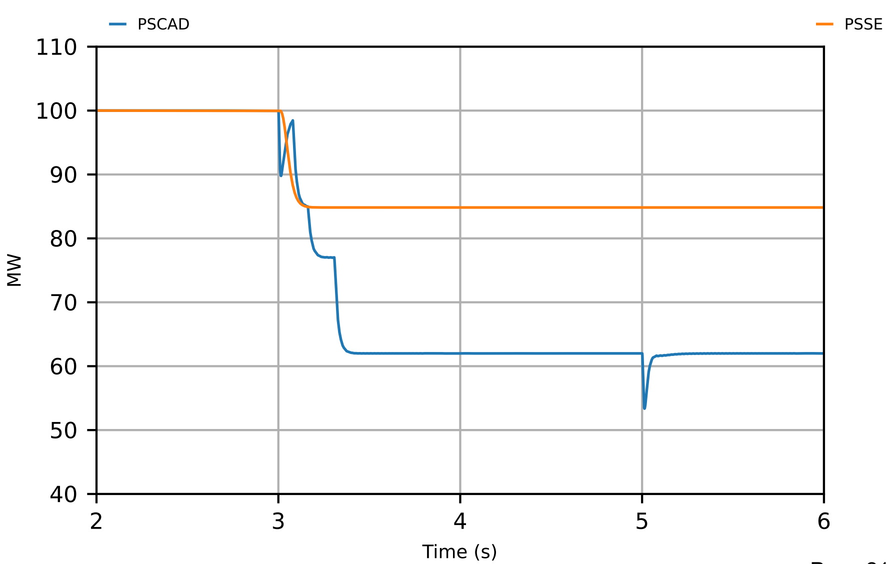
QLD DER Active Power



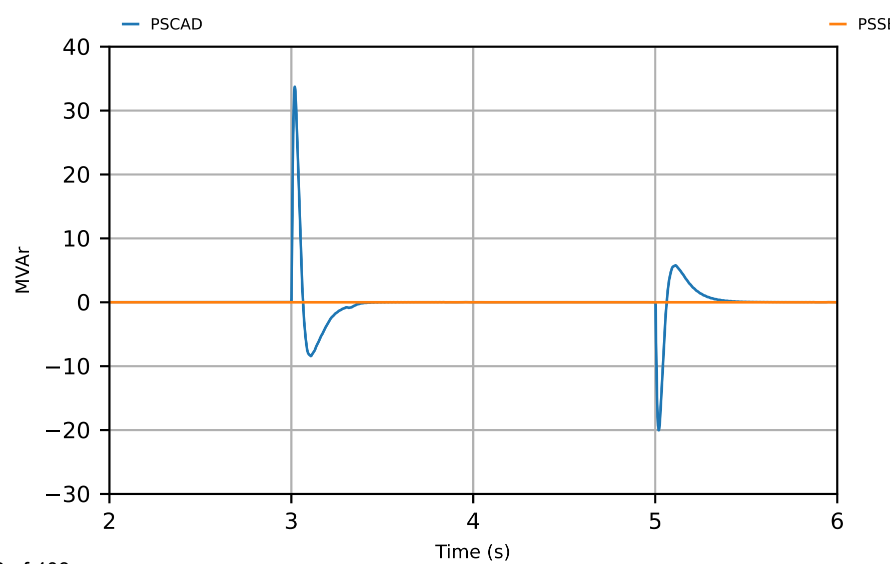
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



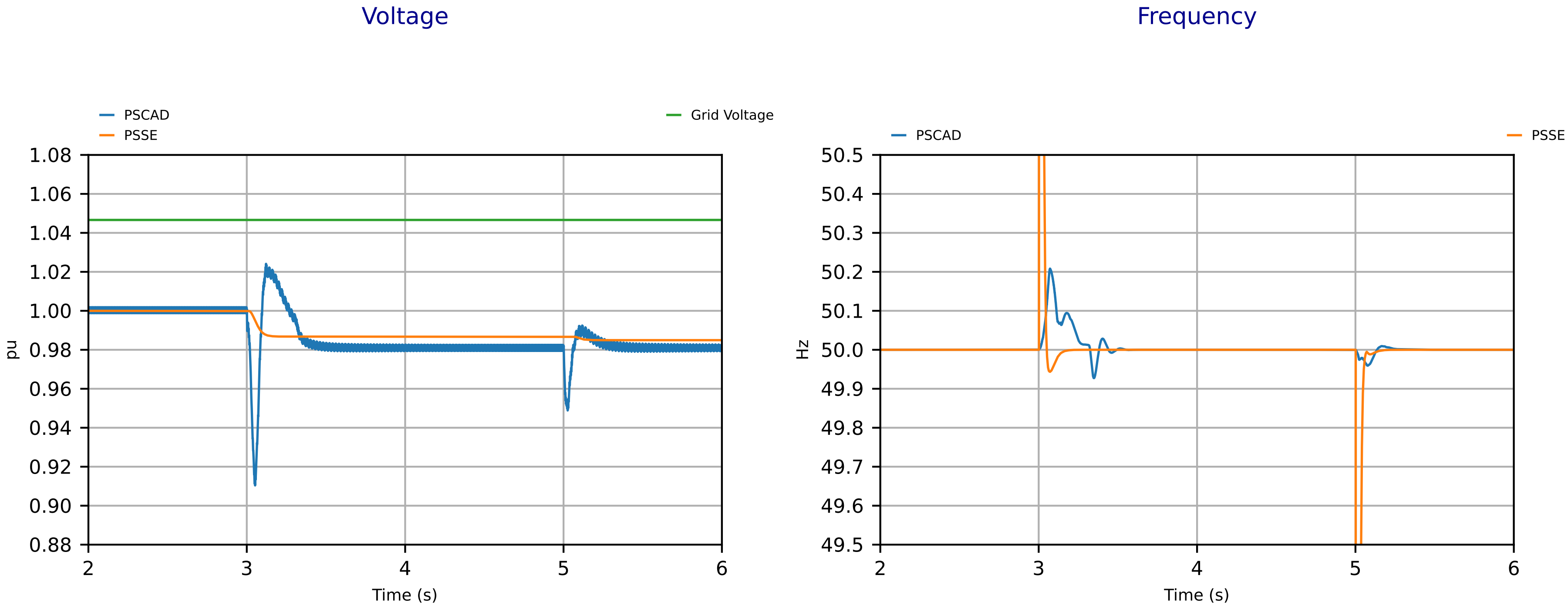
DER SMIB

SCR = 10, X/R = 3

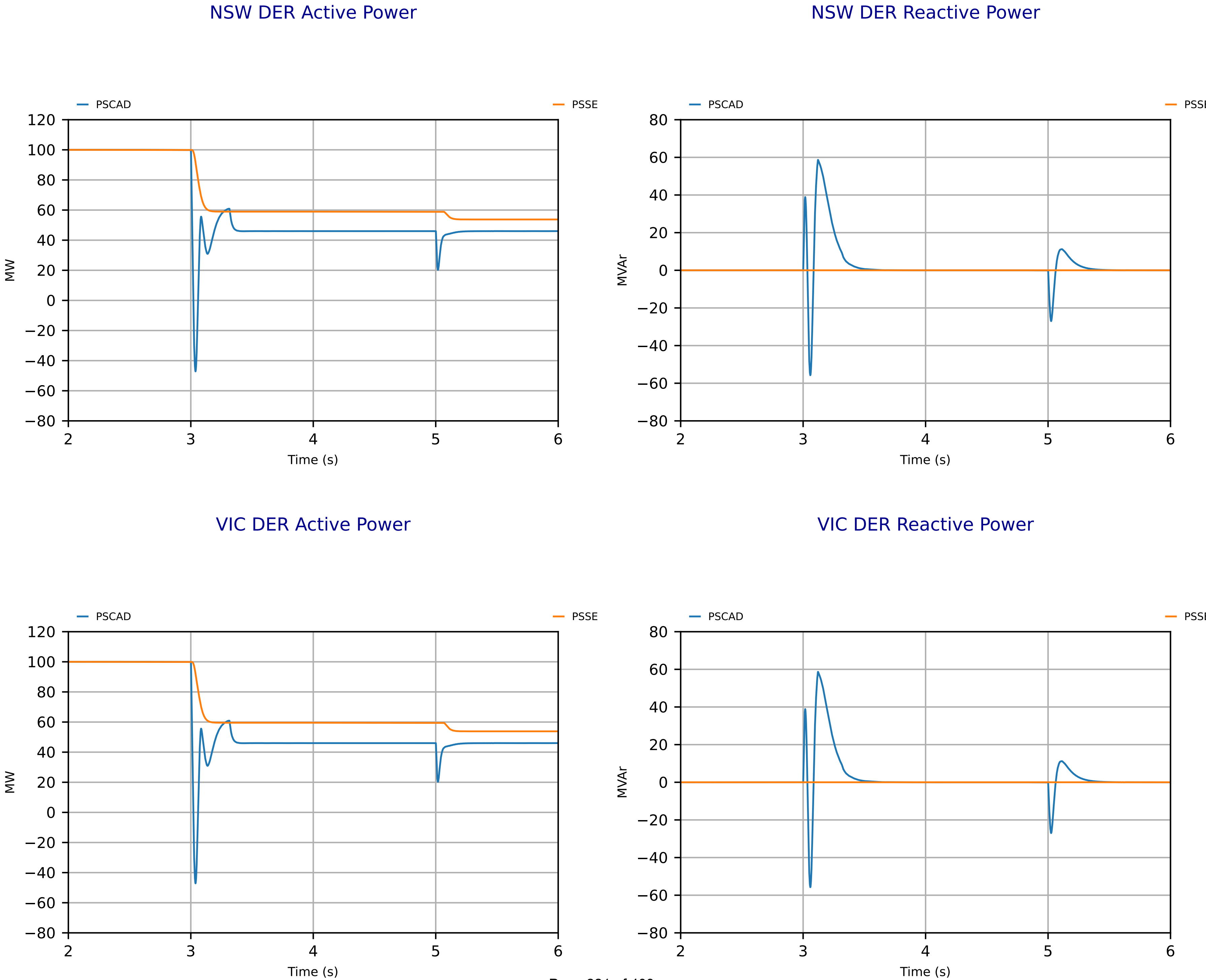
Test #13:

120° phase angle step

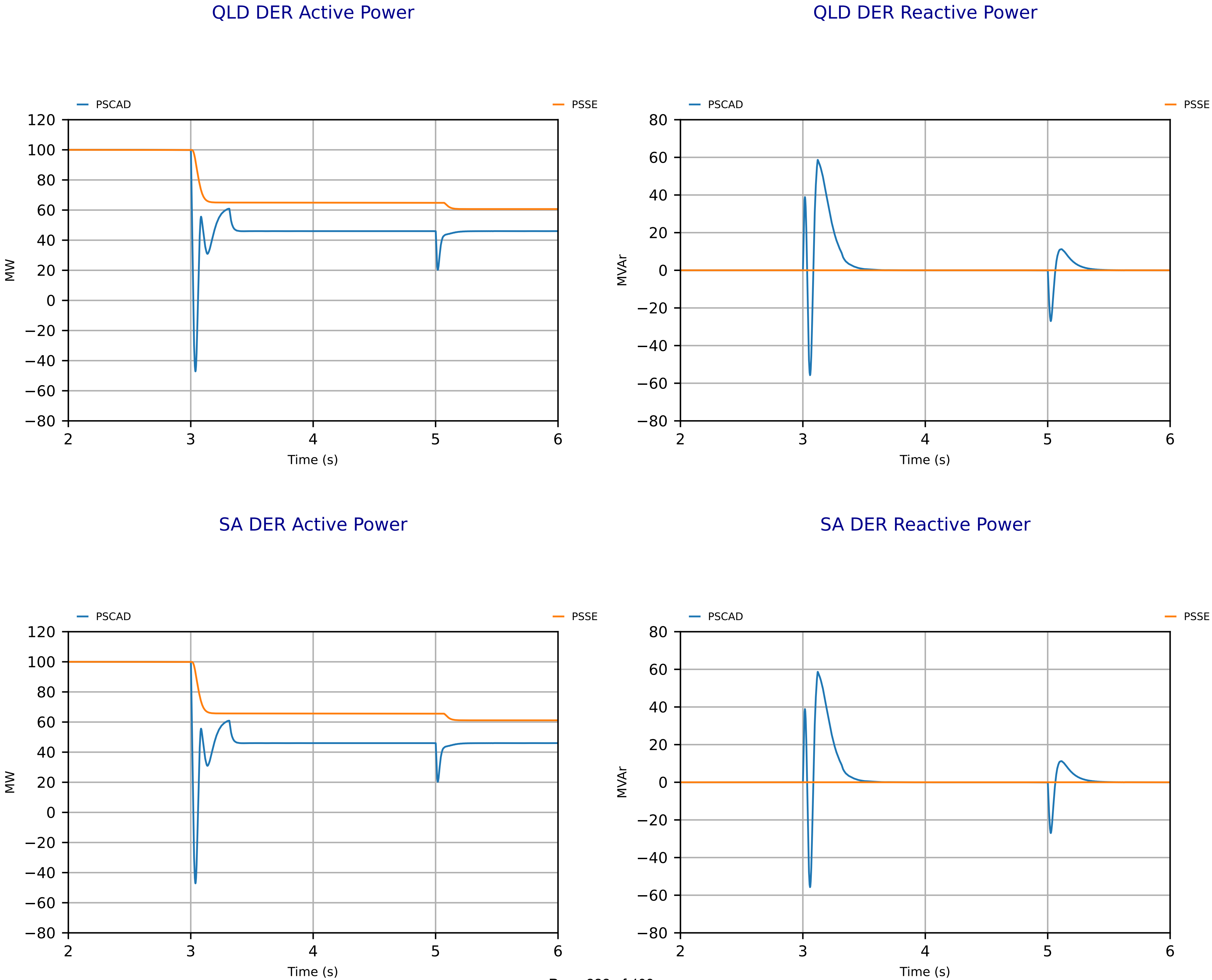
DER_SMIB_SCR_10_XR_3_T13_1



DER_SMIB_SCR_10_XR_3_T13_2



DER_SMIB_SCR_10_XR_3_T13_3



DER SMIB

SCR = 10, X/R = 14

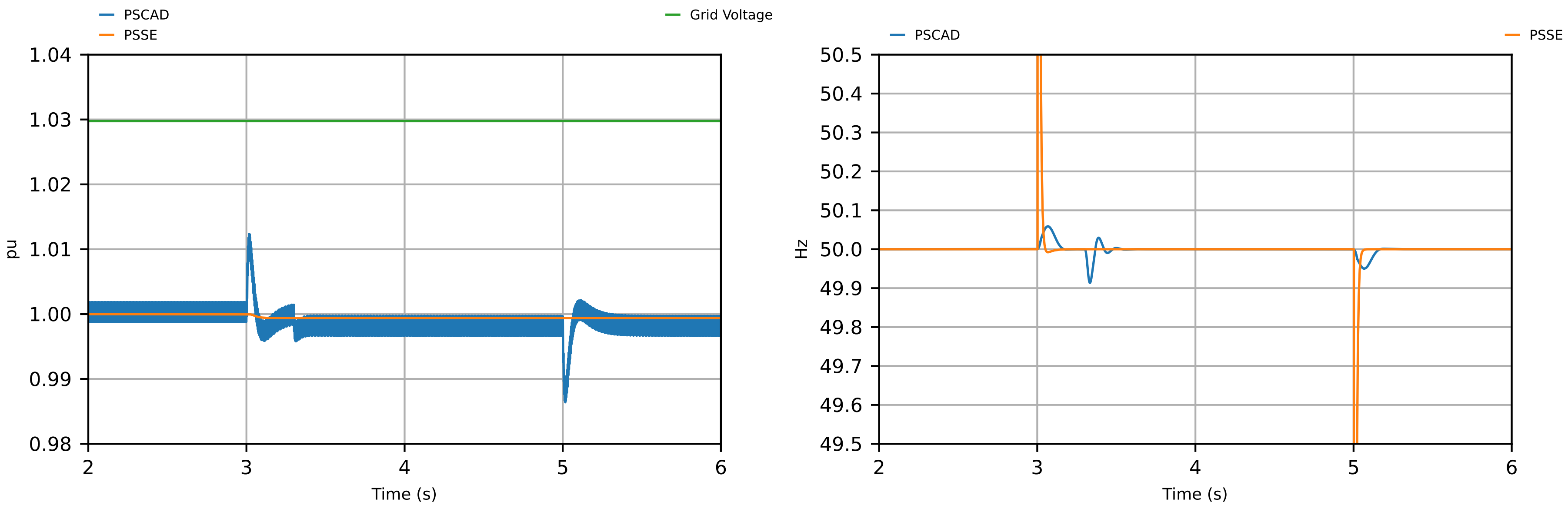
Test #10:

20° phase angle step

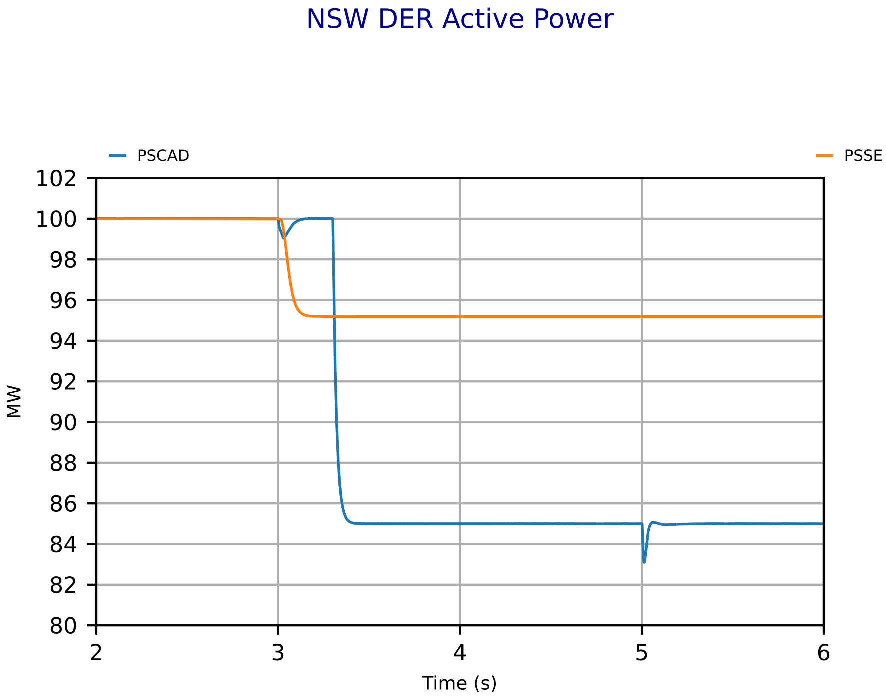
DER_SMIB_SCR_10_XR_14_T10_1

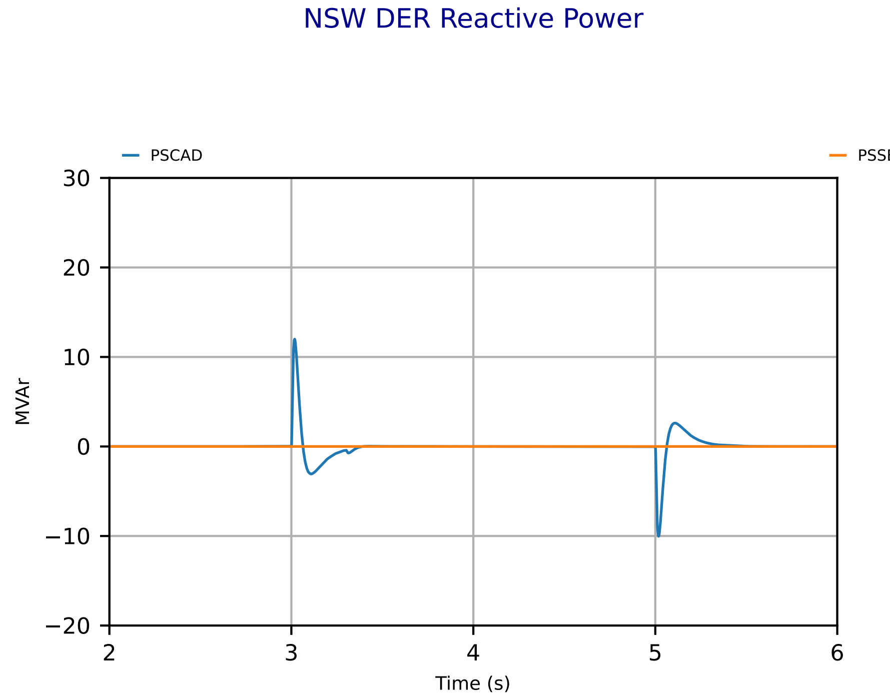
Voltage

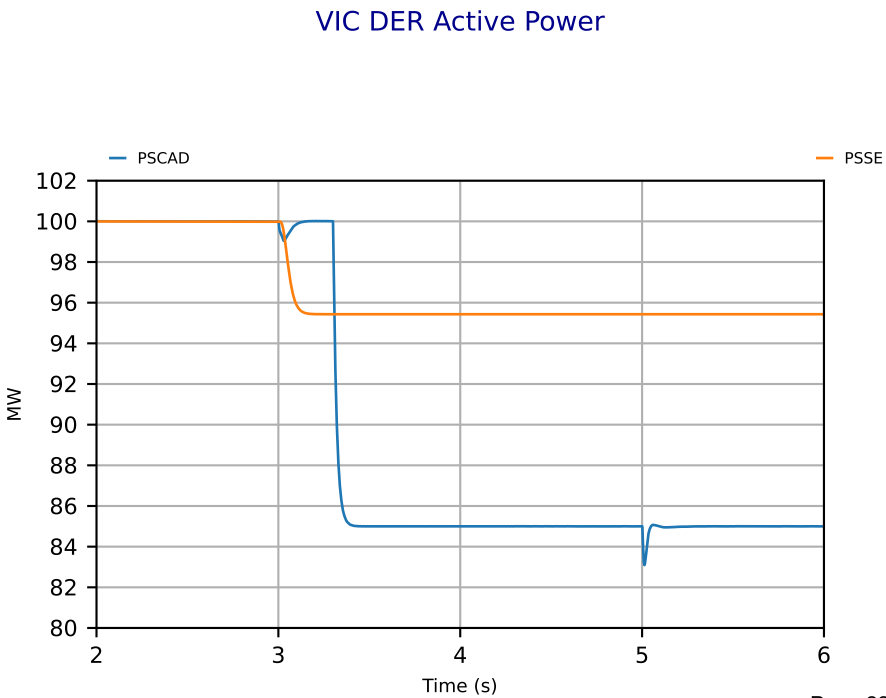
Frequency

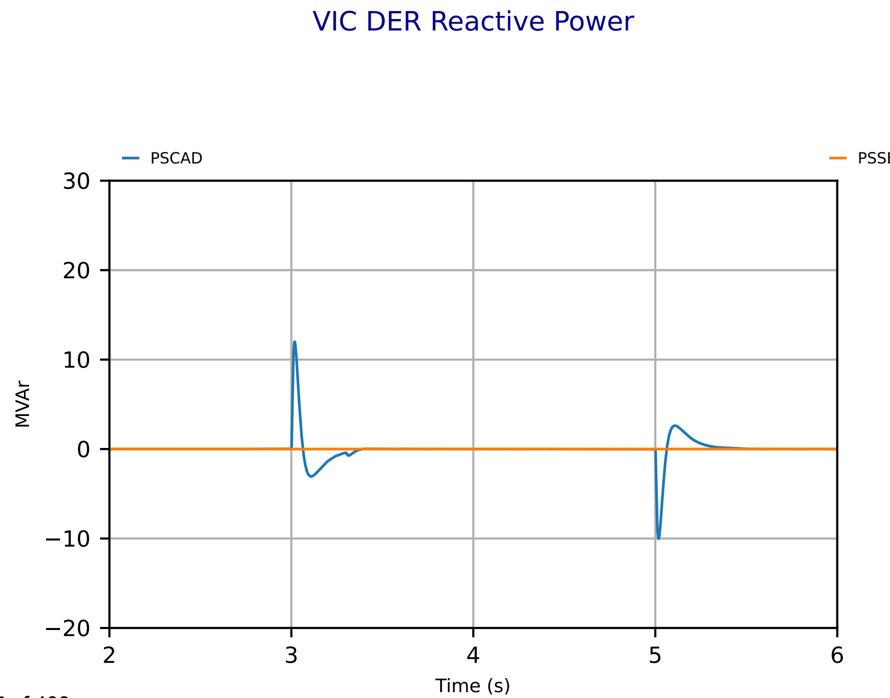


DER_SMIB_SCR_10_XR_14_T10_2

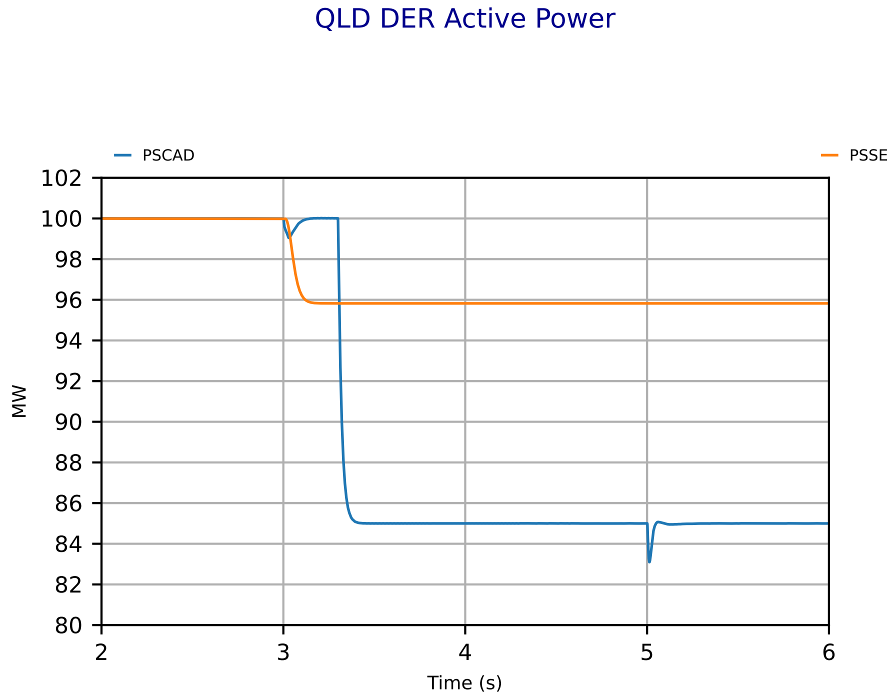


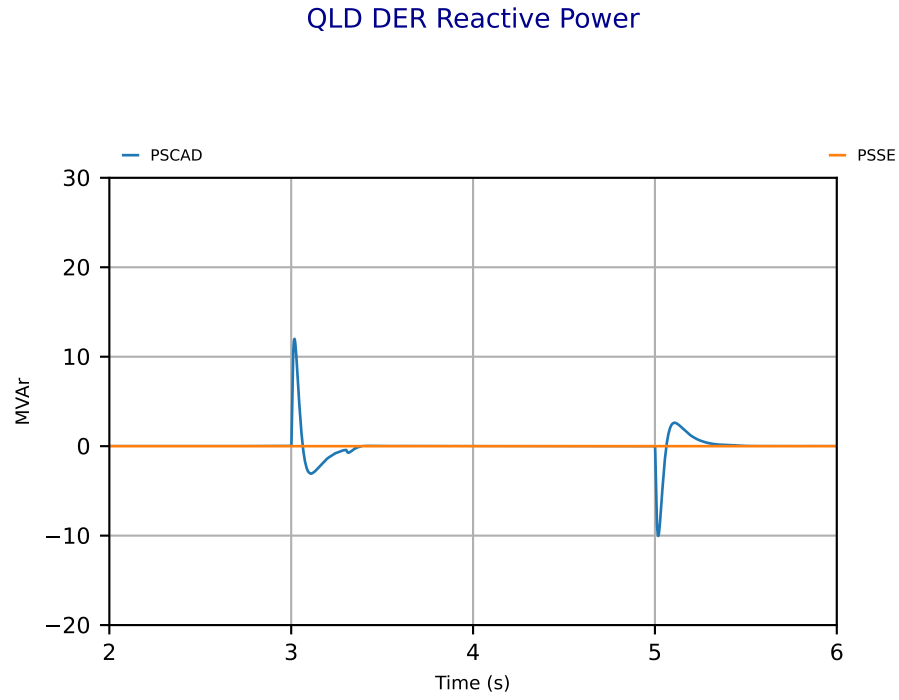


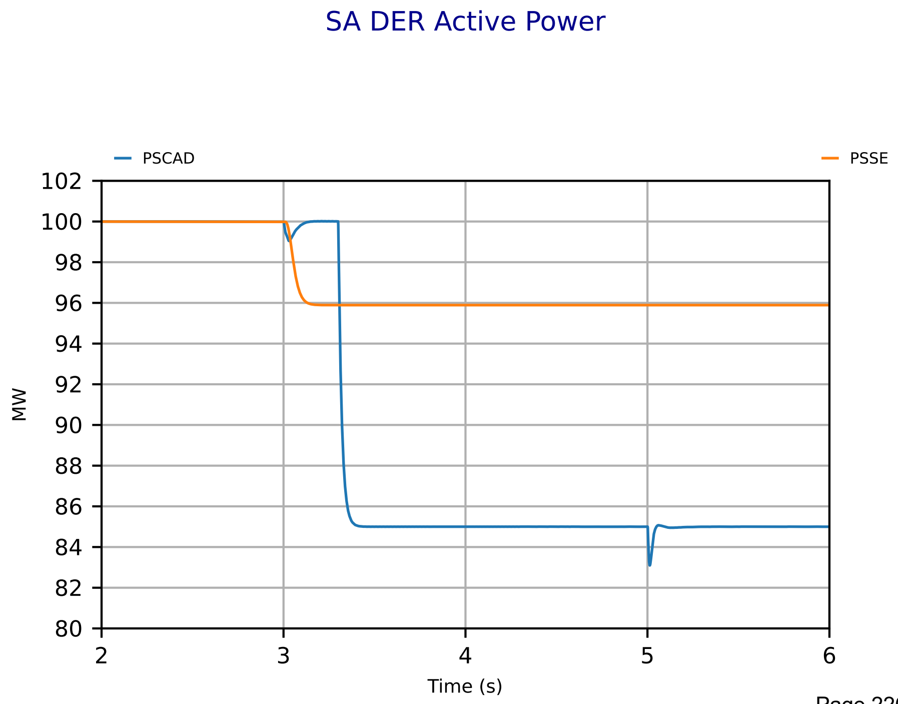


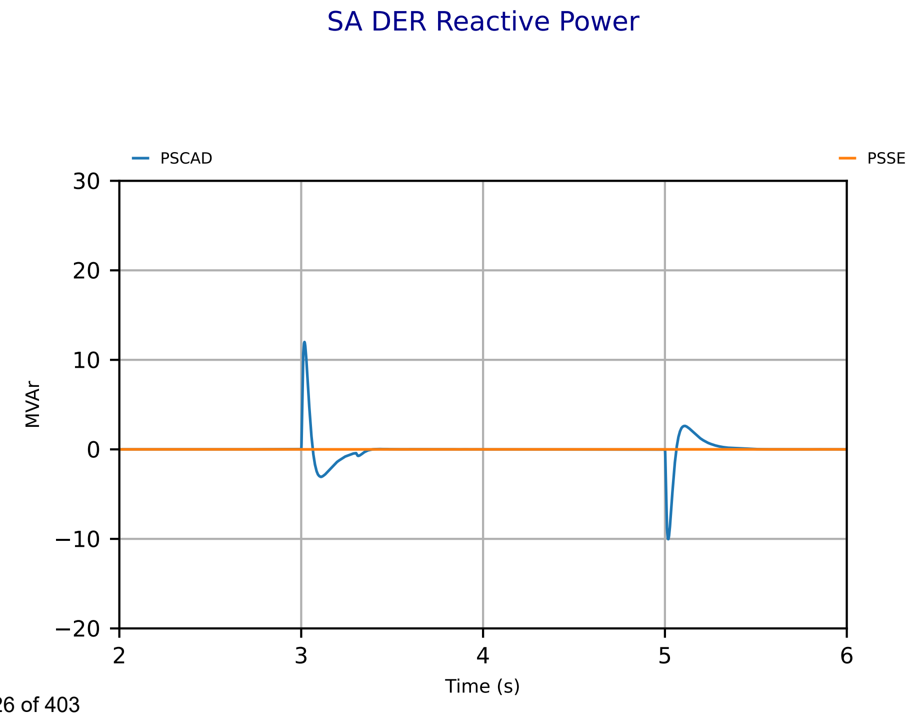


DER_SMIB_SCR_10_XR_14_T10_3









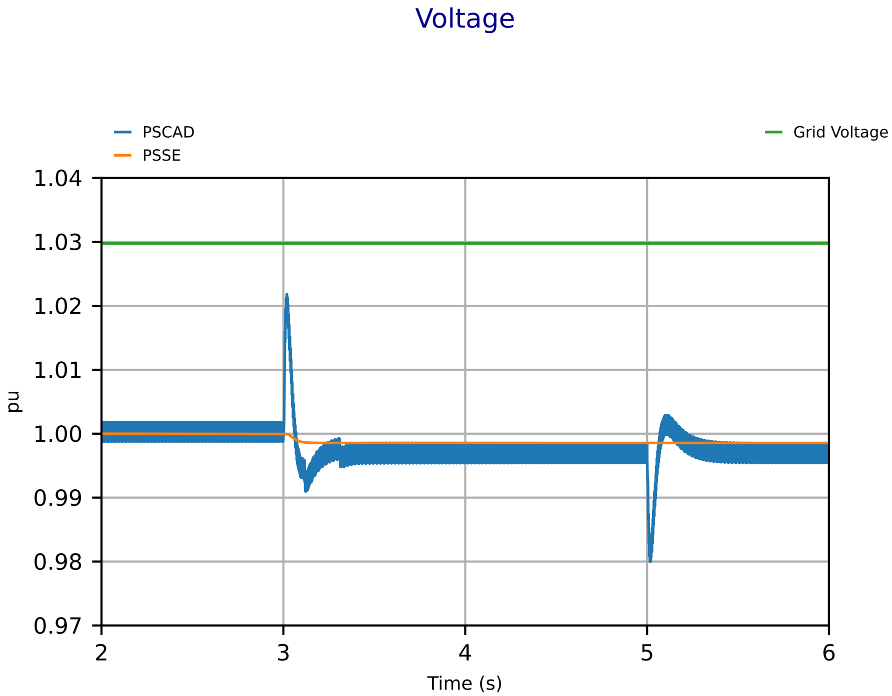
DER SMIB

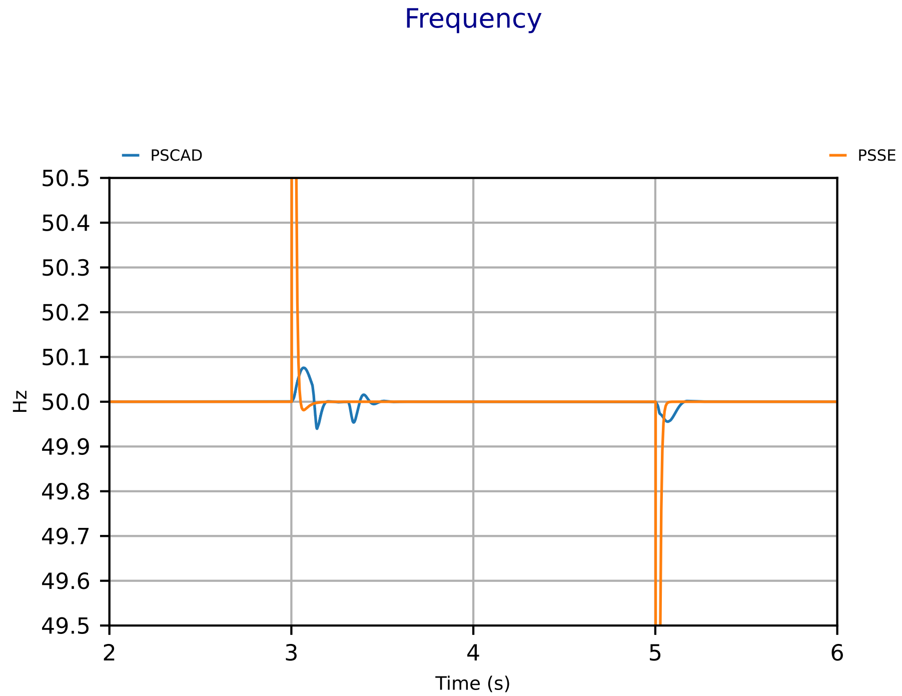
SCR = 10, X/R = 14

Test #11:

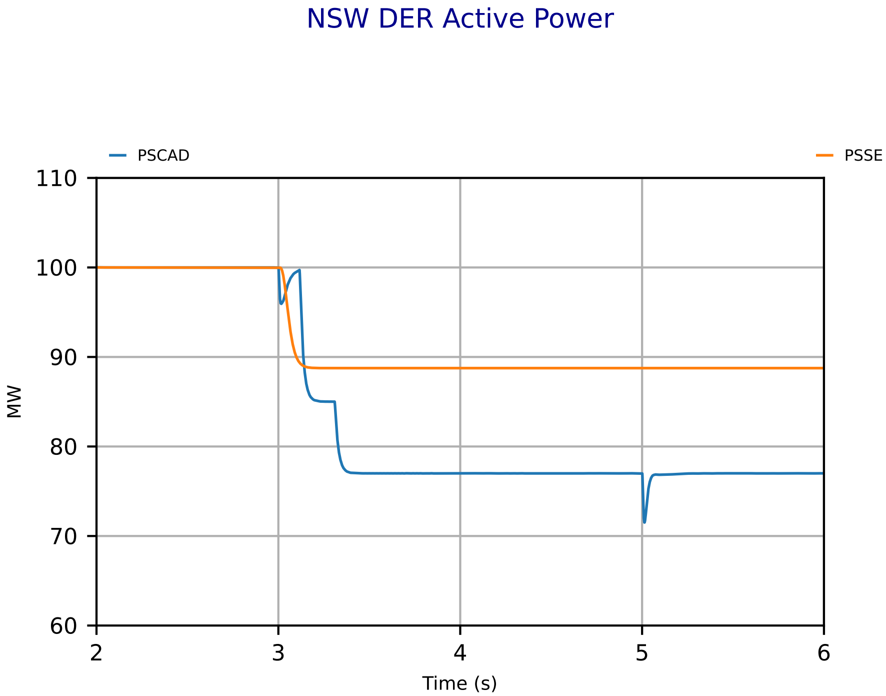
40° phase angle step

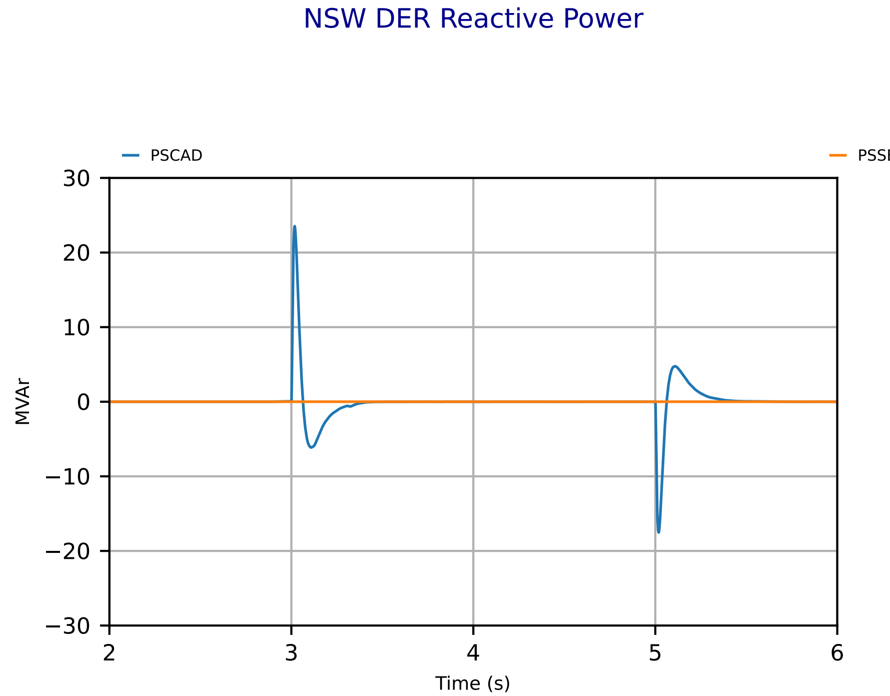
DER_SMIB_SCR_10_XR_14_T11_1

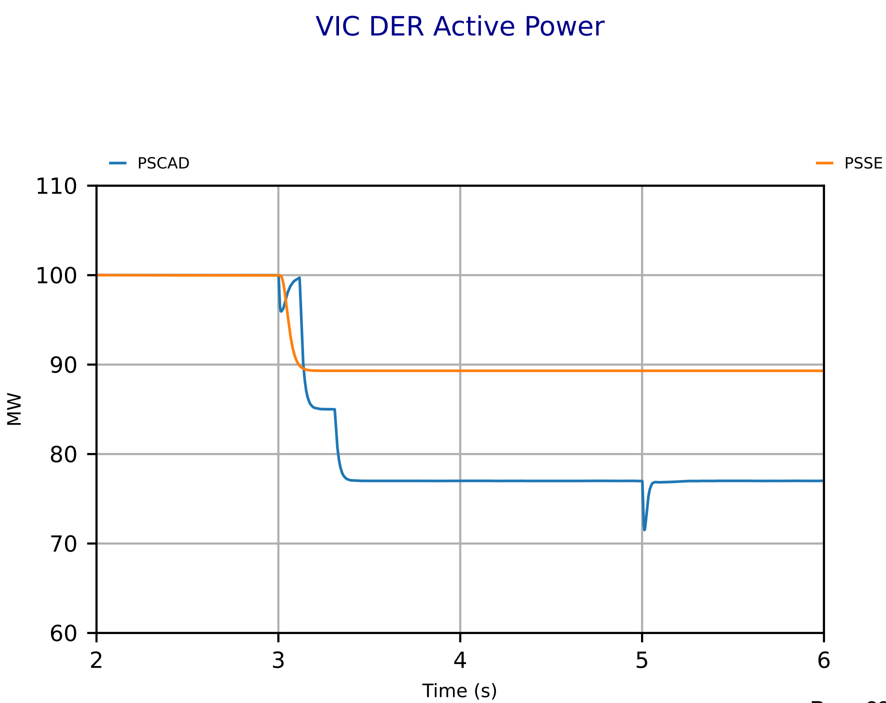


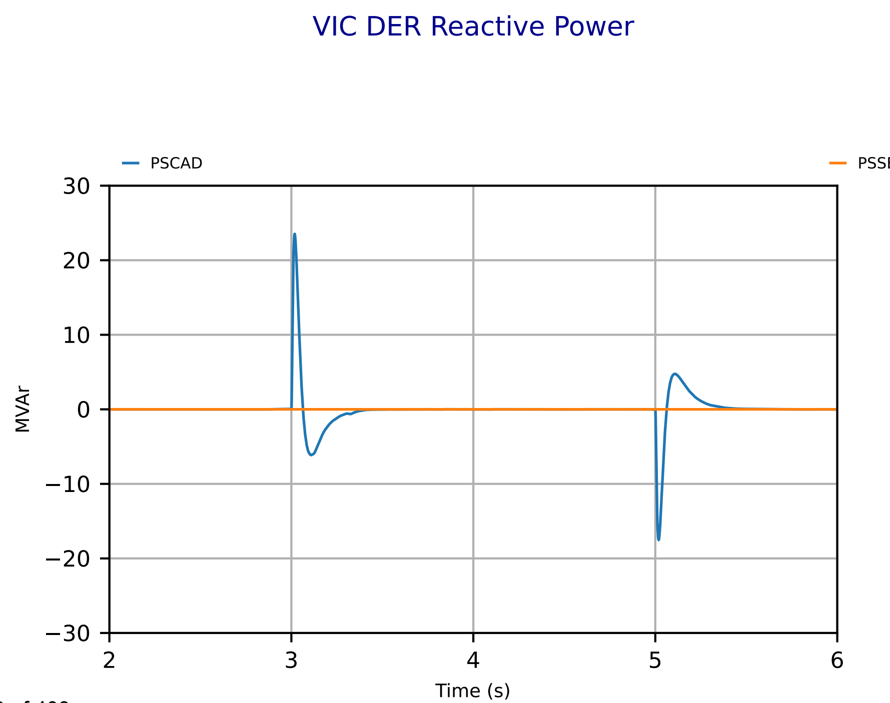


DER_SMIB_SCR_10_XR_14_T11_2



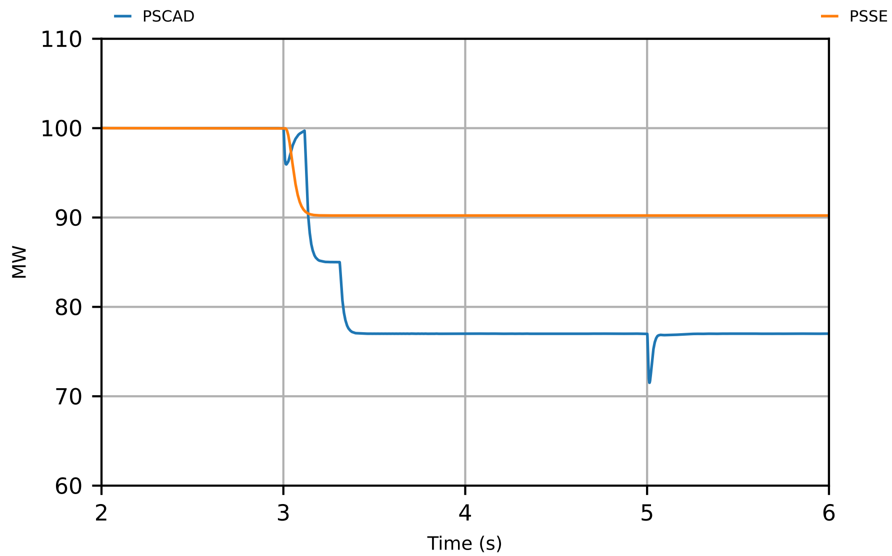




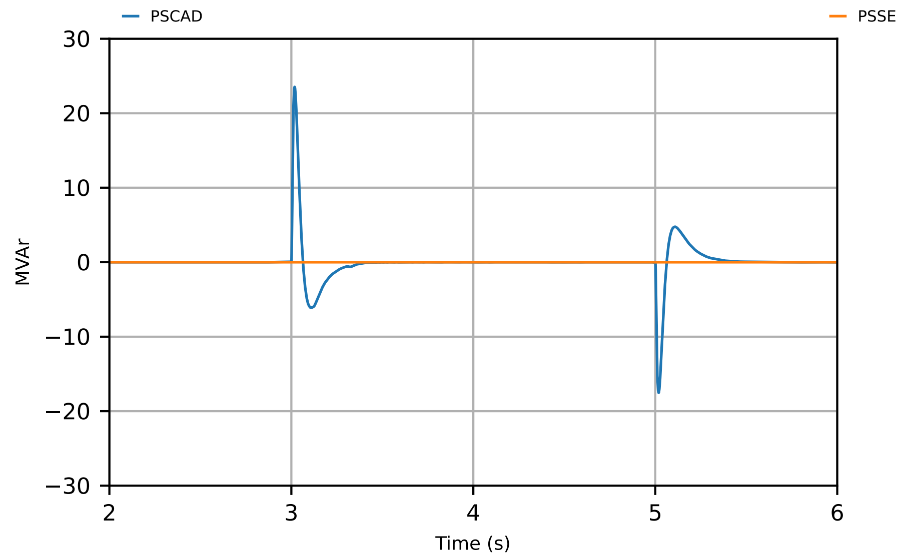


DER_SMIB_SCR_10_XR_14_T11_3

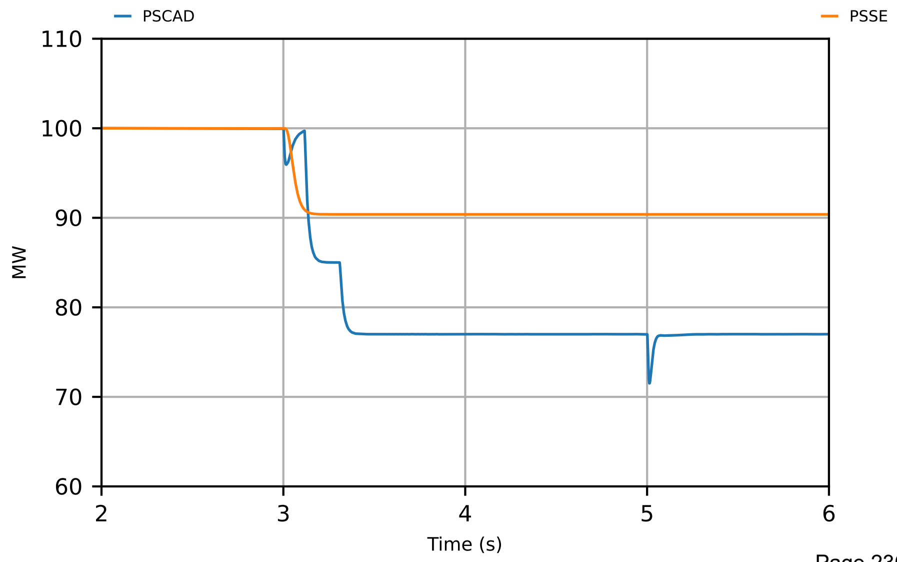
QLD DER Active Power



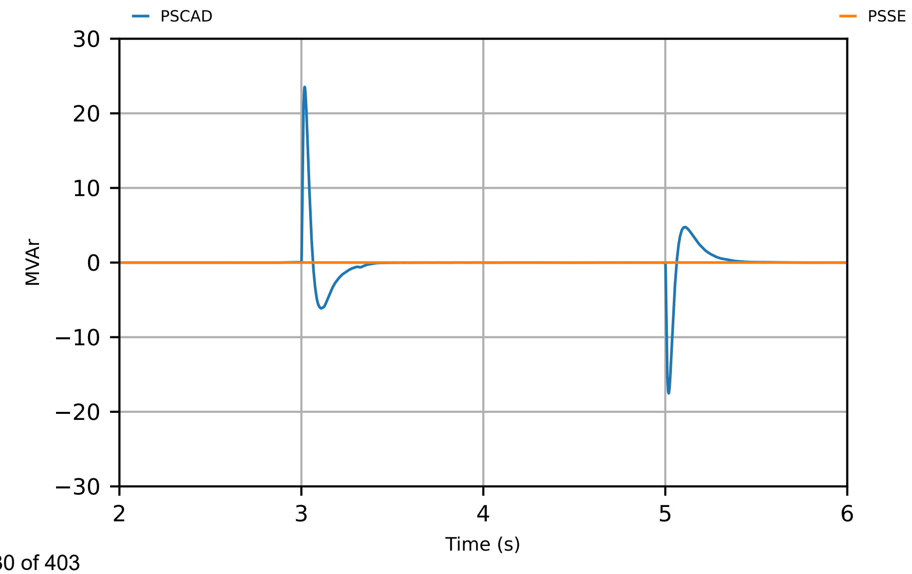
QLD DER Reactive Power



SA DER Active Power



SA DER Reactive Power



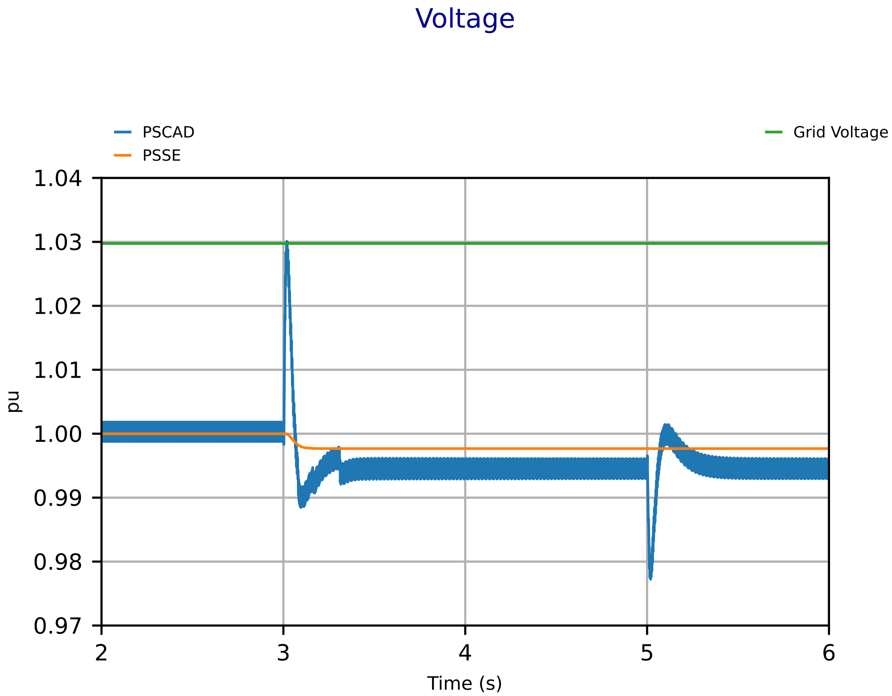
DER SMIB

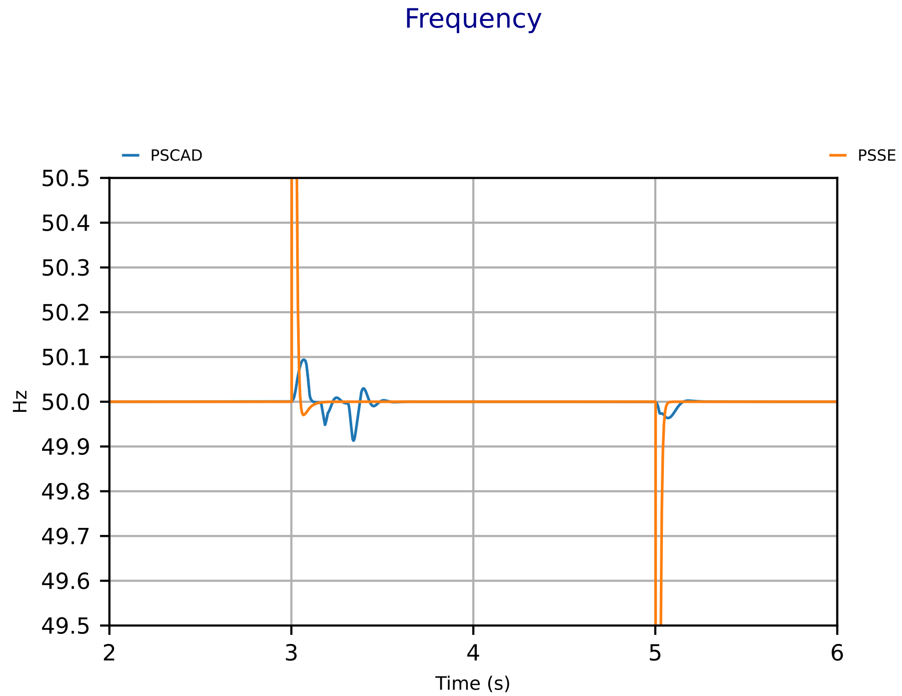
SCR = 10, X/R = 14

Test #12:

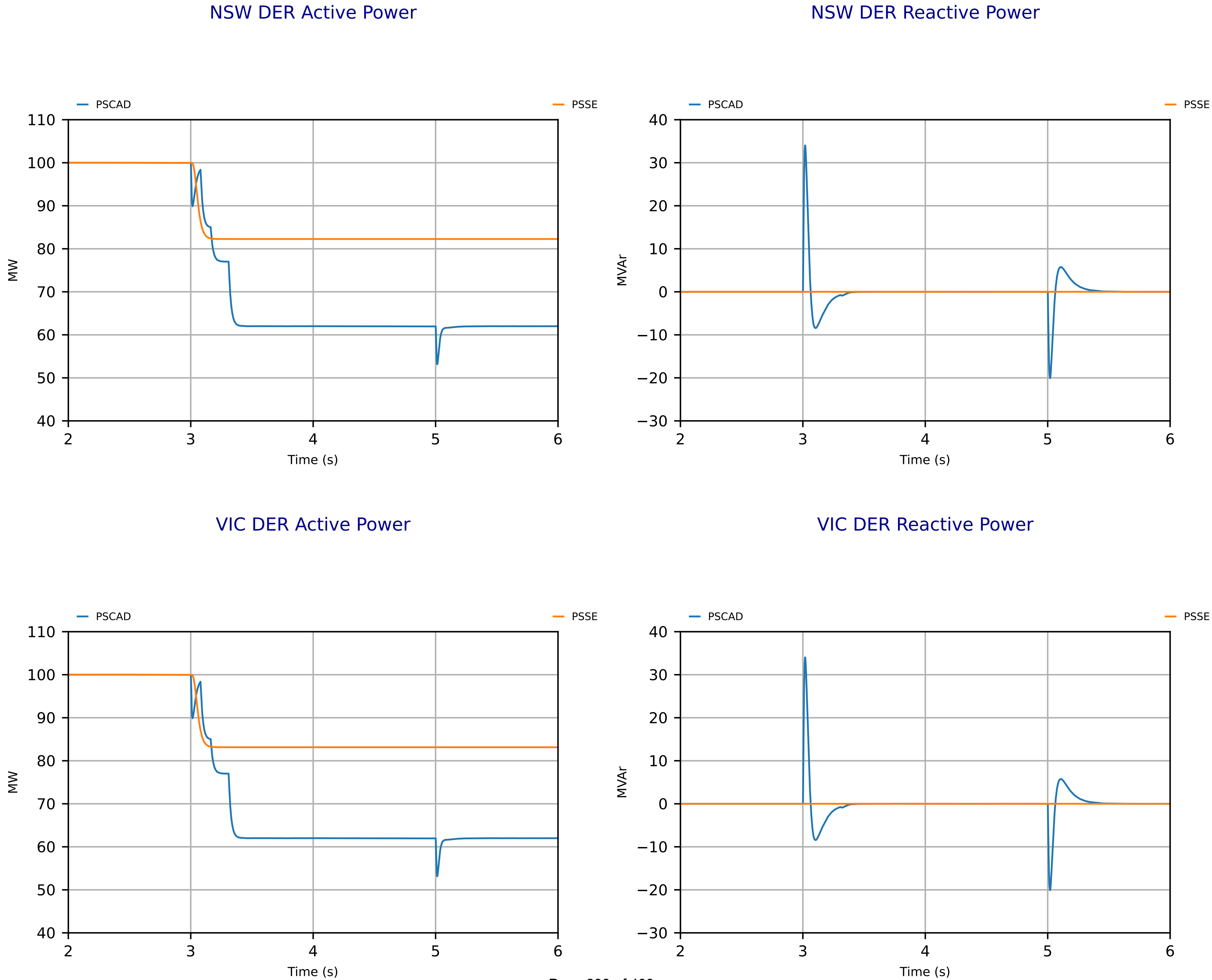
60° phase angle step

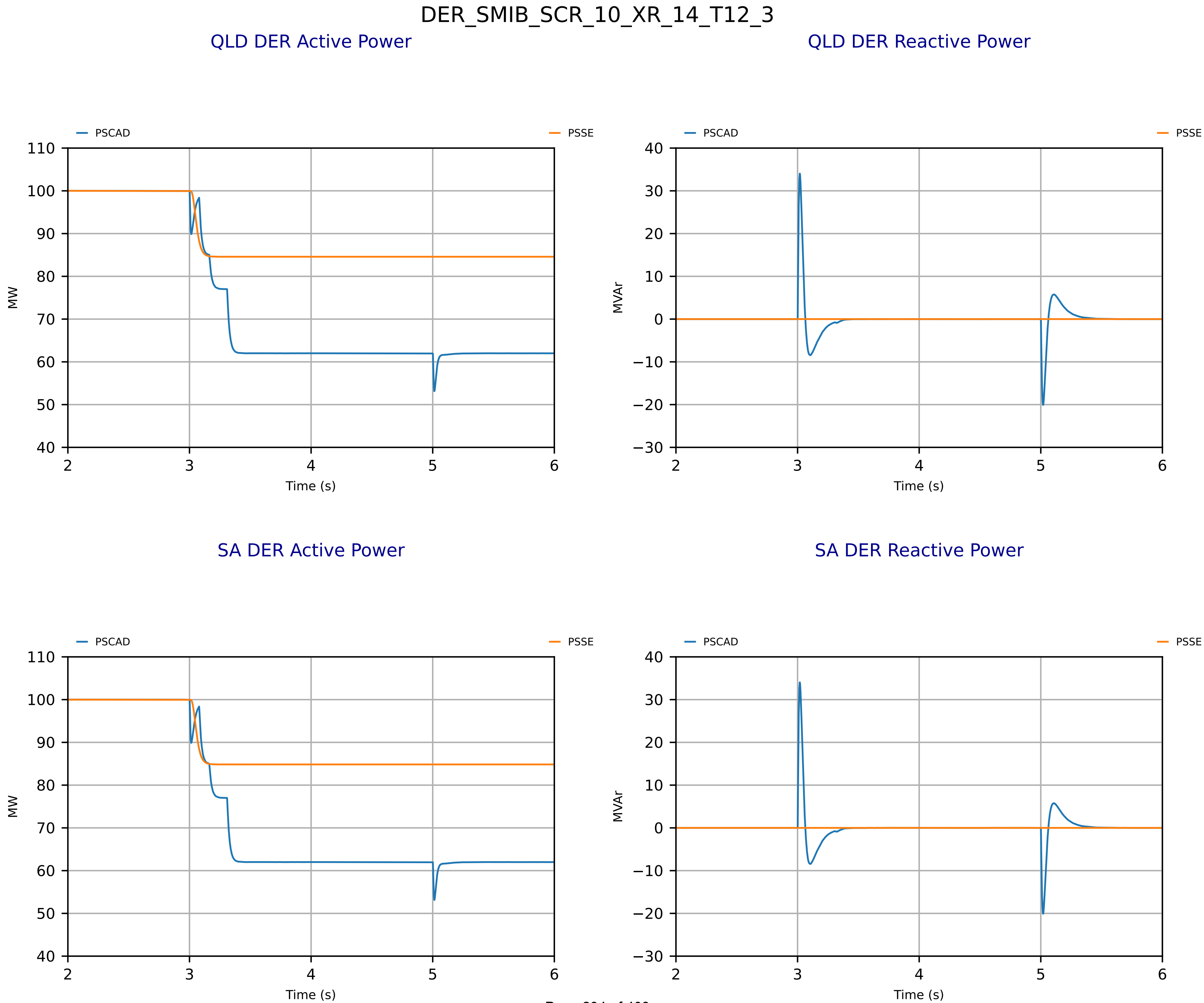
DER_SMIB_SCR_10_XR_14_T12_1





DER_SMIB_SCR_10_XR_14_T12_2




DER_SMIB_SCR_10_XR_14_T12_3
QLD DER Active Power
QLD DER Reactive Power
SA DER Active Power
SA DER Reactive Power
PSCAD
PSSE
MW
MVAr
Time (s)

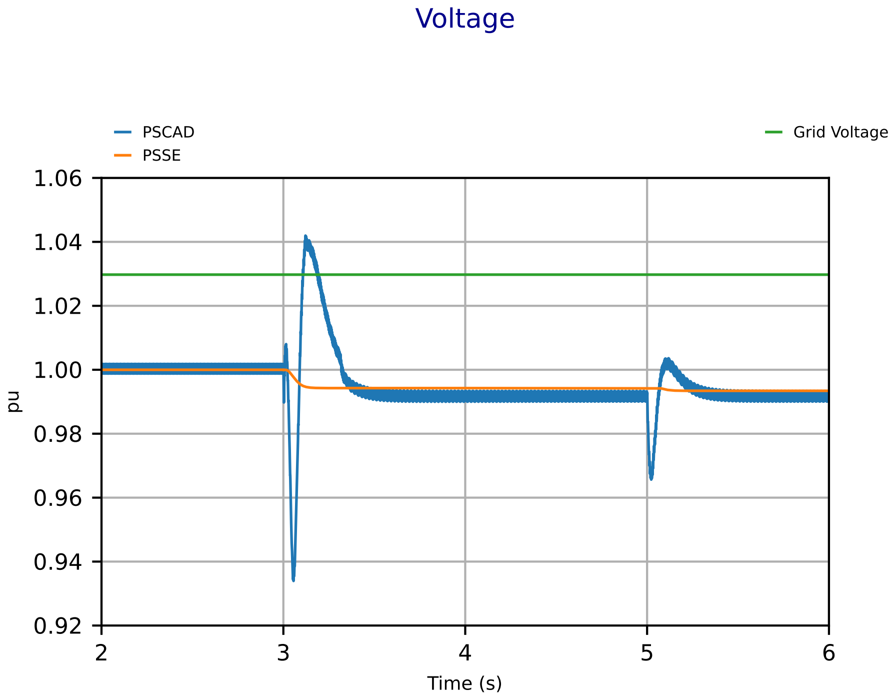
DER SMIB

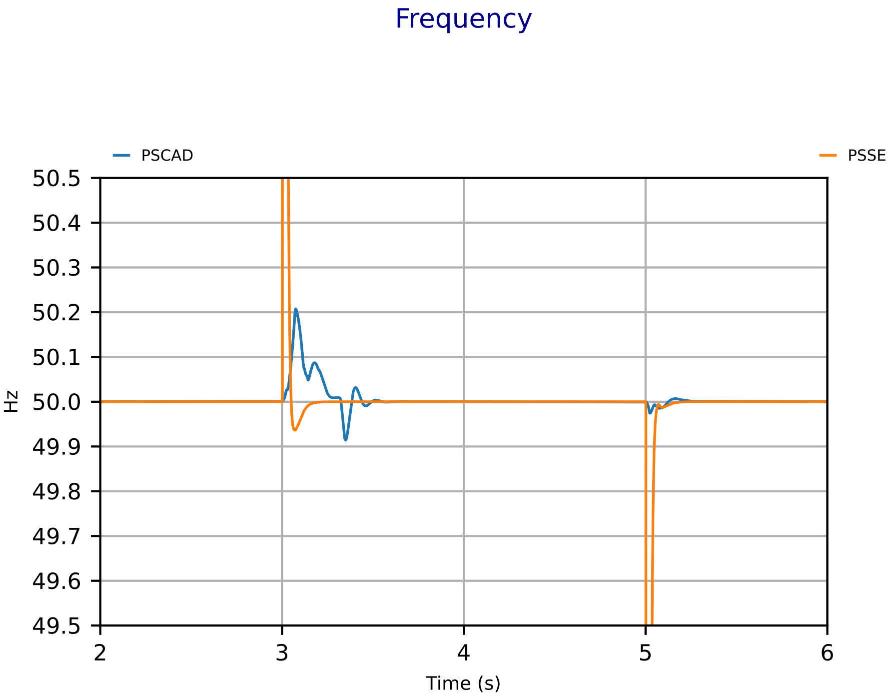
SCR = 10, X/R = 14

Test #13:

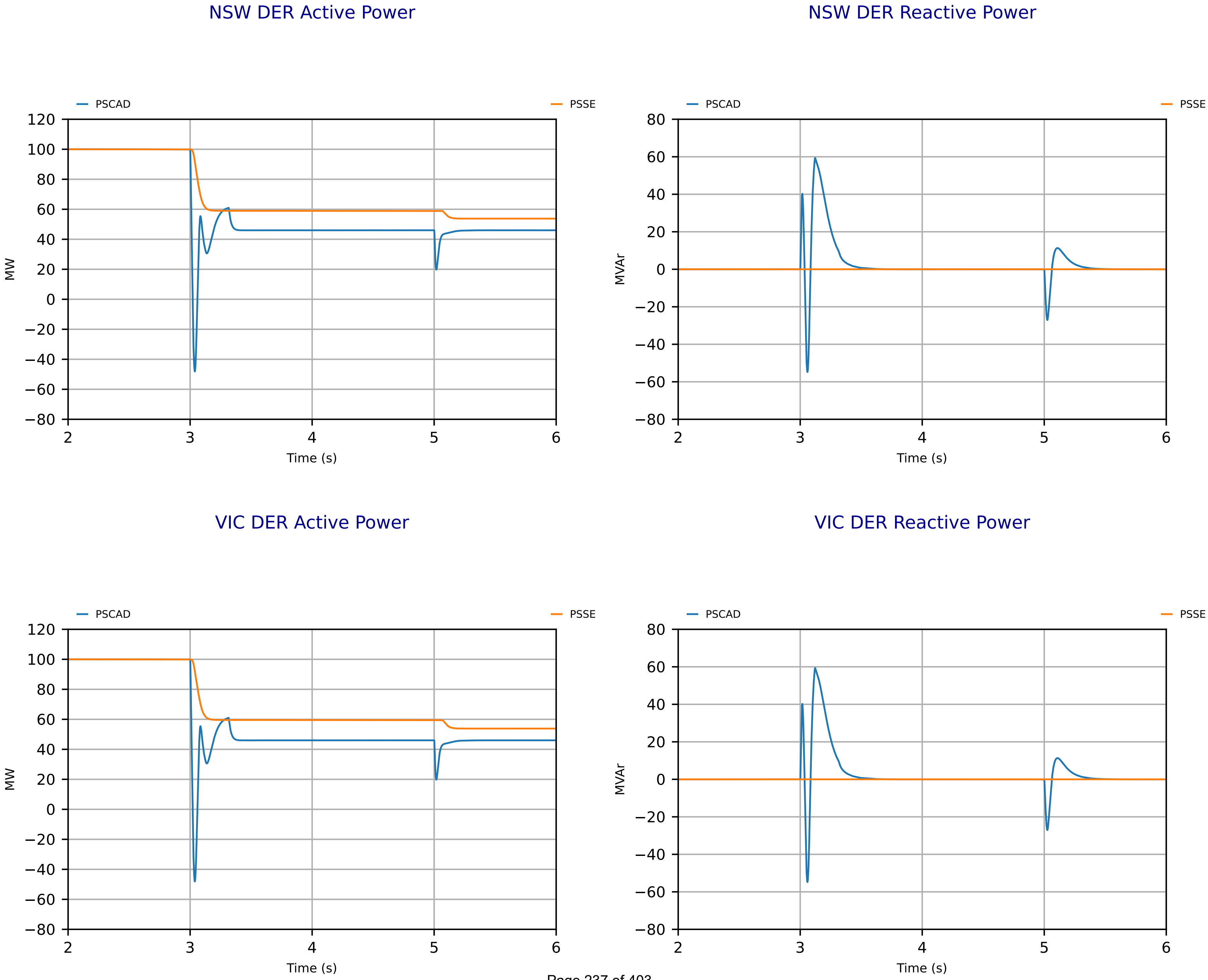
120° phase angle step

DER_SMIB_SCR_10_XR_14_T13_1

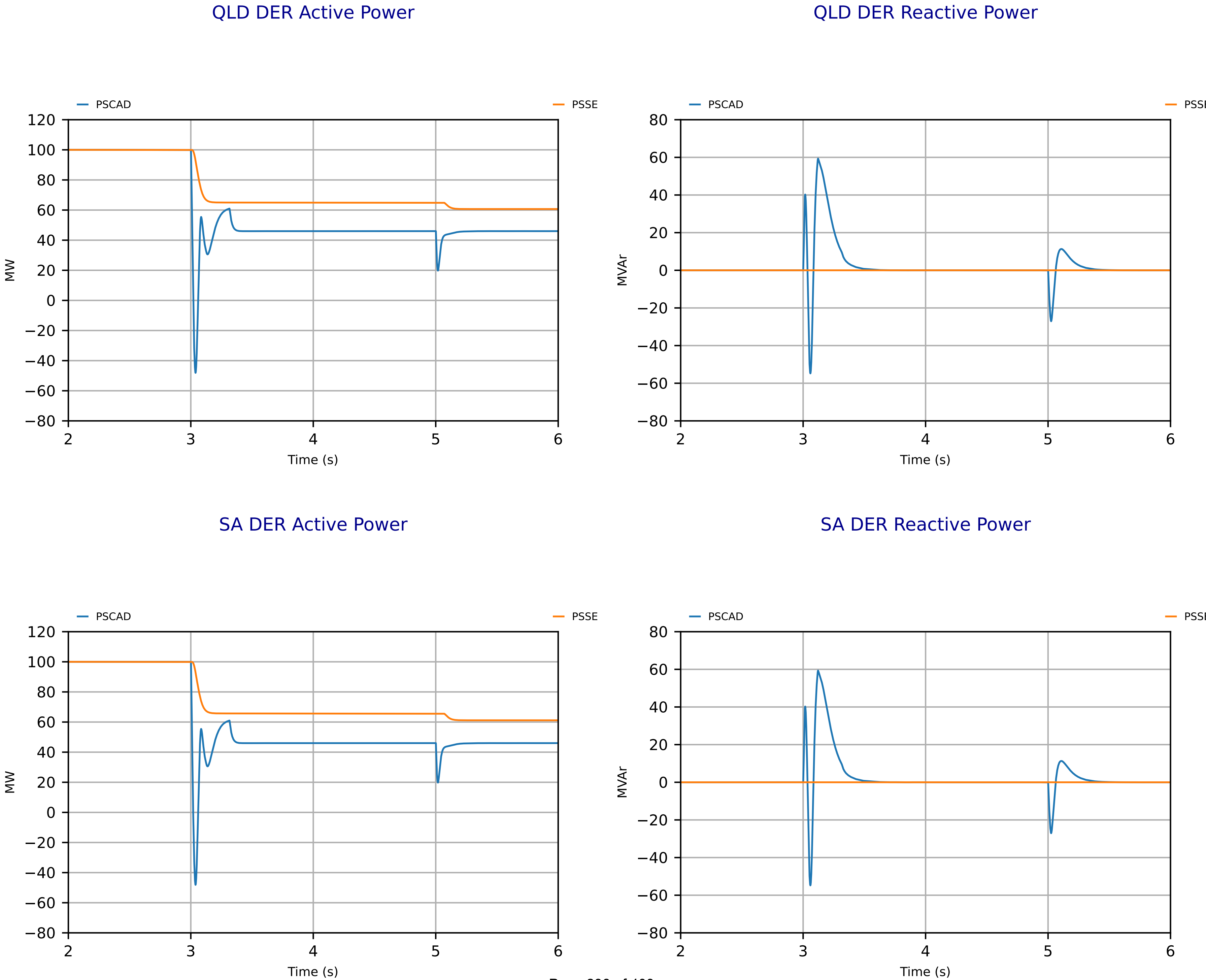




DER_SMIB_SCR_10_XR_14_T13_2



DER_SMIB_SCR_10_XR_14_T13_3



8 Appendix C: CMLD test results

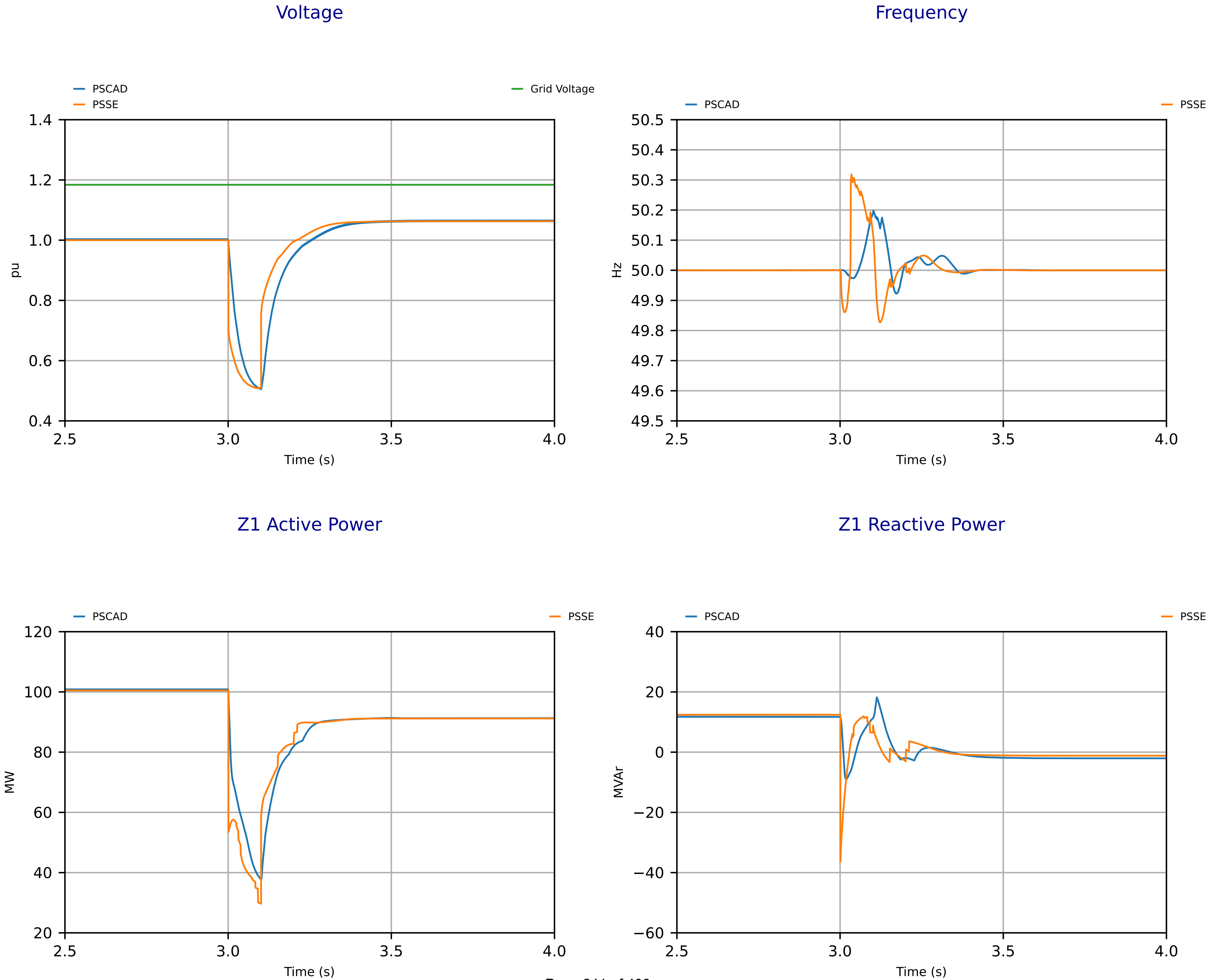
CMLD SMIB

SCR = 3, X/R = 3

Test #2:

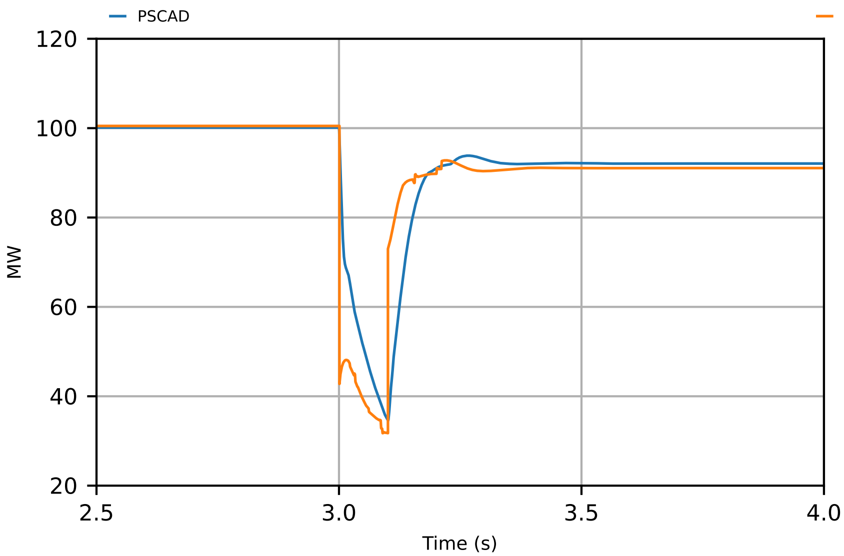
LLG fault for 100 ms

CMLD_SMIB_SCR_3_XR_3_T2_1

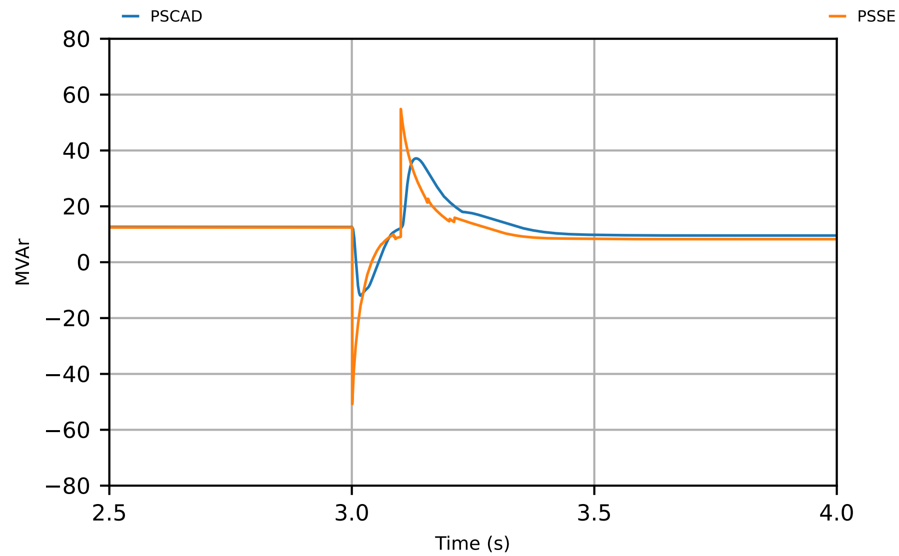


CMLD_SMIB_SCR_3_XR_3_T2_2

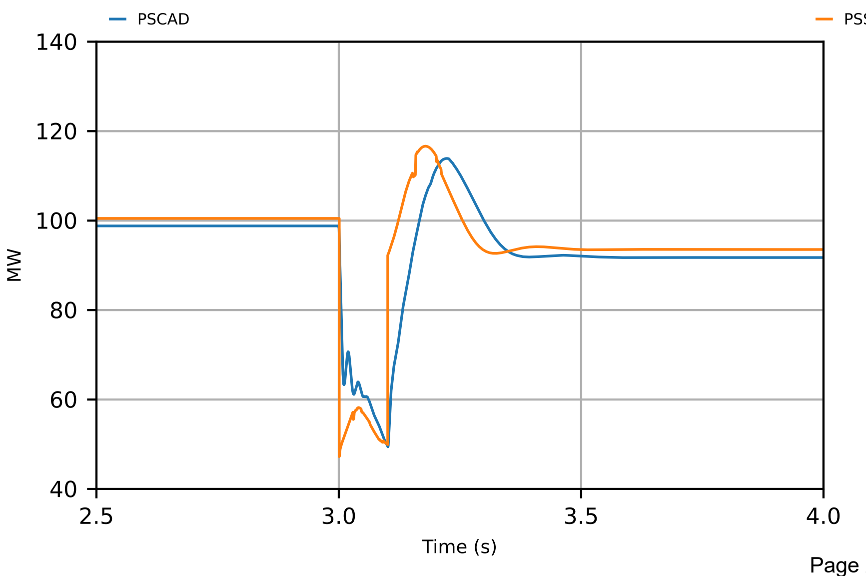
Z20 Active Power



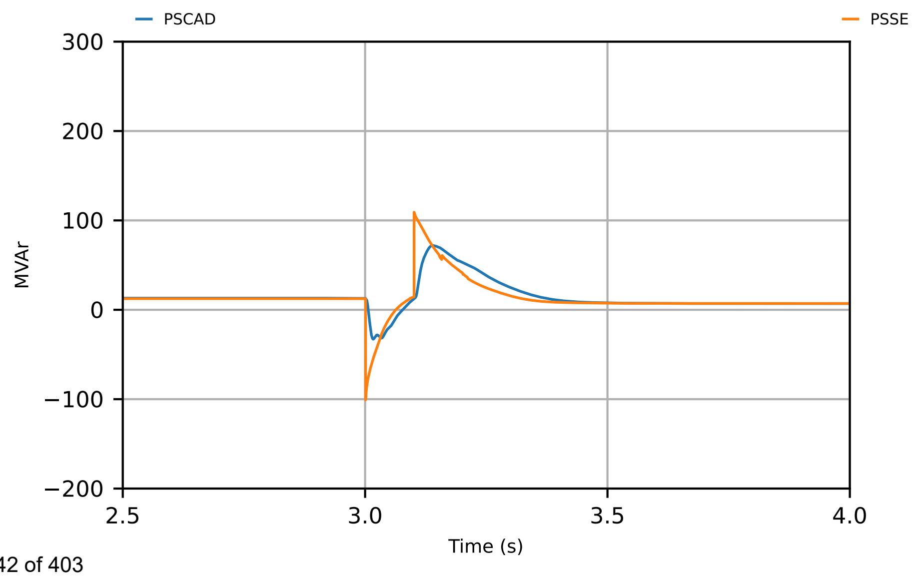
Z20 Reactive Power



Z22 Active Power

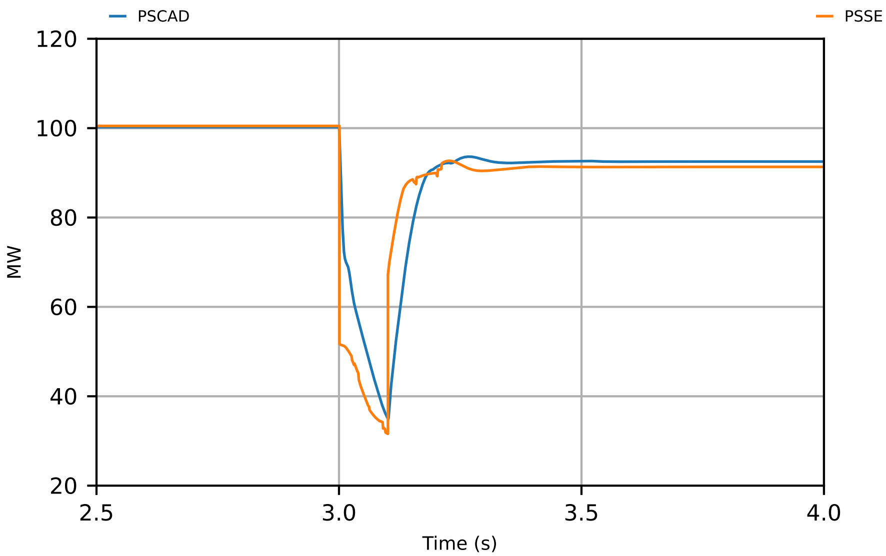


Z22 Reactive Power

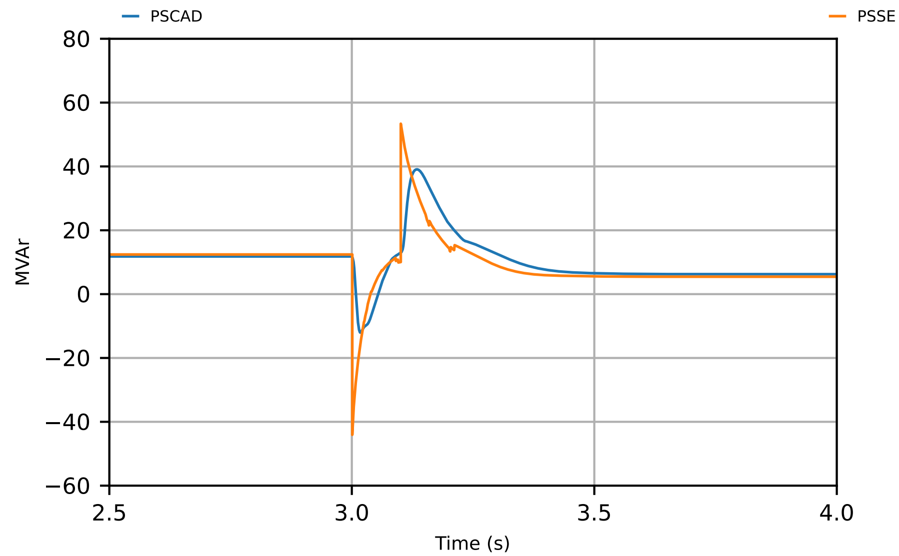


CMLD_SMIB_SCR_3_XR_3_T2_3

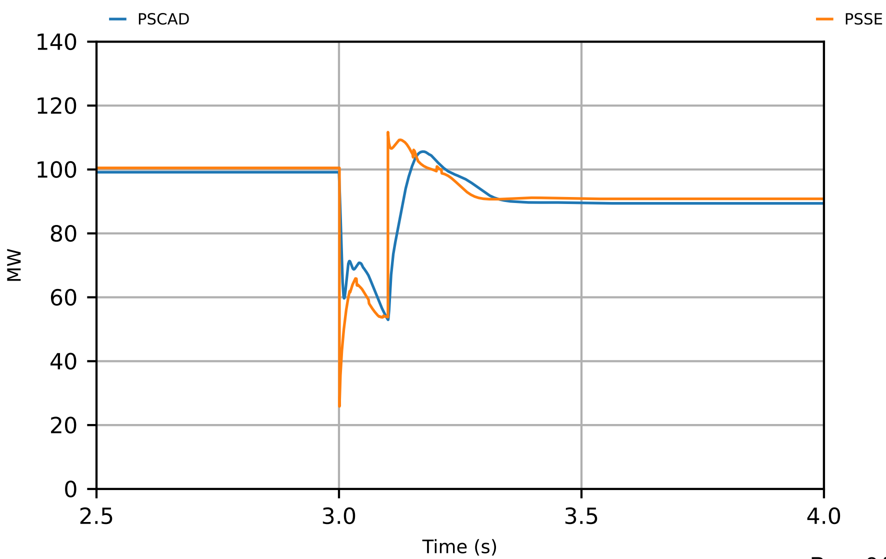
Z29 Active Power



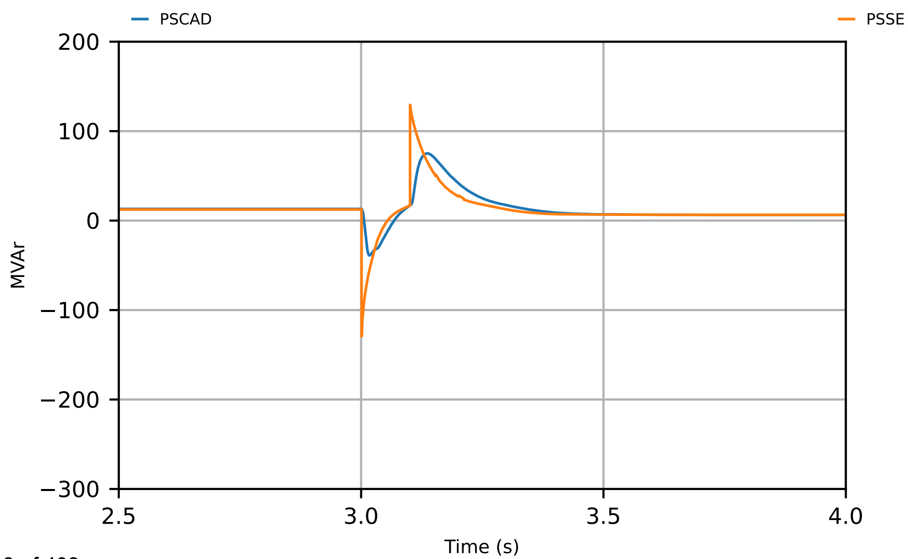
Z29 Reactive Power



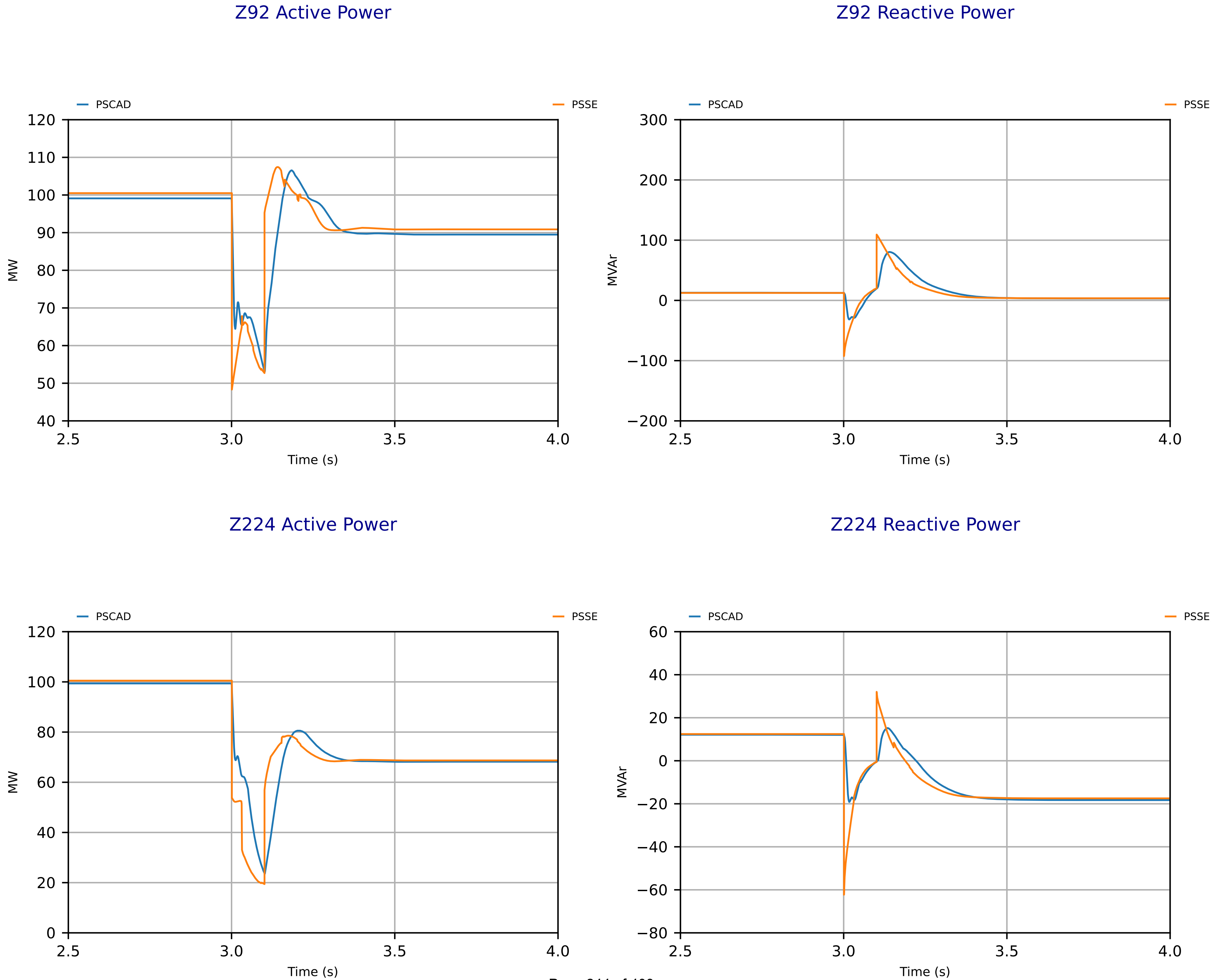
Z82 Active Power



Z82 Reactive Power



CMLD_SMIB_SCR_3_XR_3_T2_4



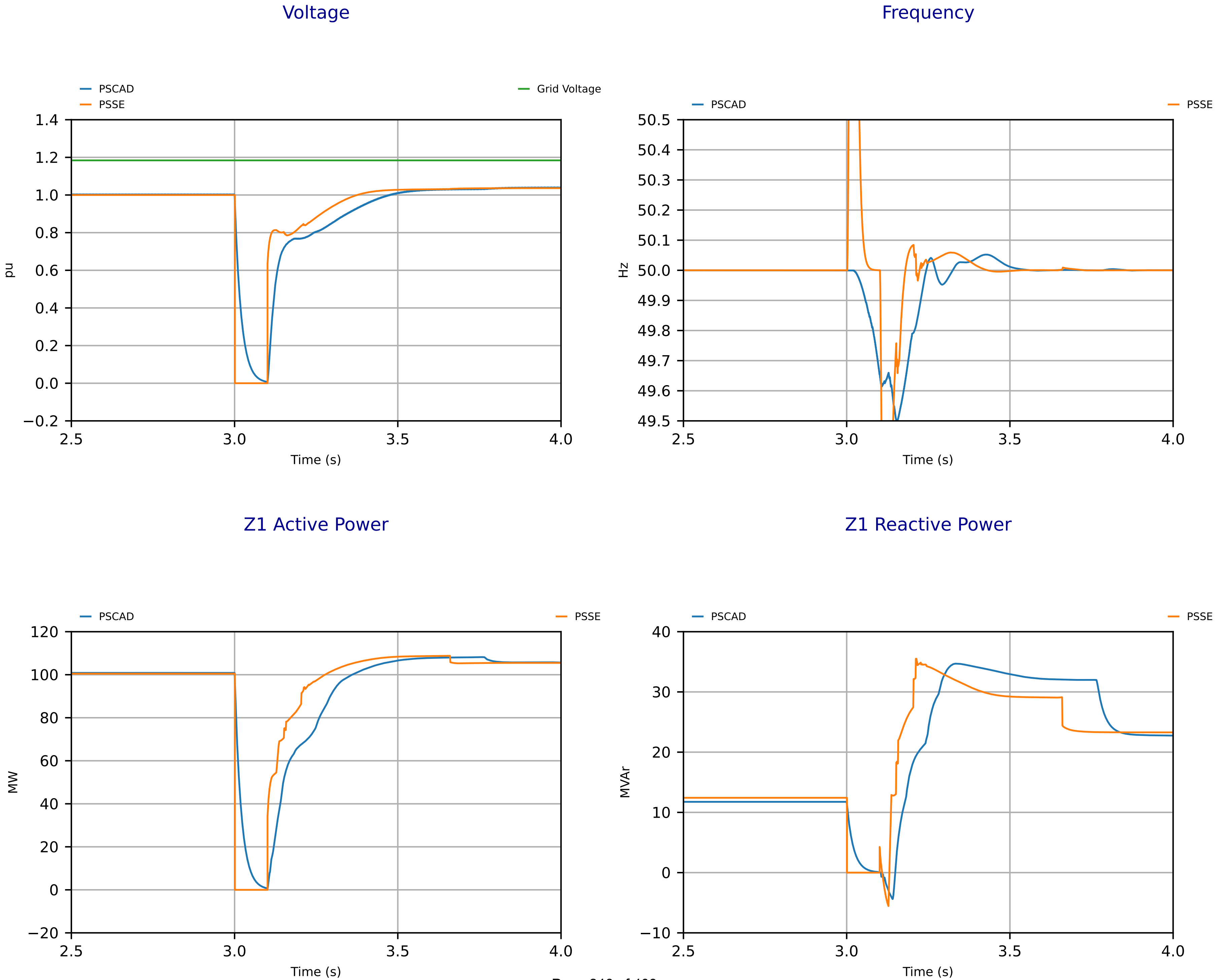
CMLD SMIB

SCR = 3, X/R = 3

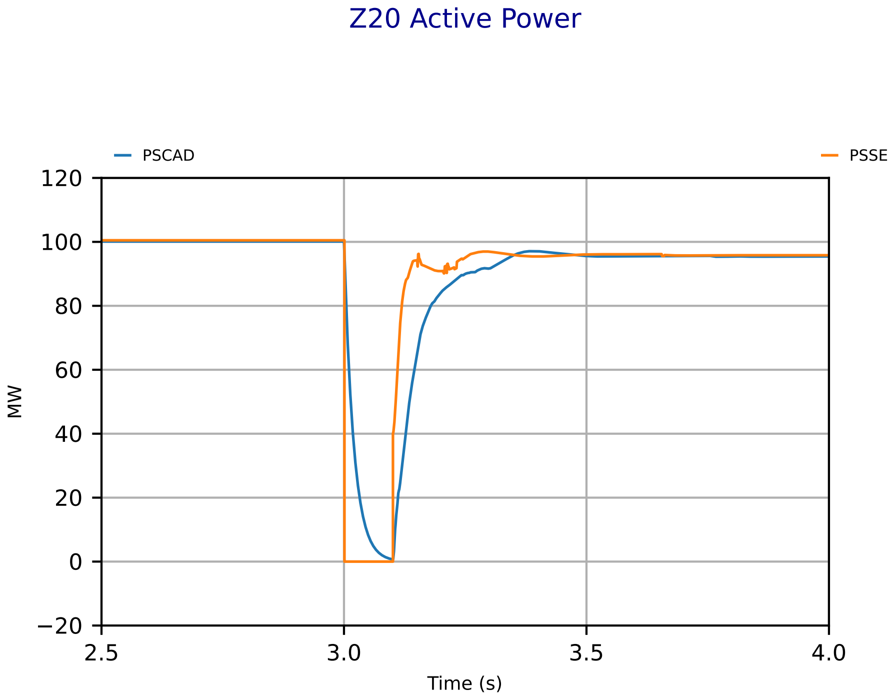
Test #3:

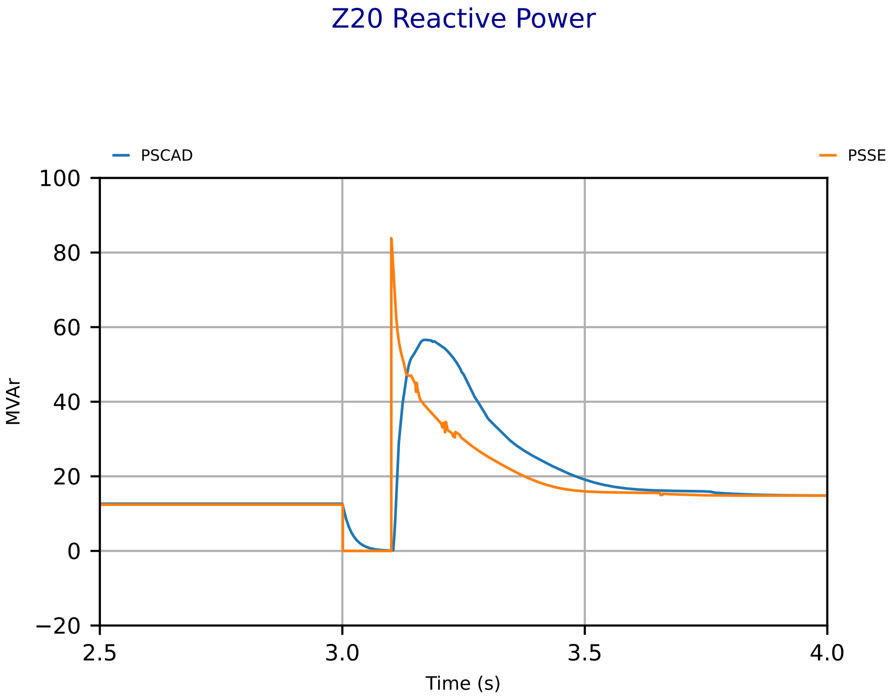
3PH-G fault for 100 ms

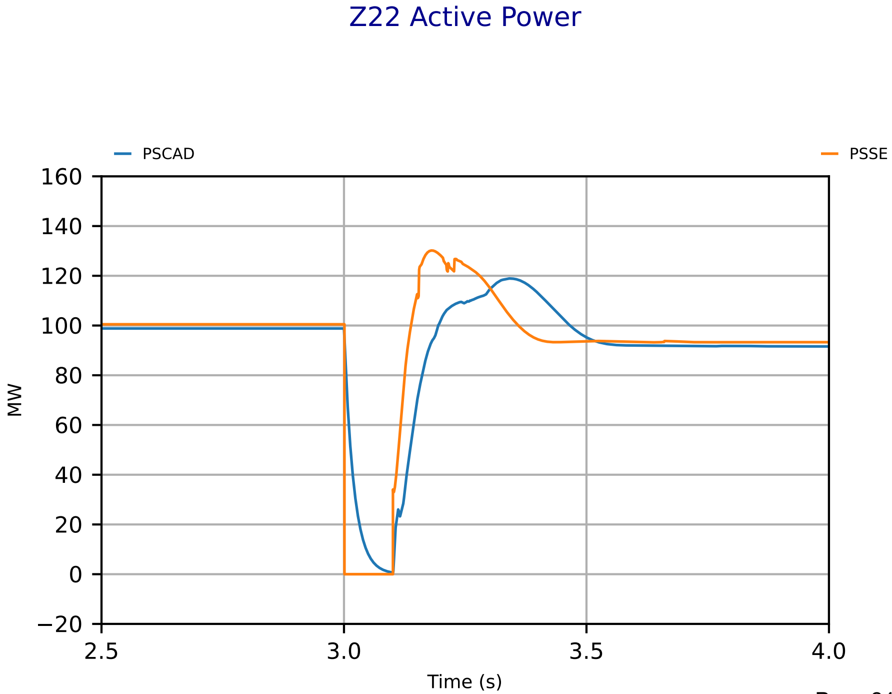
CMLD_SMIB_SCR_3_XR_3_T3_1

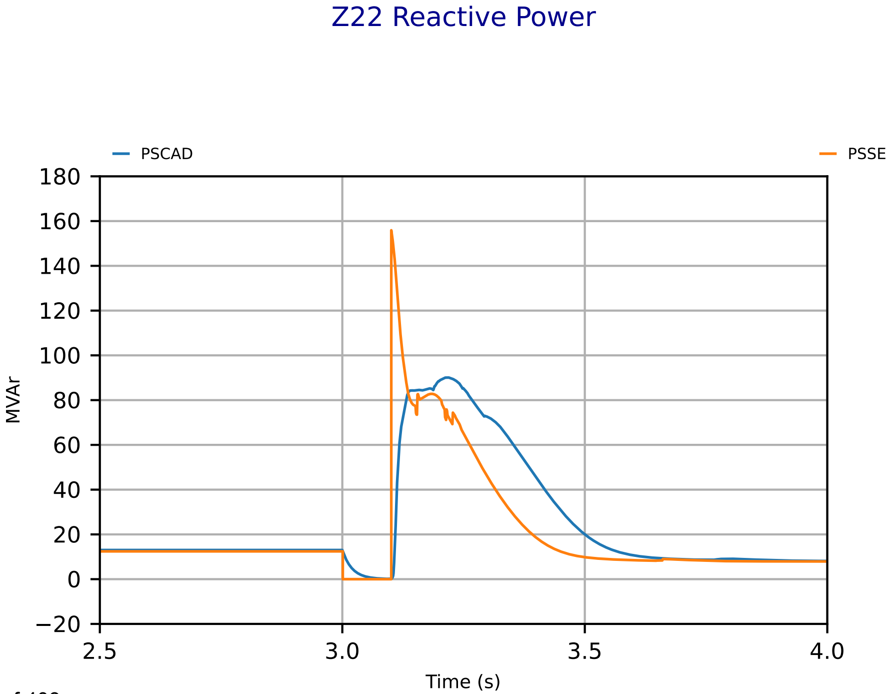


CMLD_SMIB_SCR_3_XR_3_T3_2

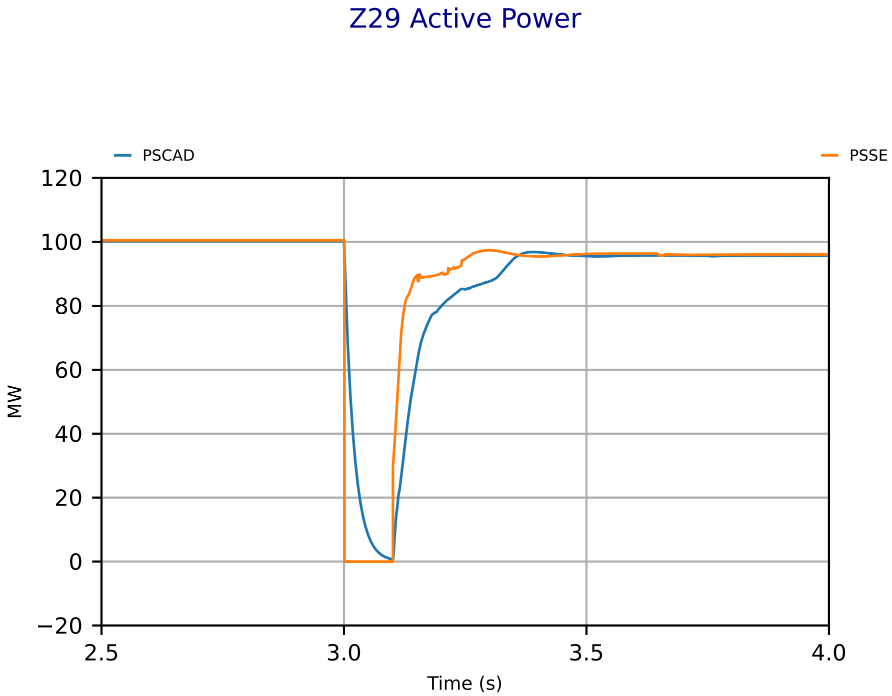


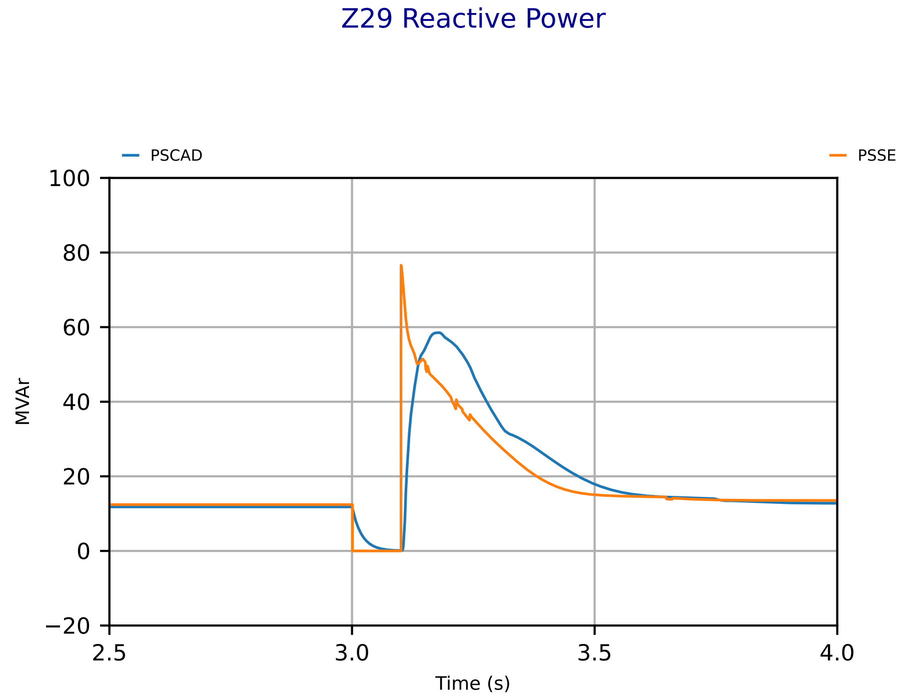


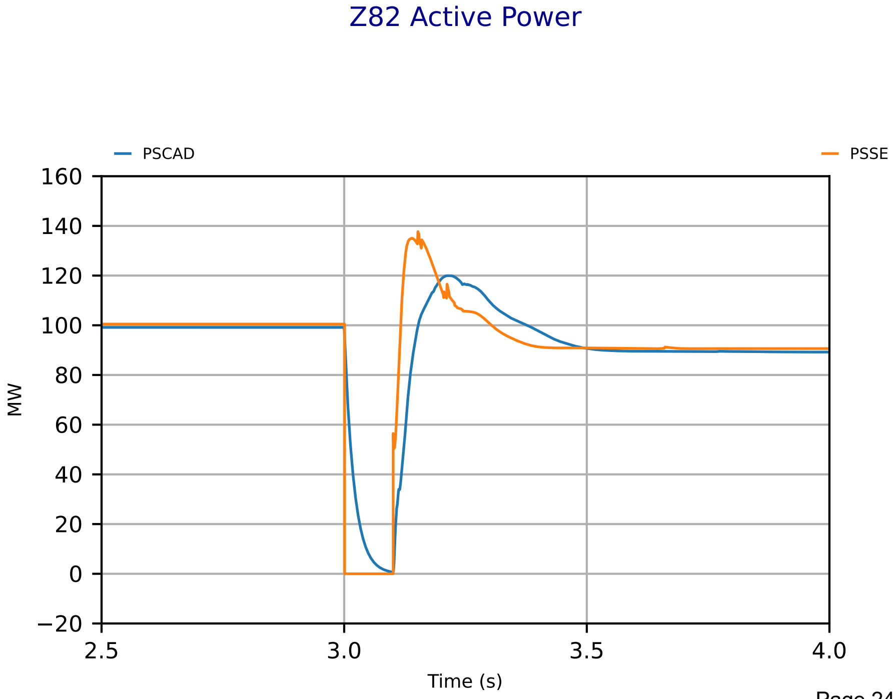


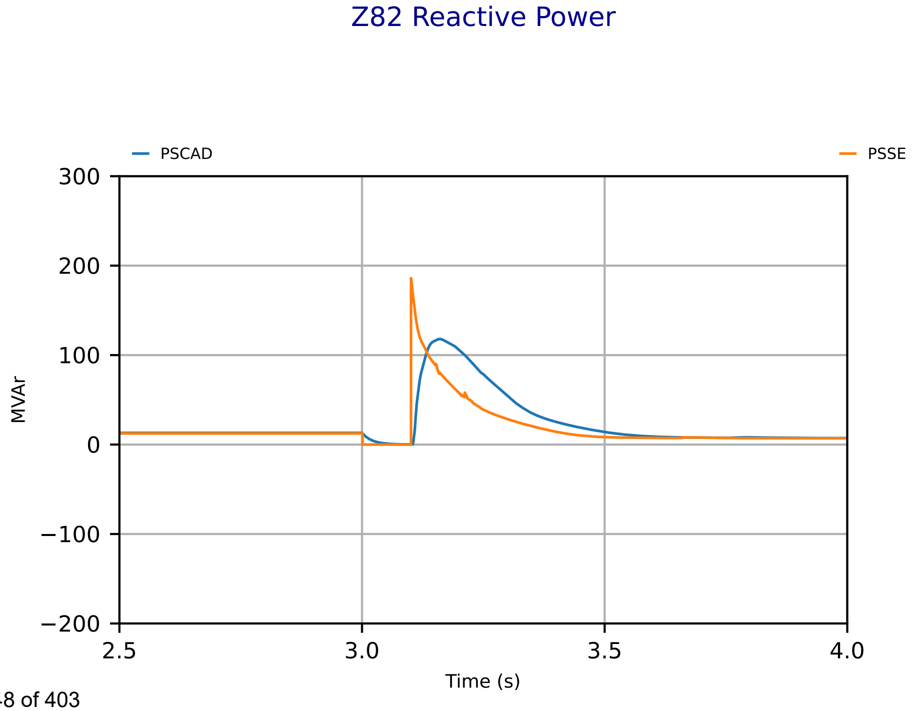


CMLD_SMIB_SCR_3_XR_3_T3_3

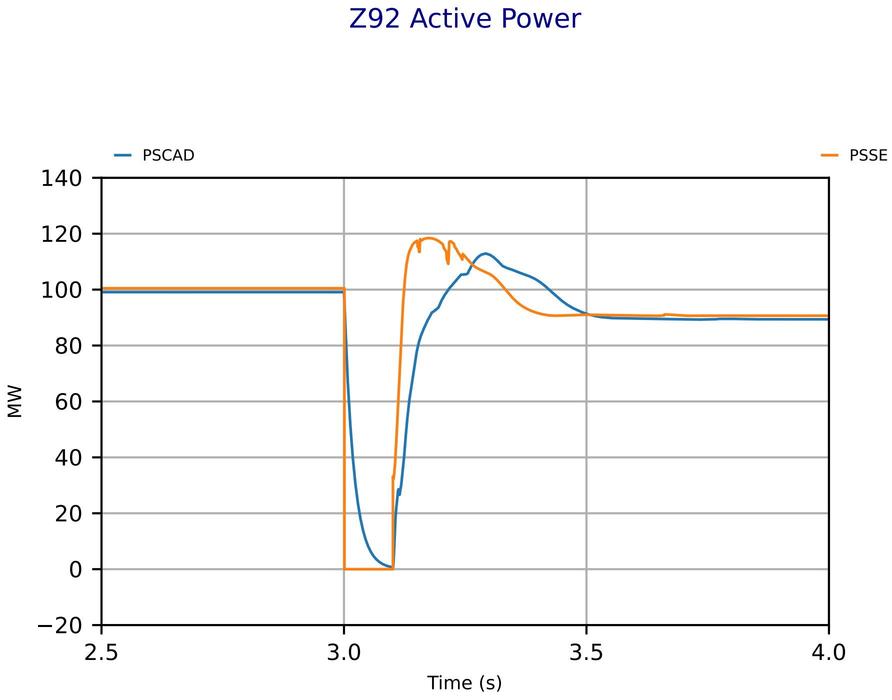


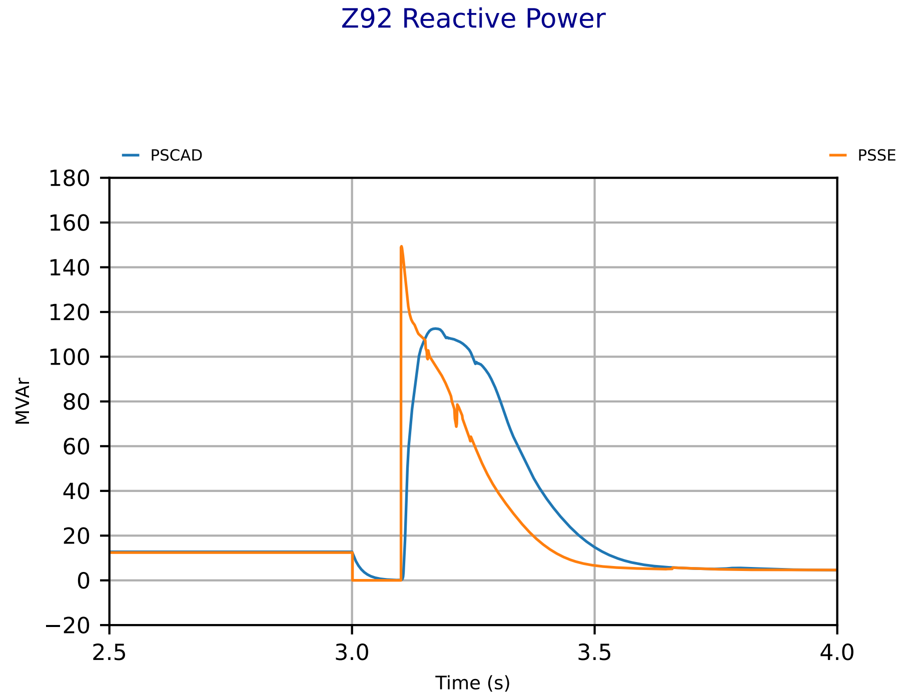


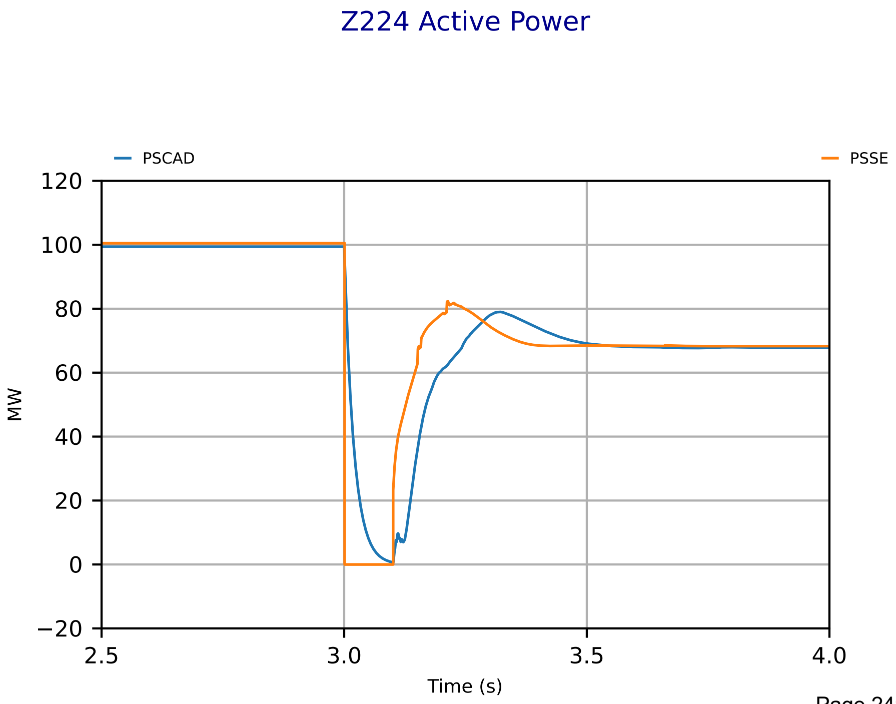


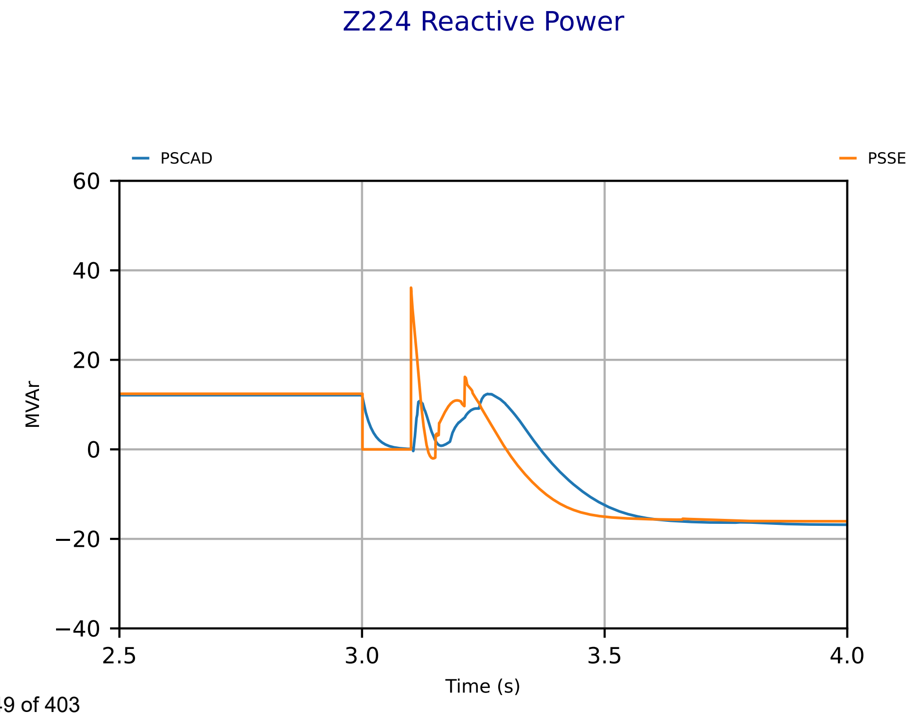


CMLD_SMIB_SCR_3_XR_3_T3_4









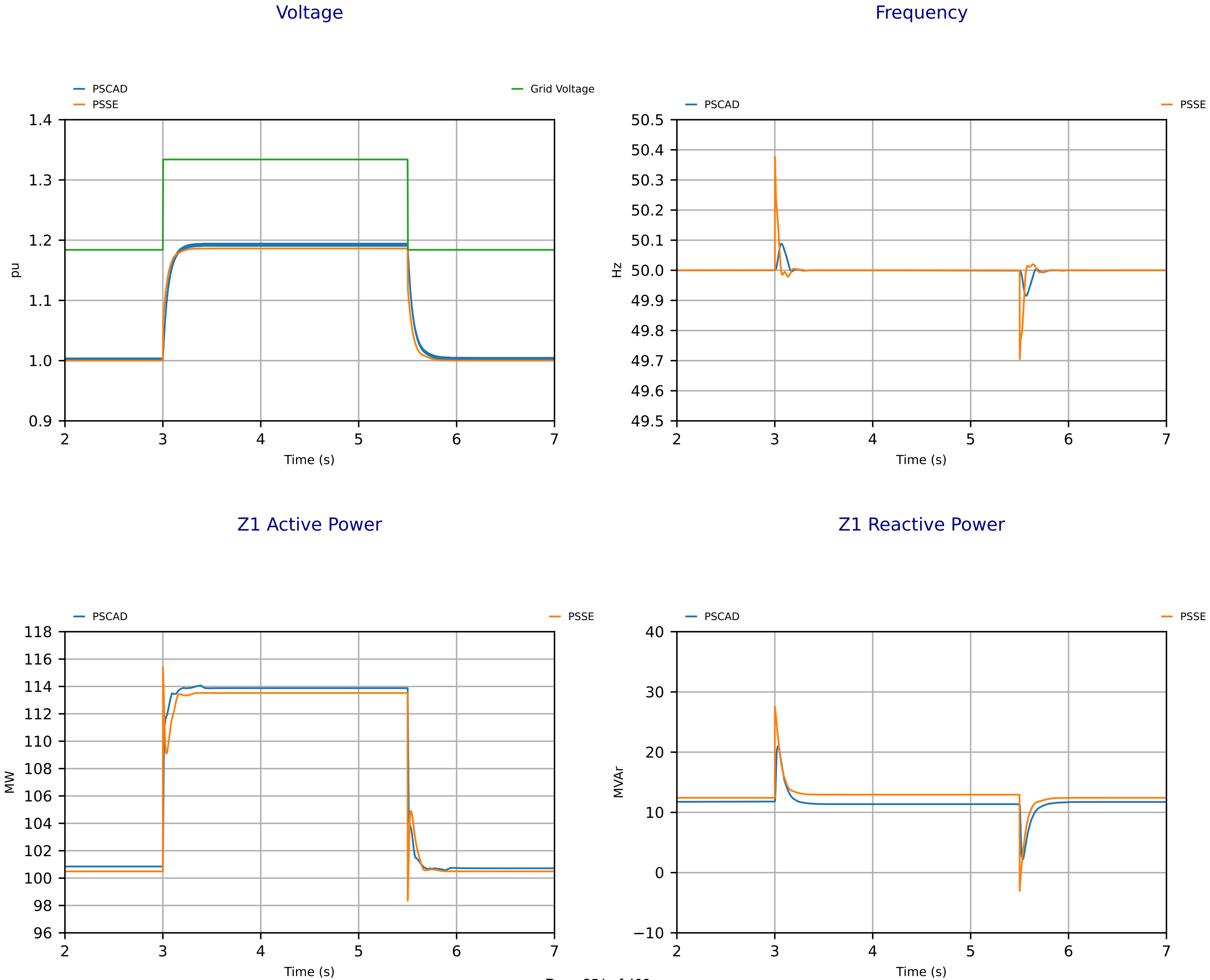
CMLD SMIB

SCR = 3, X/R = 3

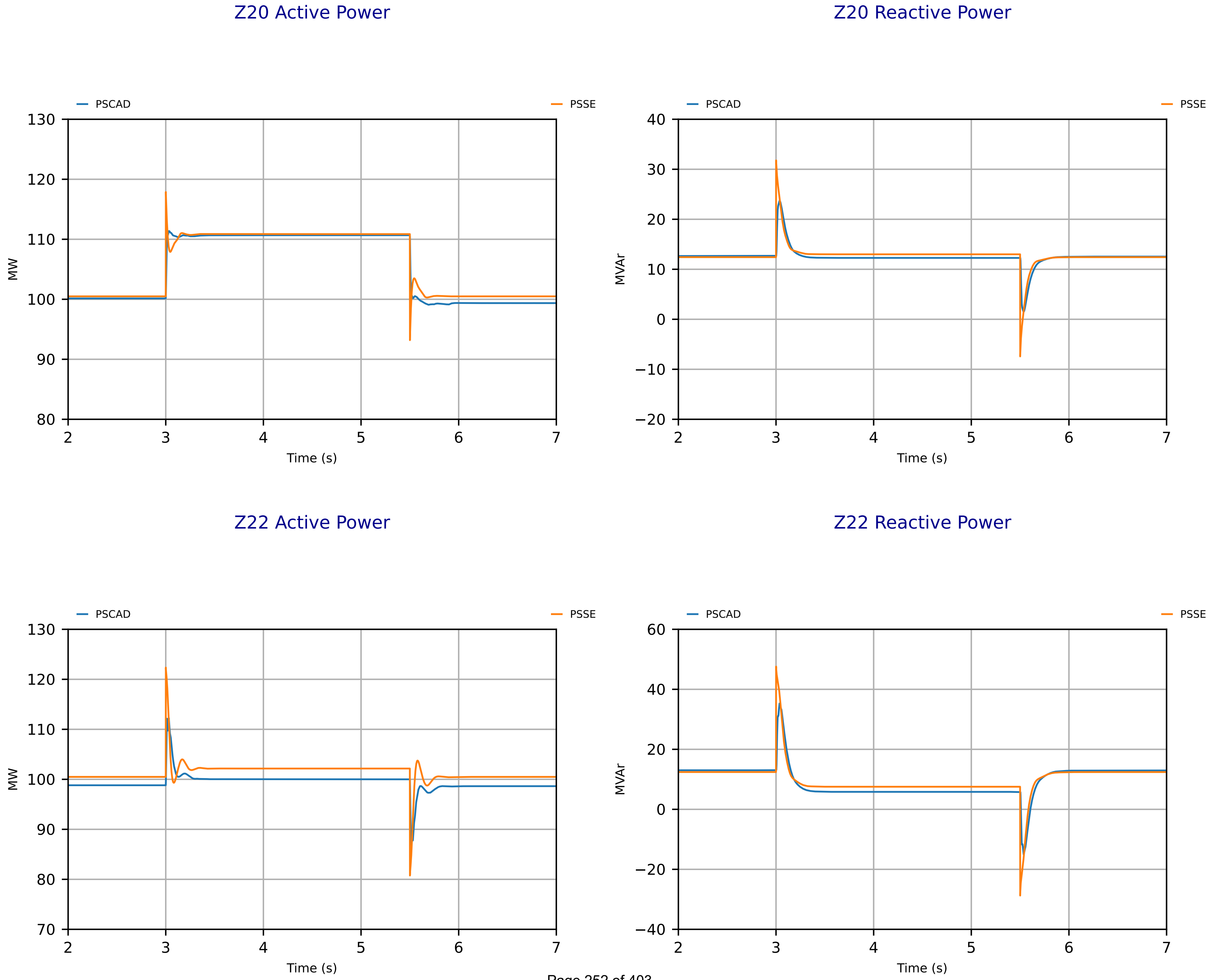
Test #4:

~115% Voltage disturbance for 2.5 s

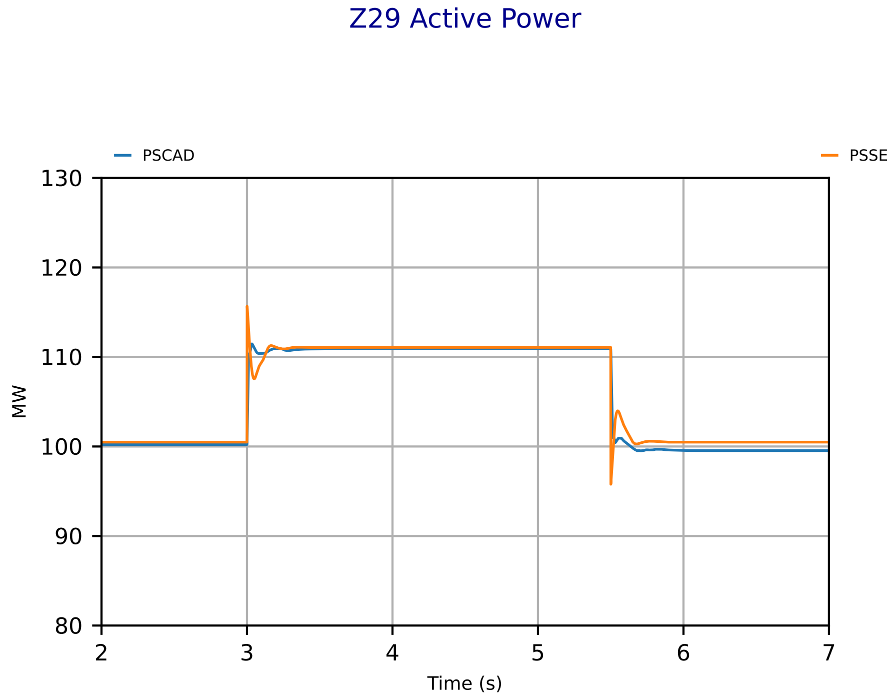
CMLD_SMIB_SCR_3_XR_3_T4_1

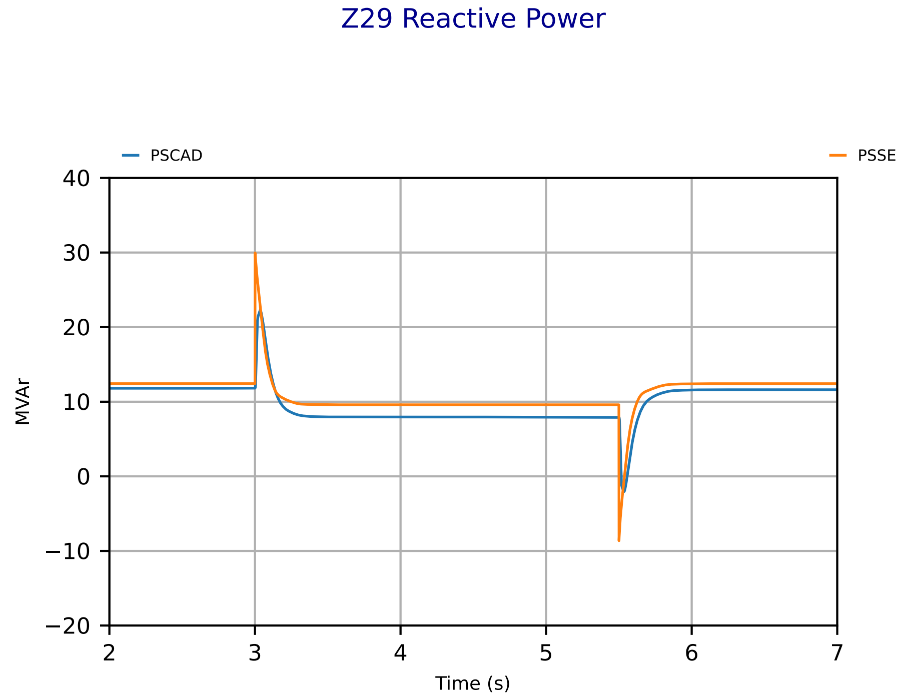


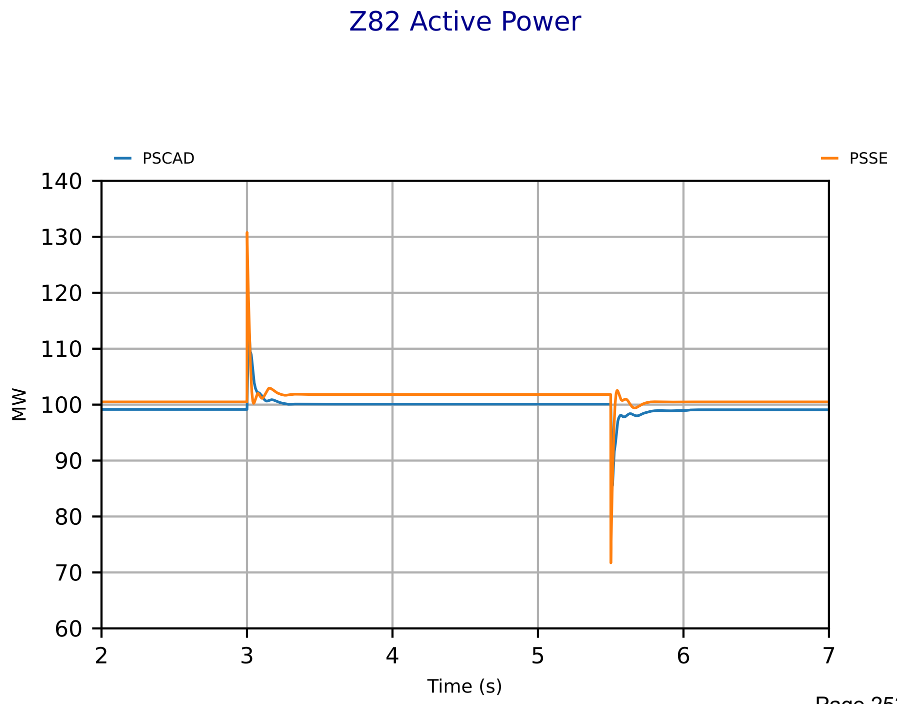
CMLD_SMIB_SCR_3_XR_3_T4_2

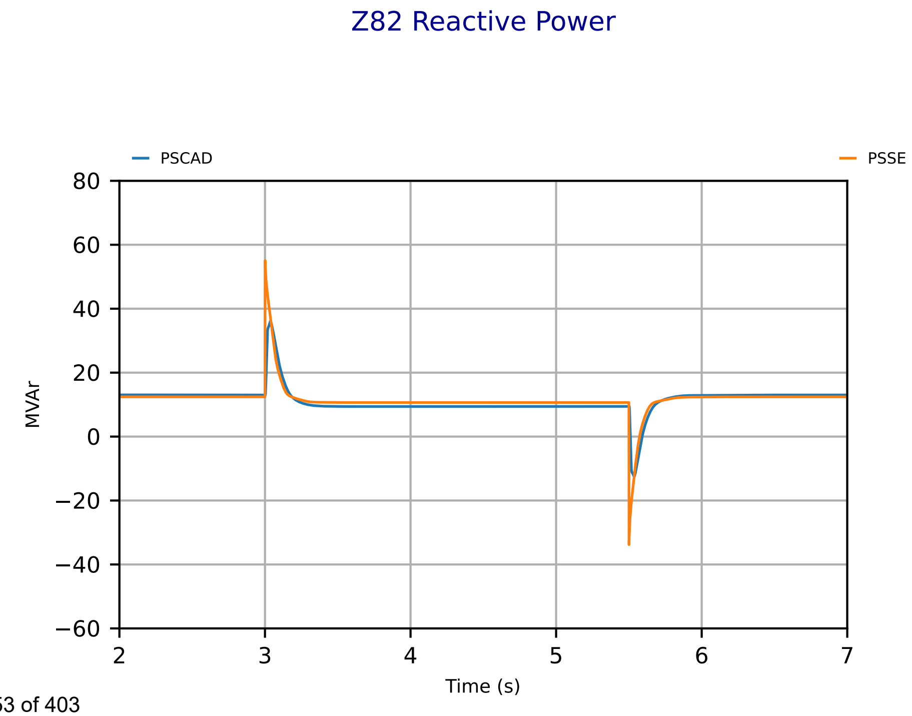


CMLD_SMIB_SCR_3_XR_3_T4_3



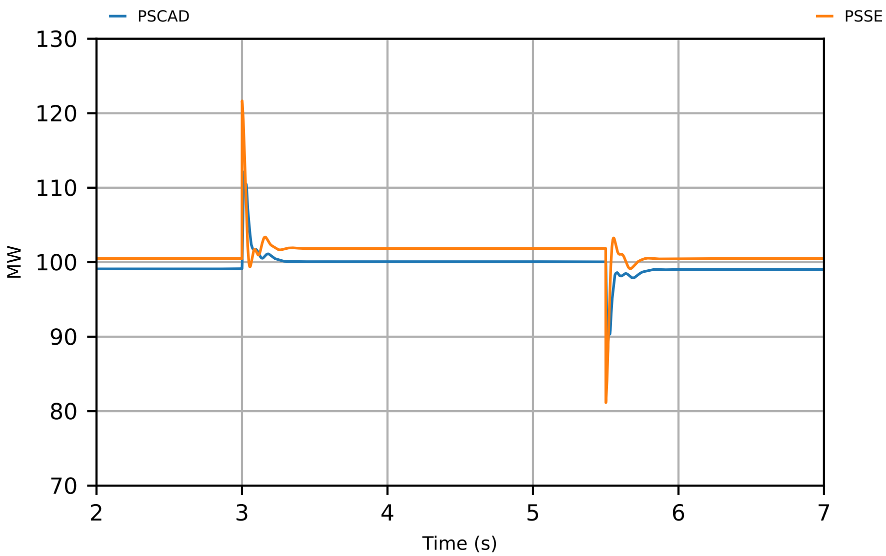




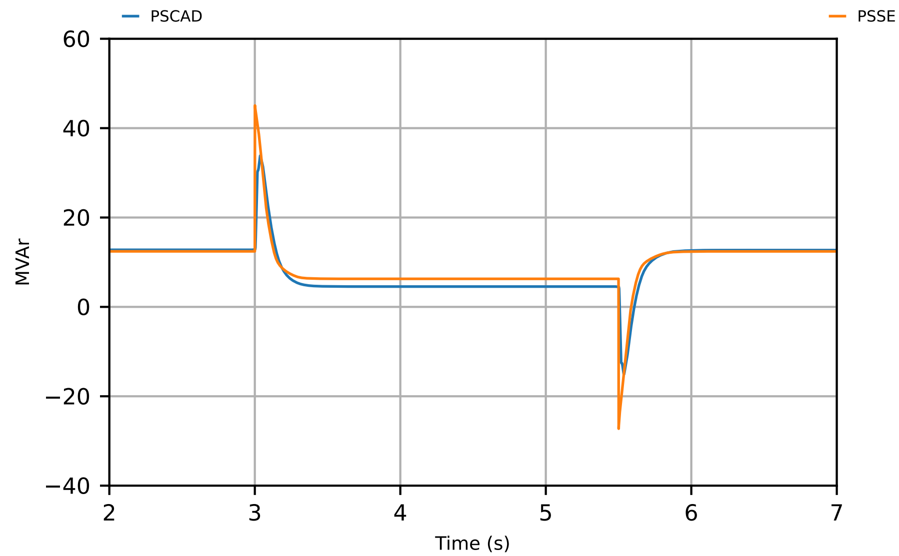


CMLD_SMIB_SCR_3_XR_3_T4_4

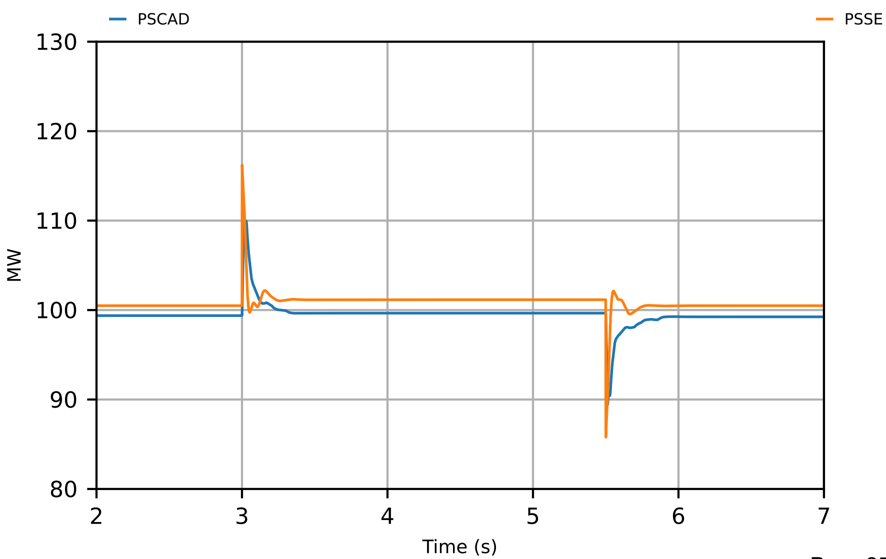
Z92 Active Power



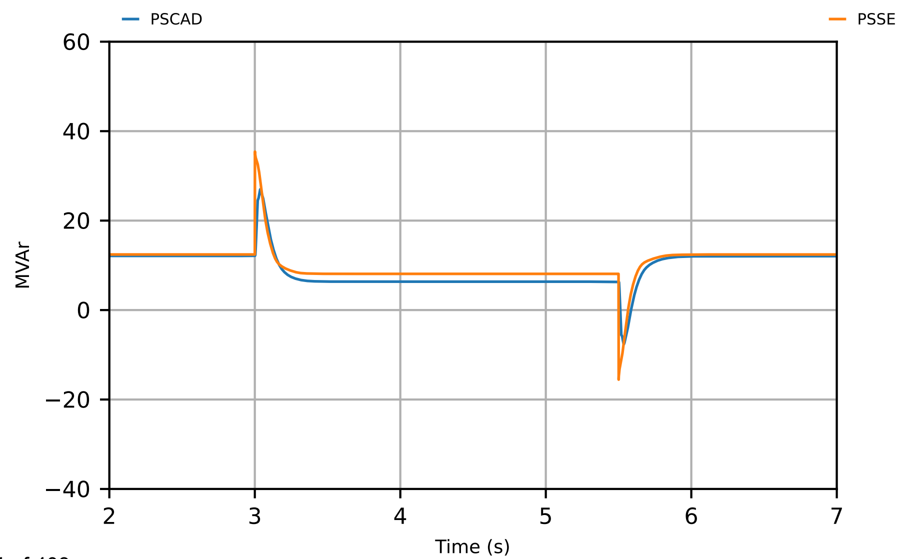
Z92 Reactive Power



Z224 Active Power



Z224 Reactive Power



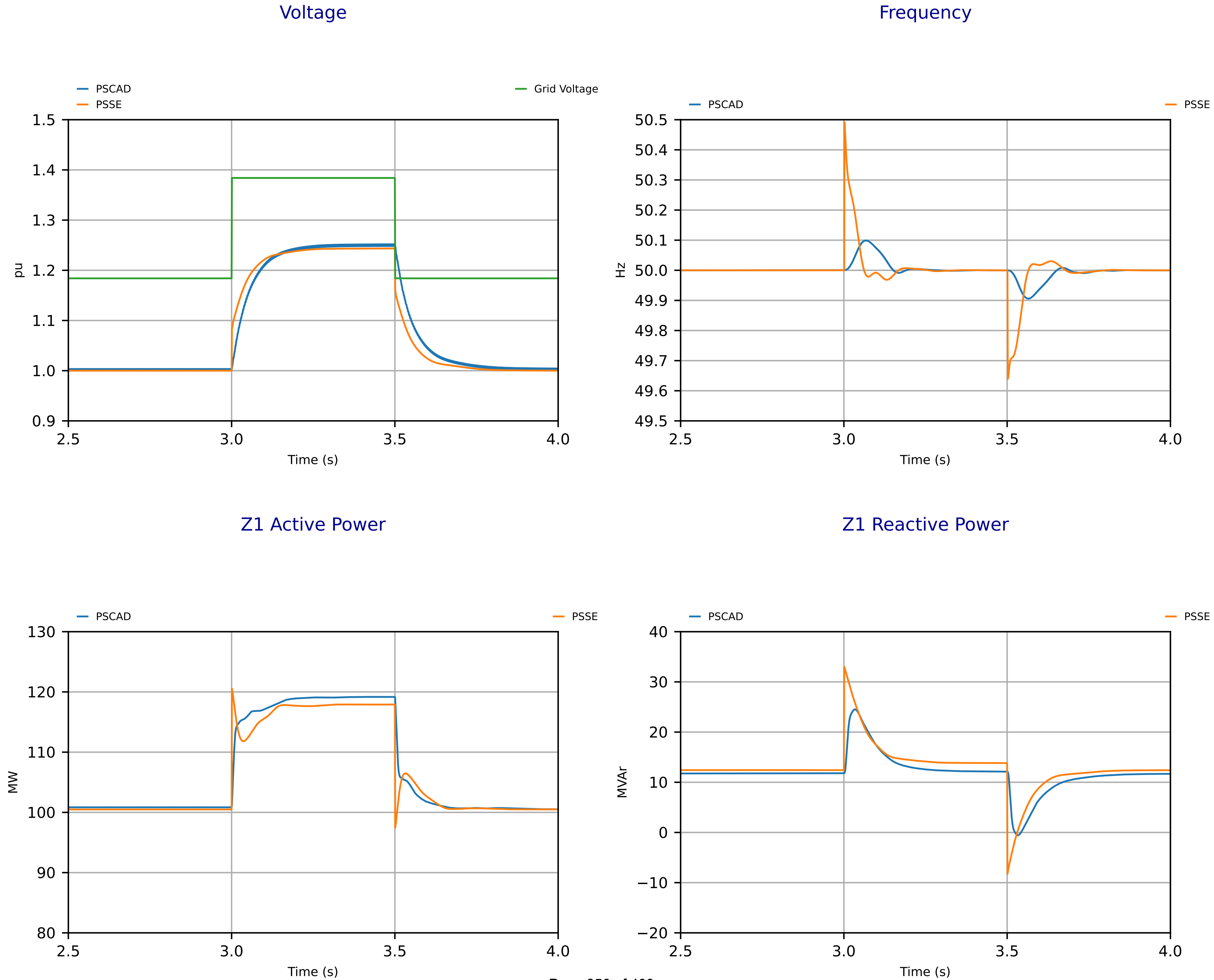
CMLD SMIB

SCR = 3, X/R = 3

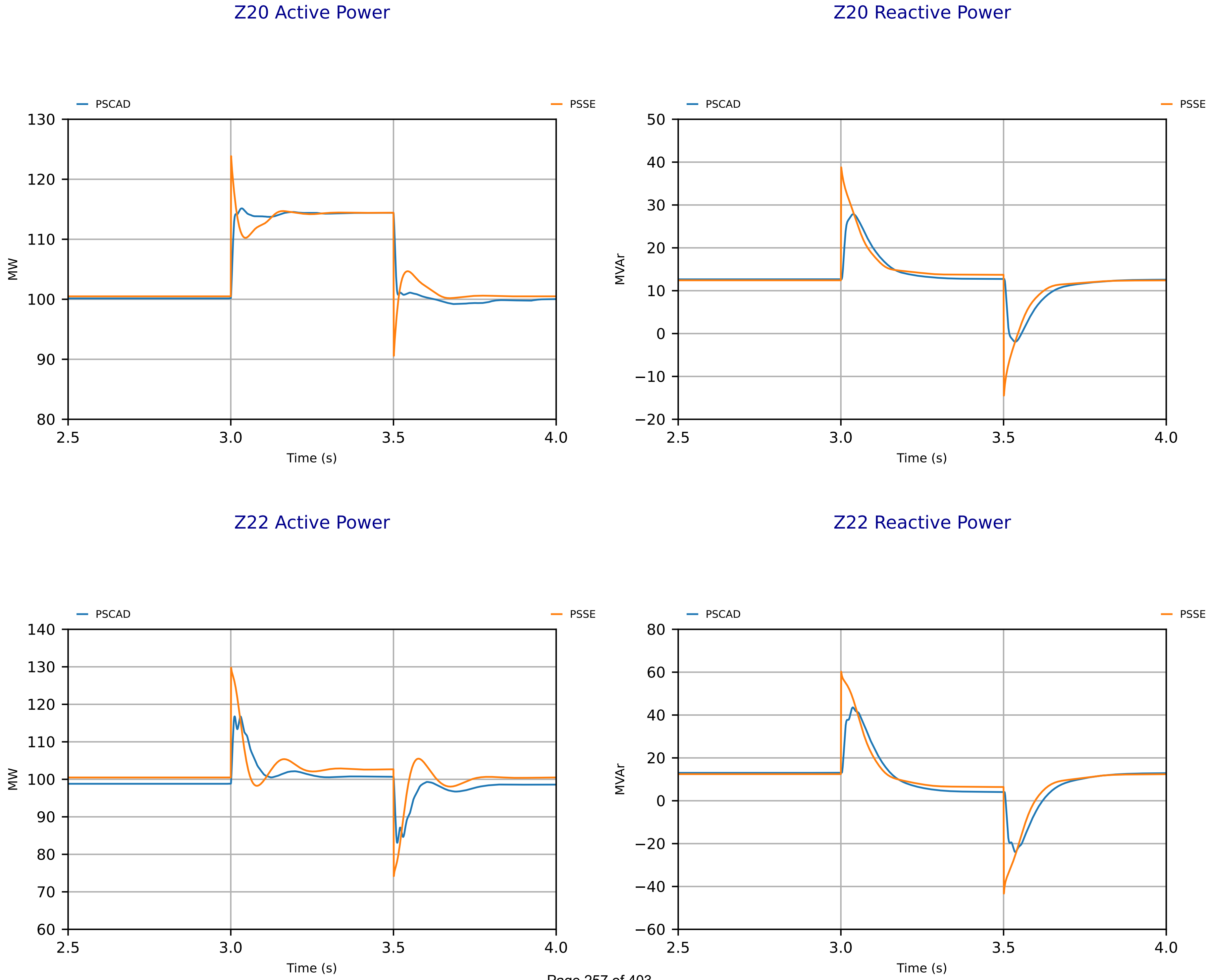
Test #5:

~120% Voltage disturbance for 500 ms

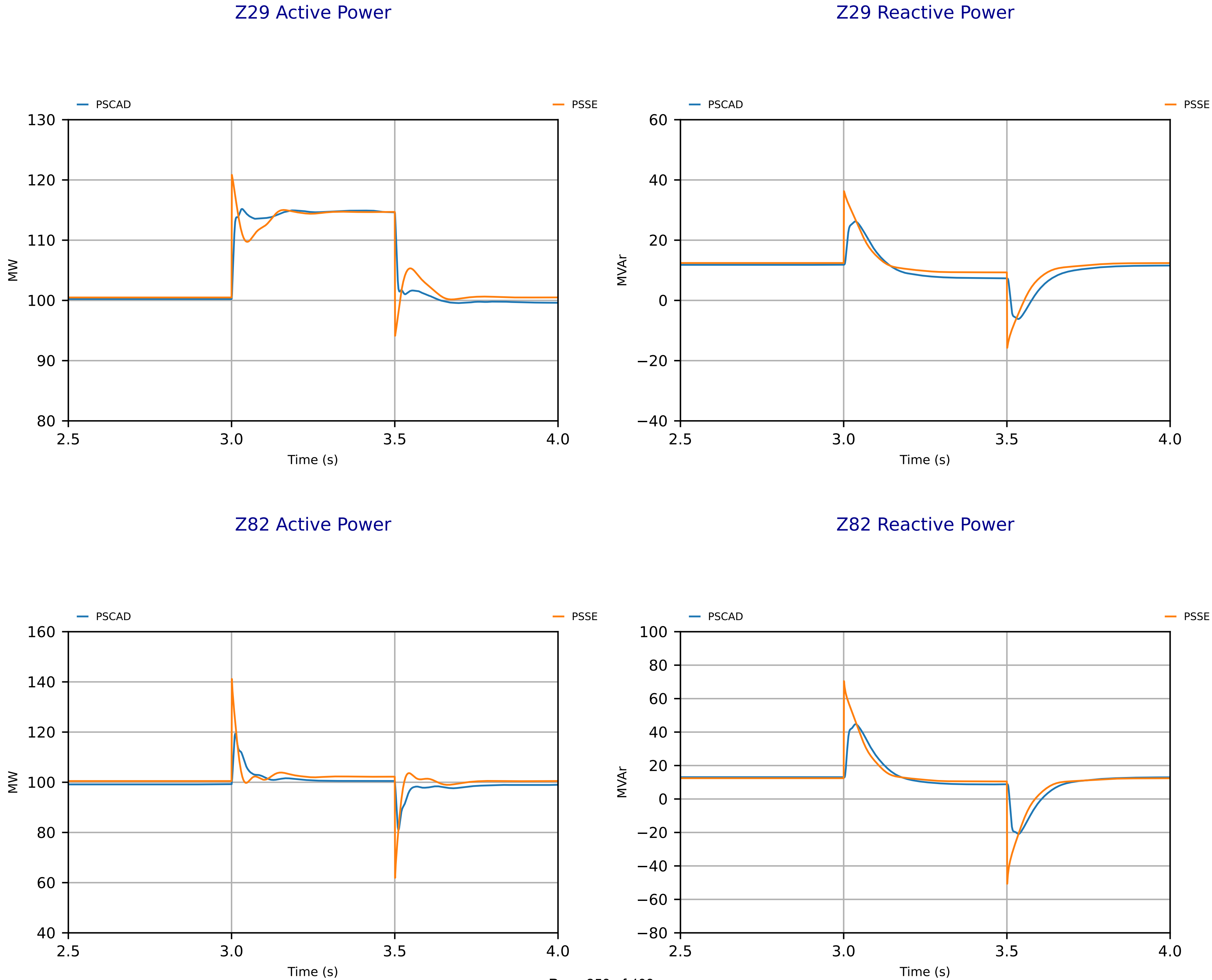
CMLD_SMIB_SCR_3_XR_3_T5_1



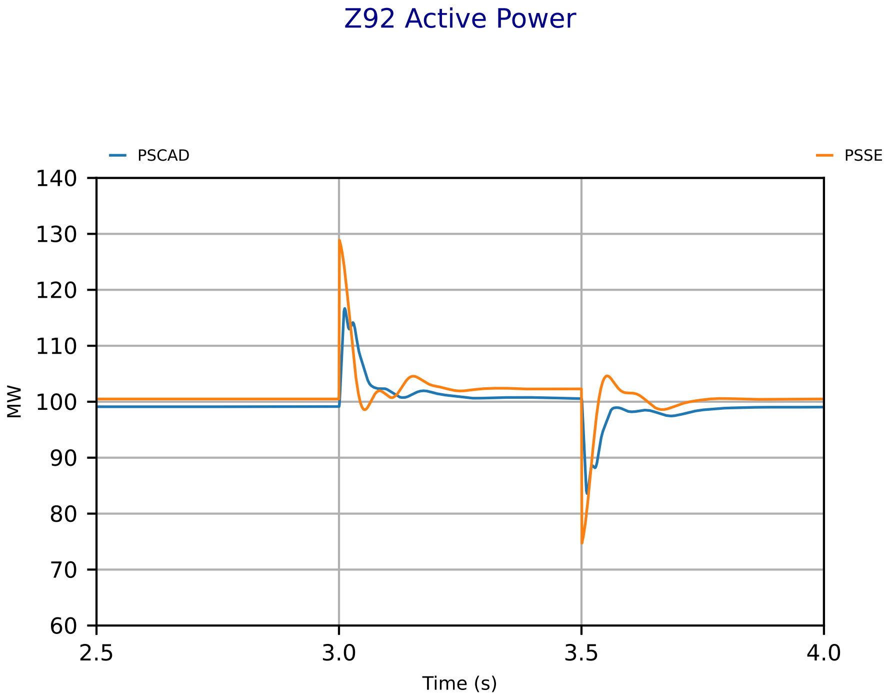
CMLD_SMIB_SCR_3_XR_3_T5_2

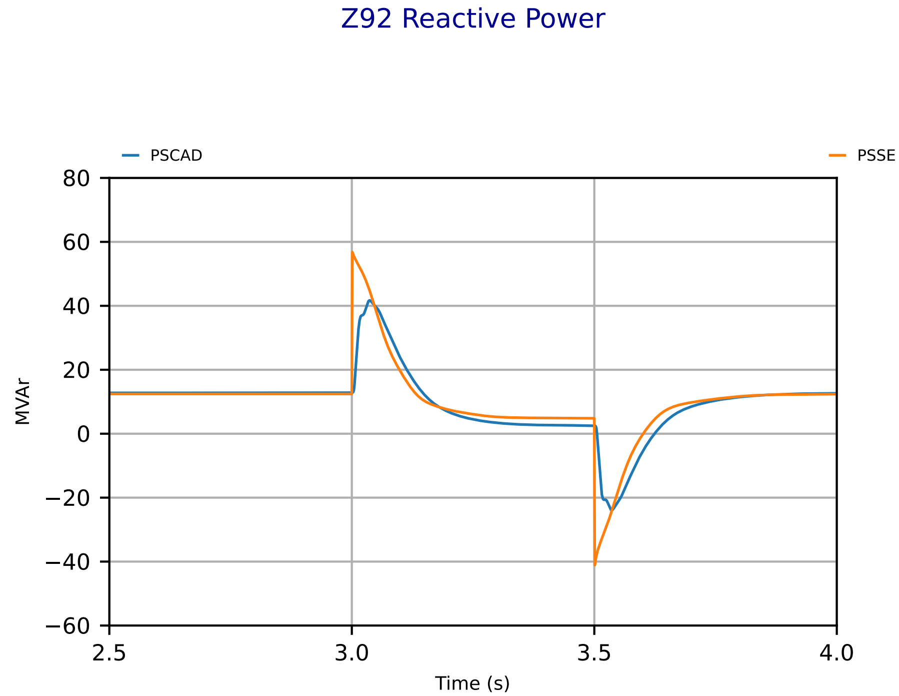


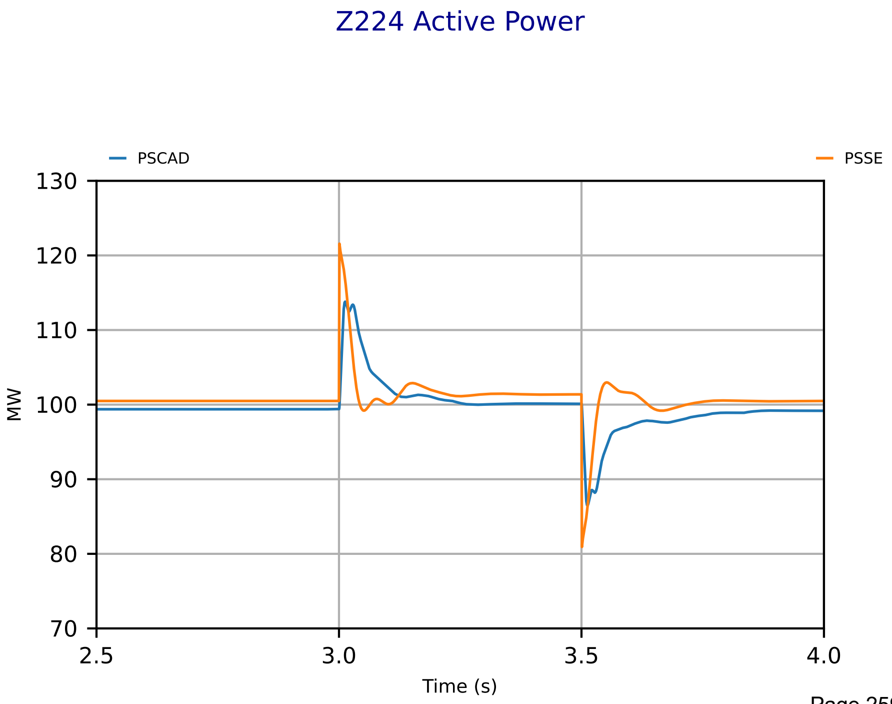
CMLD_SMIB_SCR_3_XR_3_T5_3

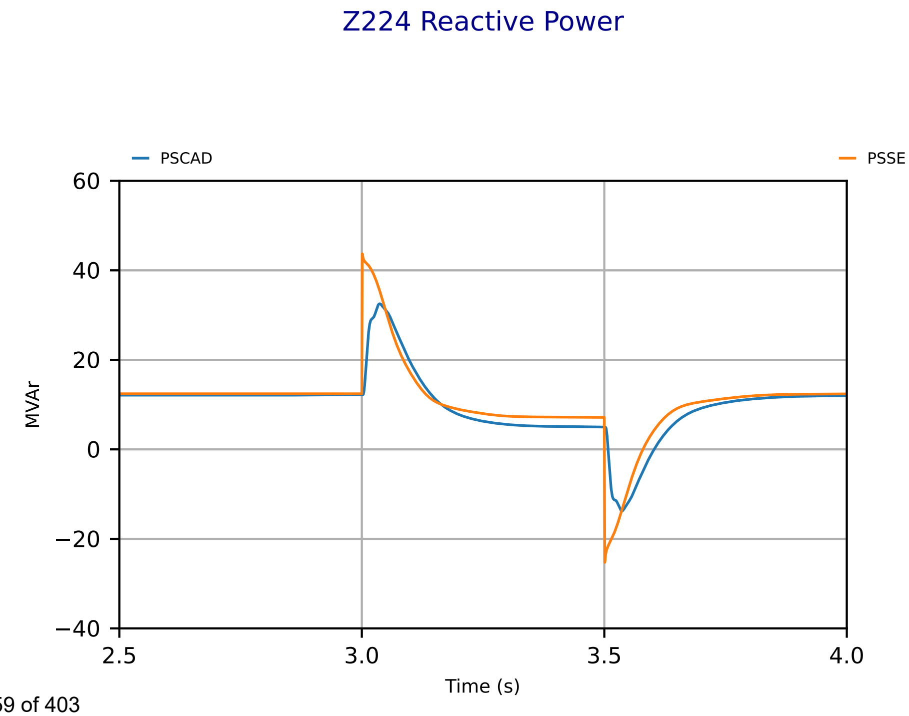


CMLD_SMIB_SCR_3_XR_3_T5_4









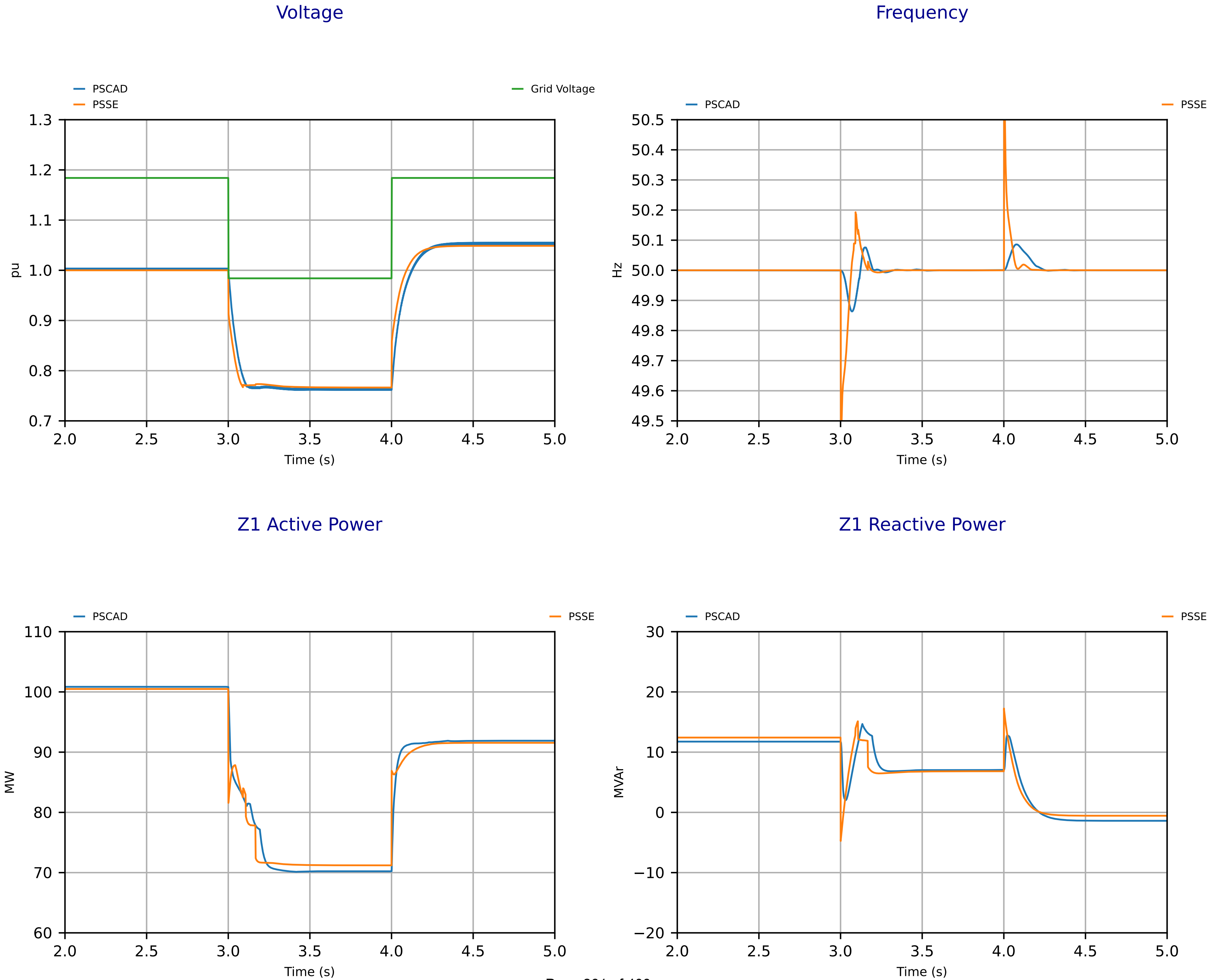
CMLD SMIB

SCR = 3, X/R = 3

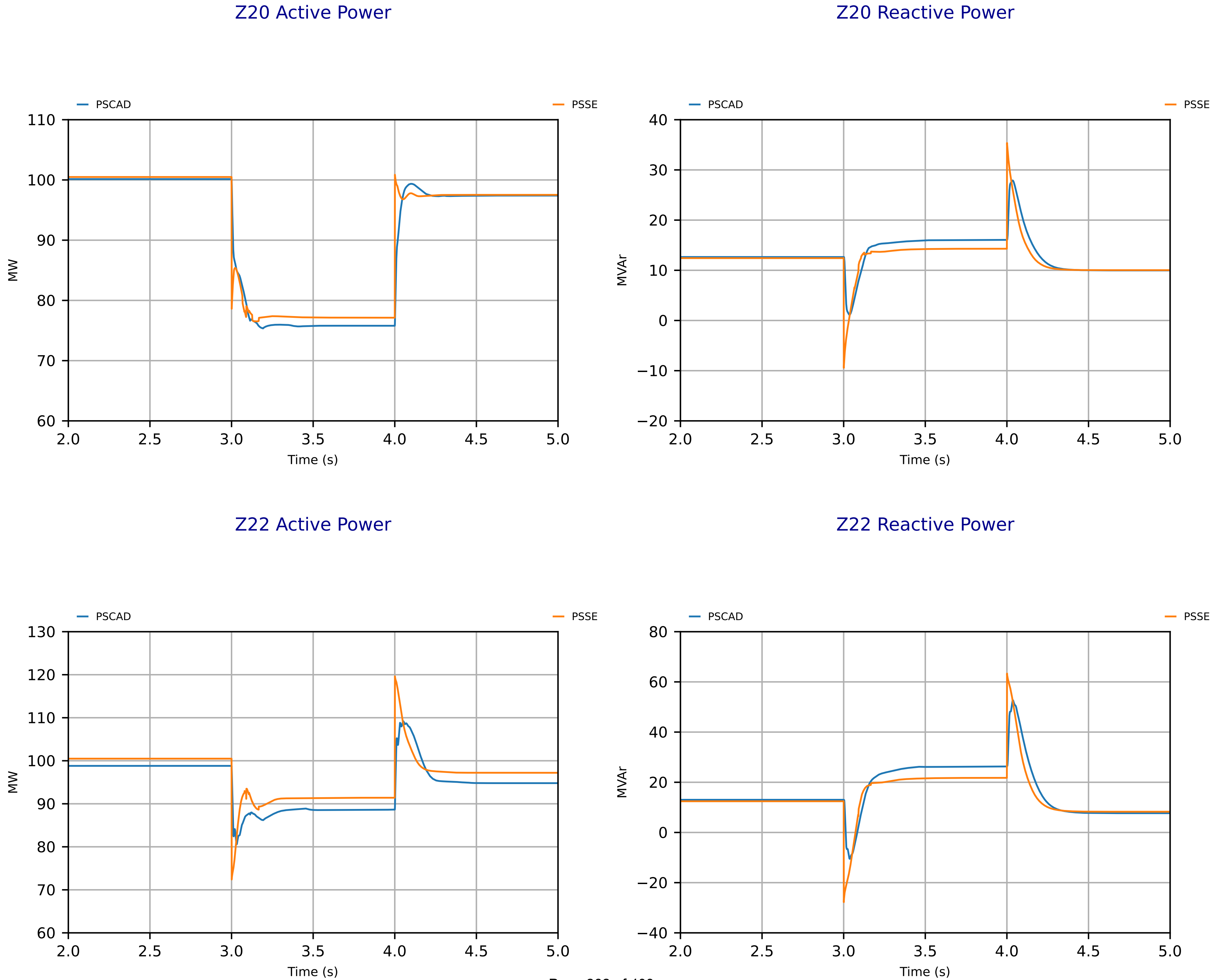
Test #6:

~80% Voltage disturbance for 1 sec

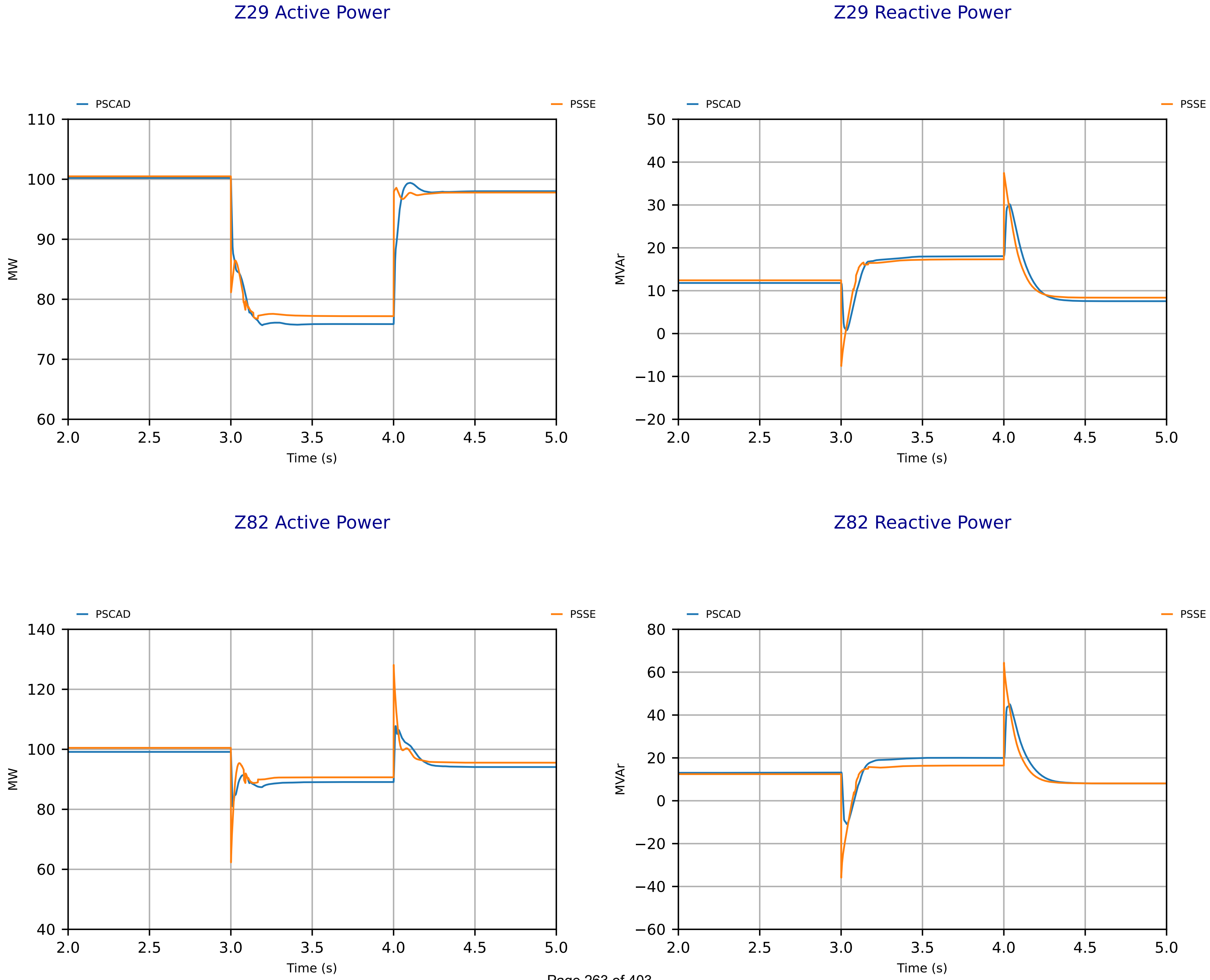
CMLD_SMIB_SCR_3_XR_3_T6_1



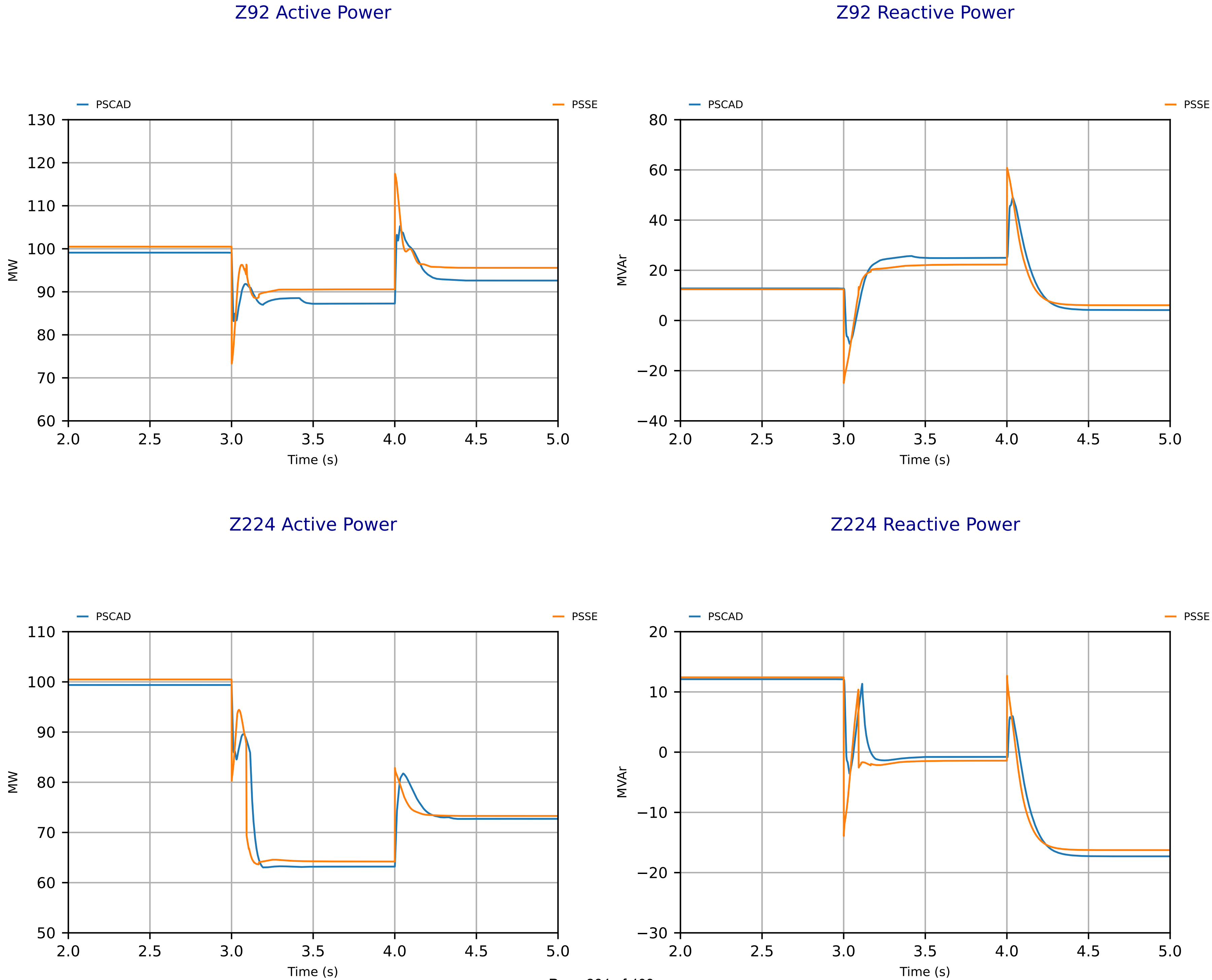
CMLD_SMIB_SCR_3_XR_3_T6_2



CMLD_SMIB_SCR_3_XR_3_T6_3



CMLD_SMIB_SCR_3_XR_3_T6_4



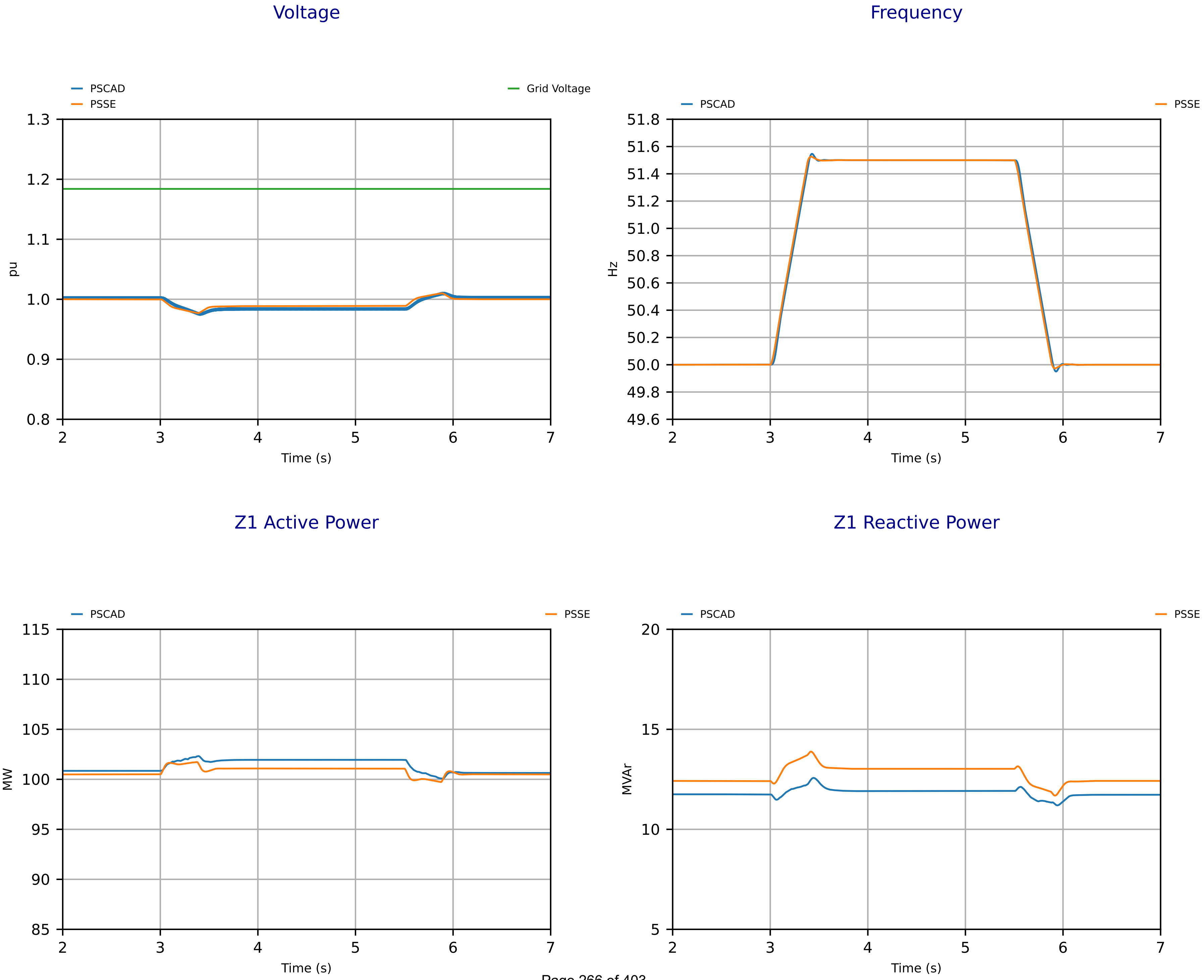
CMLD SMIB

SCR = 3, X/R = 3

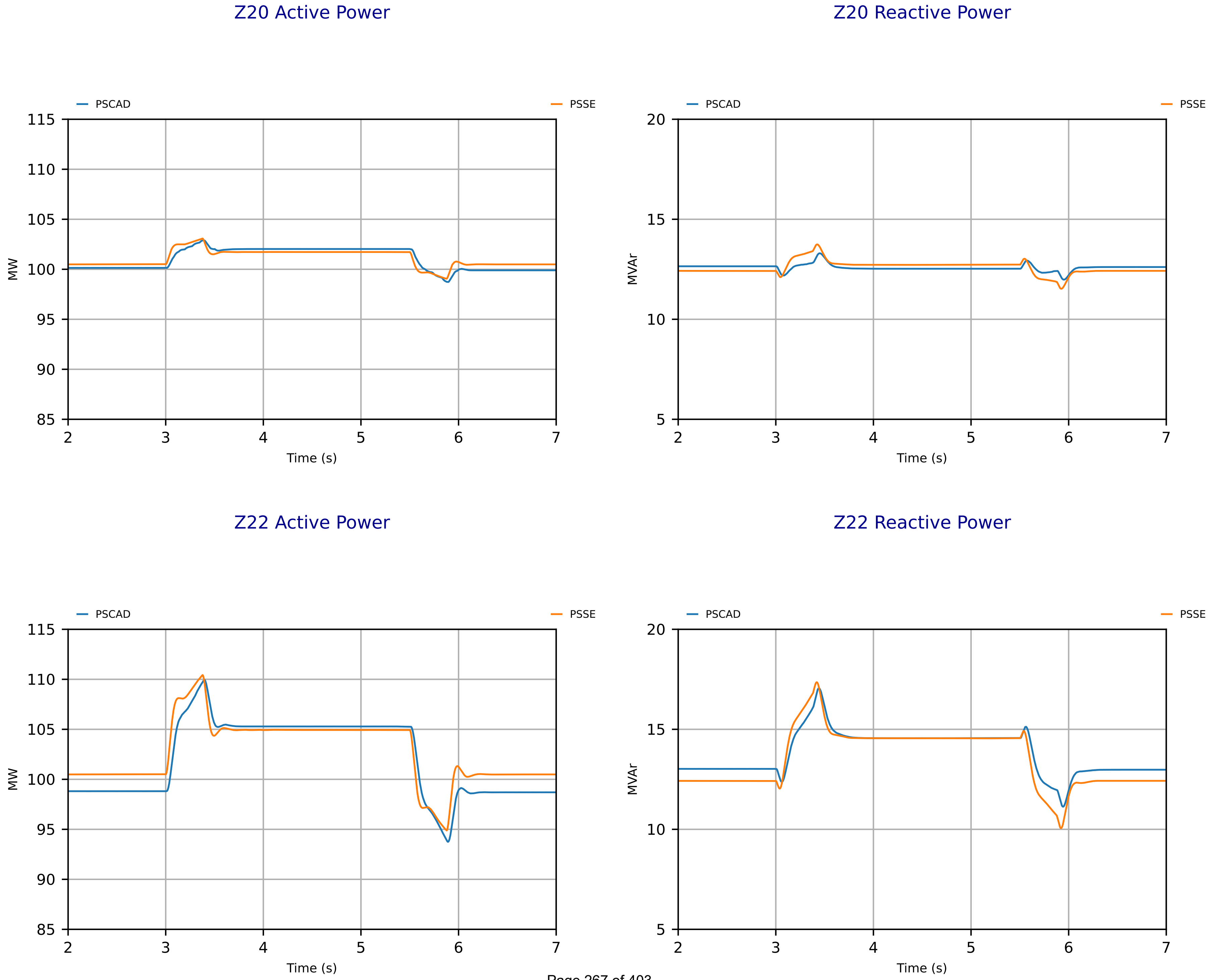
Test #7:

51.5 Hz frequency step for 2.5 sec (4 Hz/s)

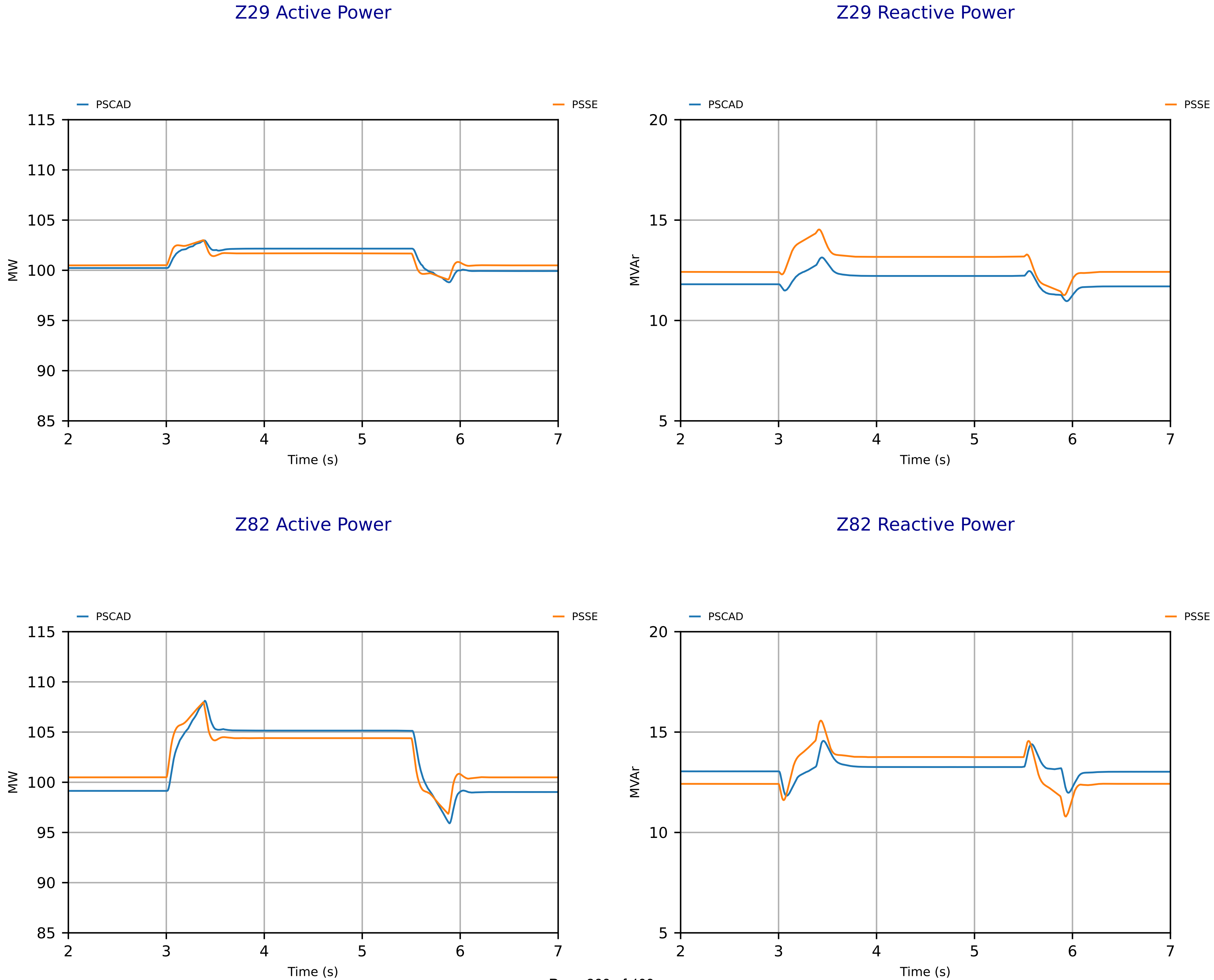
CMLD_SMIB_SCR_3_XR_3_T7_1



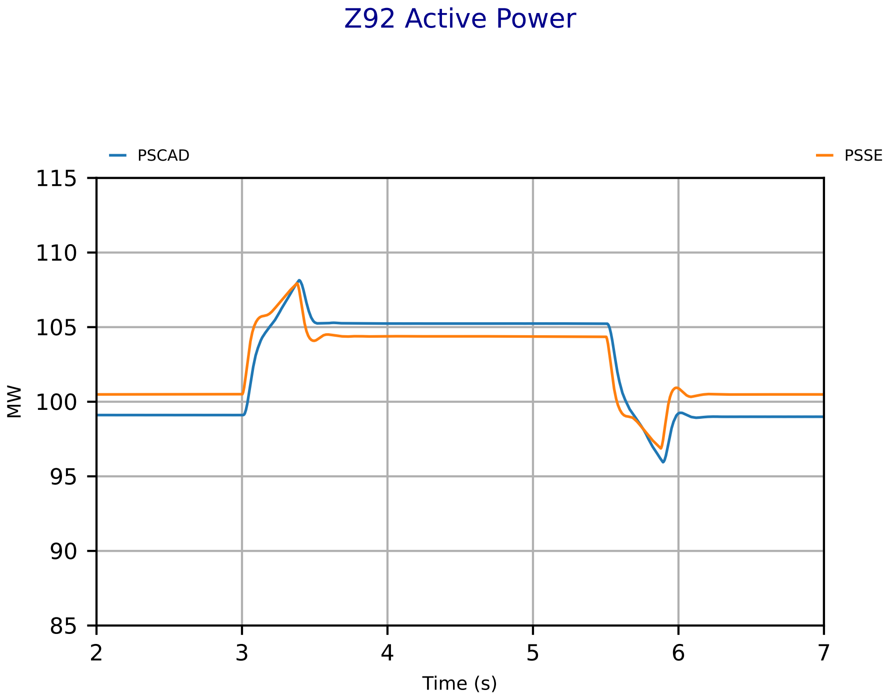
CMLD_SMIB_SCR_3_XR_3_T7_2

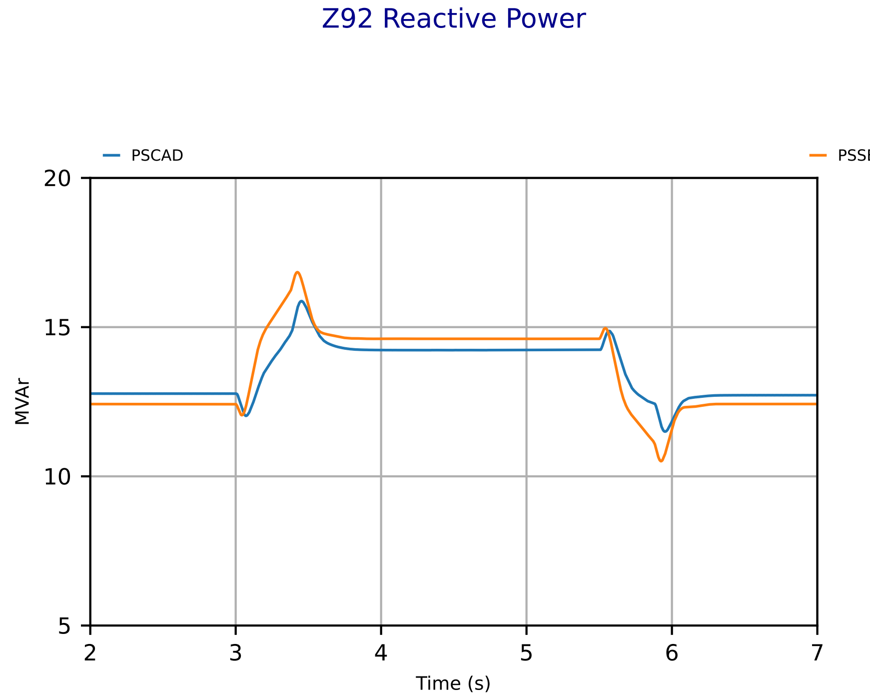


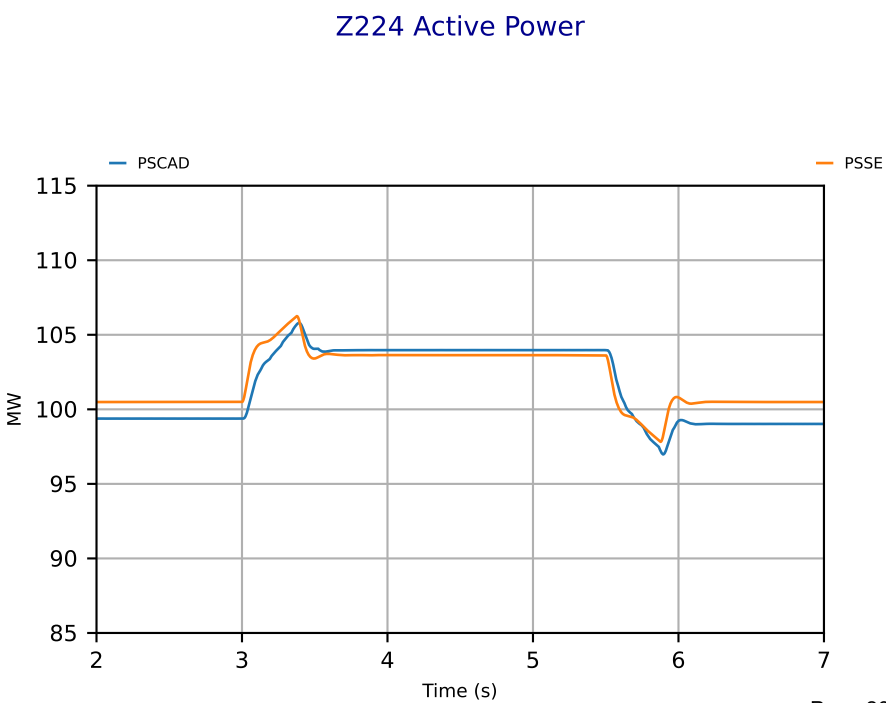
CMLD_SMIB_SCR_3_XR_3_T7_3

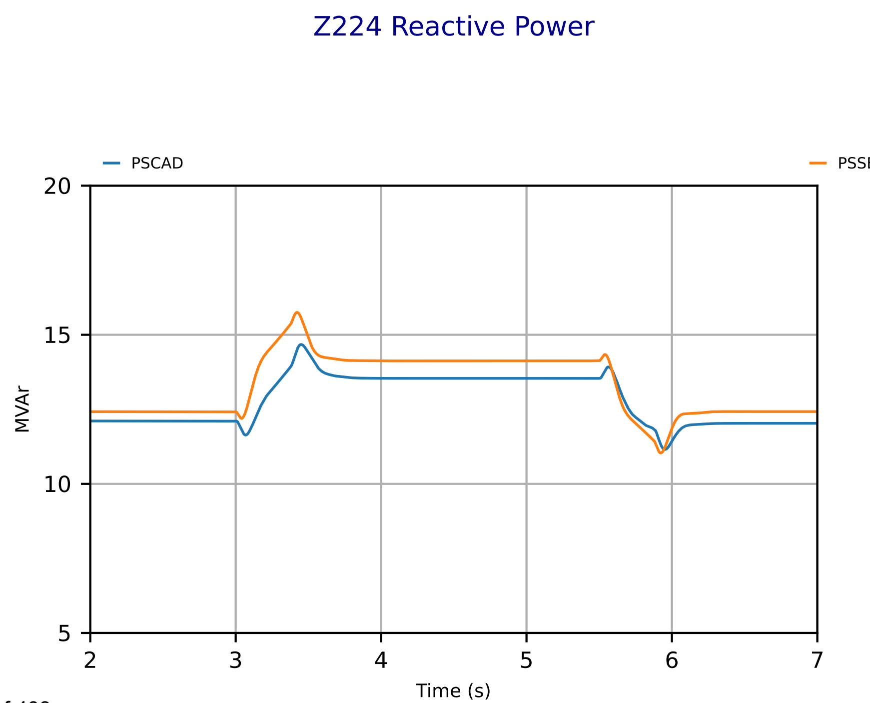


CMLD_SMIB_SCR_3_XR_3_T7_4









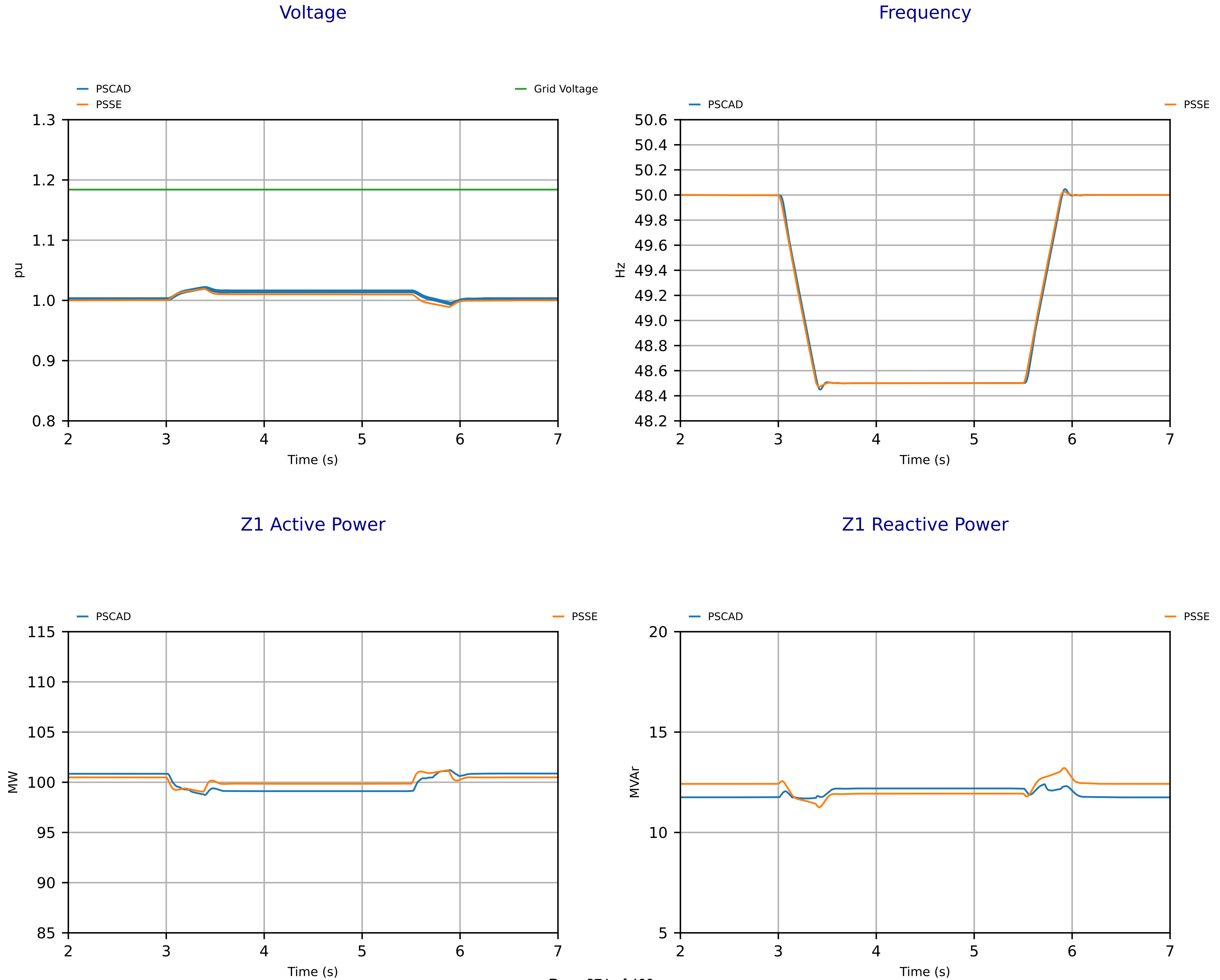
CMLD SMIB

SCR = 3, X/R = 3

Test #8:

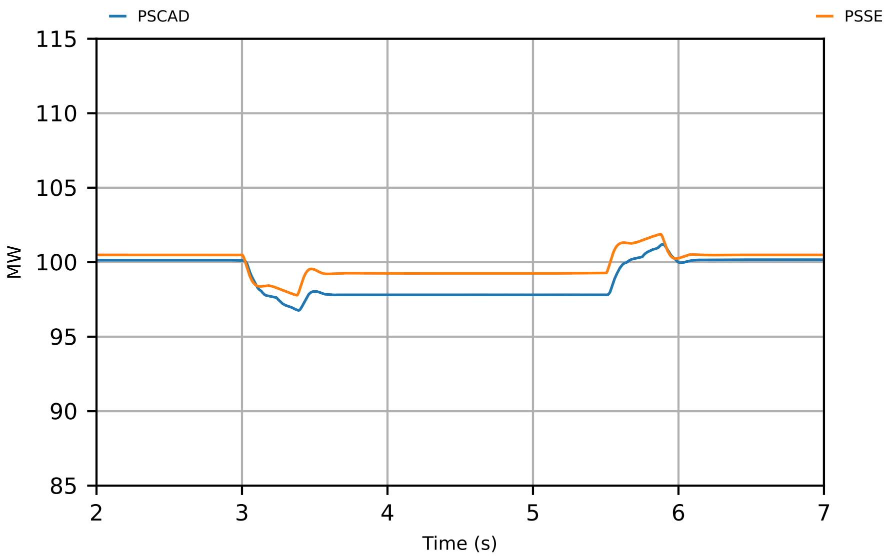
48.5 Hz frequency step for 2.5 sec (4 Hz/s)

CMLD_SMIB_SCR_3_XR_3_T8_1

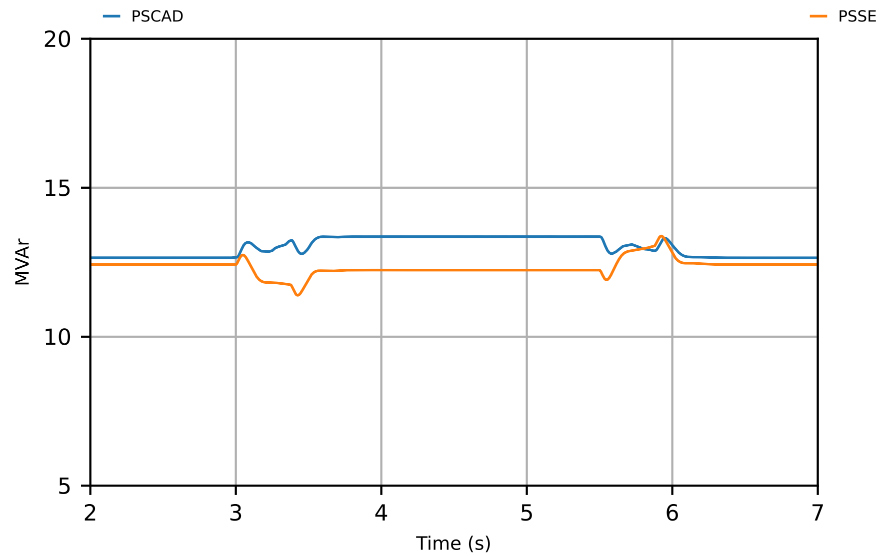


CMLD_SMIB_SCR_3_XR_3_T8_2

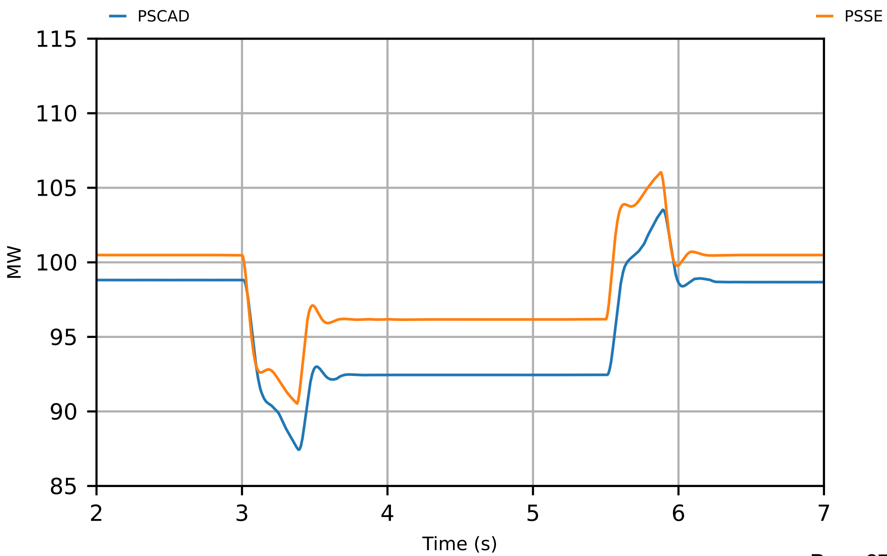
Z20 Active Power



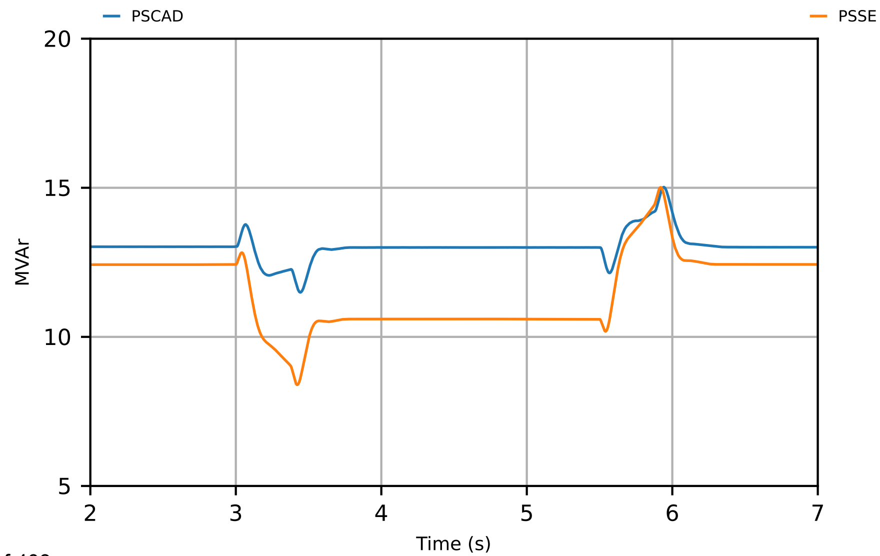
Z20 Reactive Power



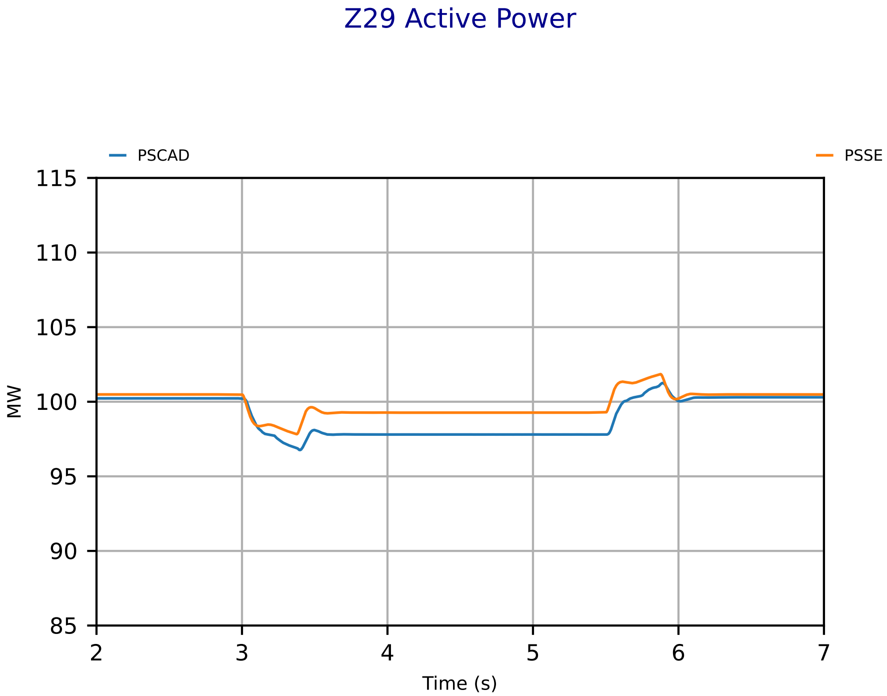
Z22 Active Power

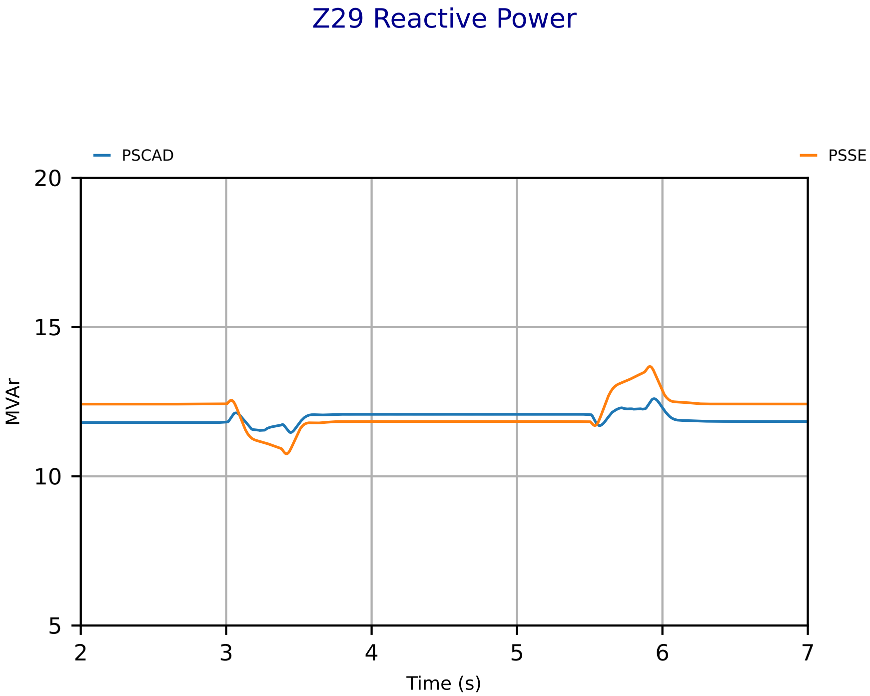


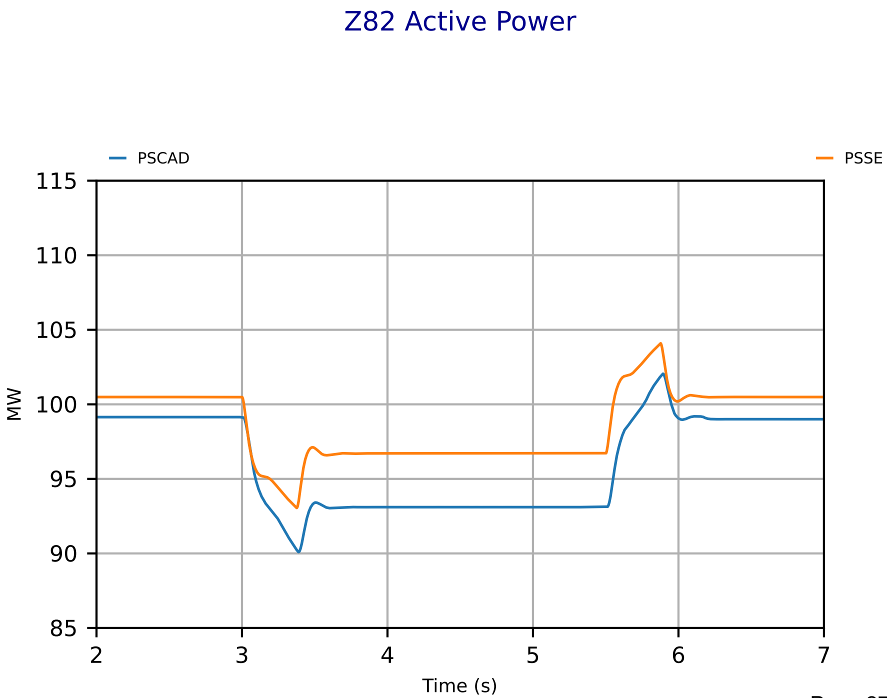
Z22 Reactive Power

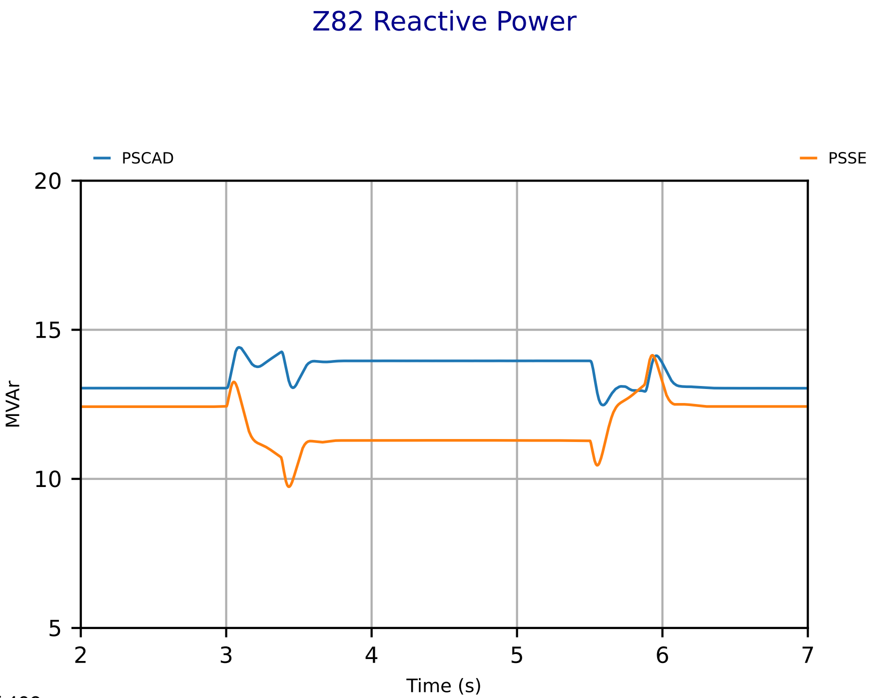


CMLD_SMIB_SCR_3_XR_3_T8_3

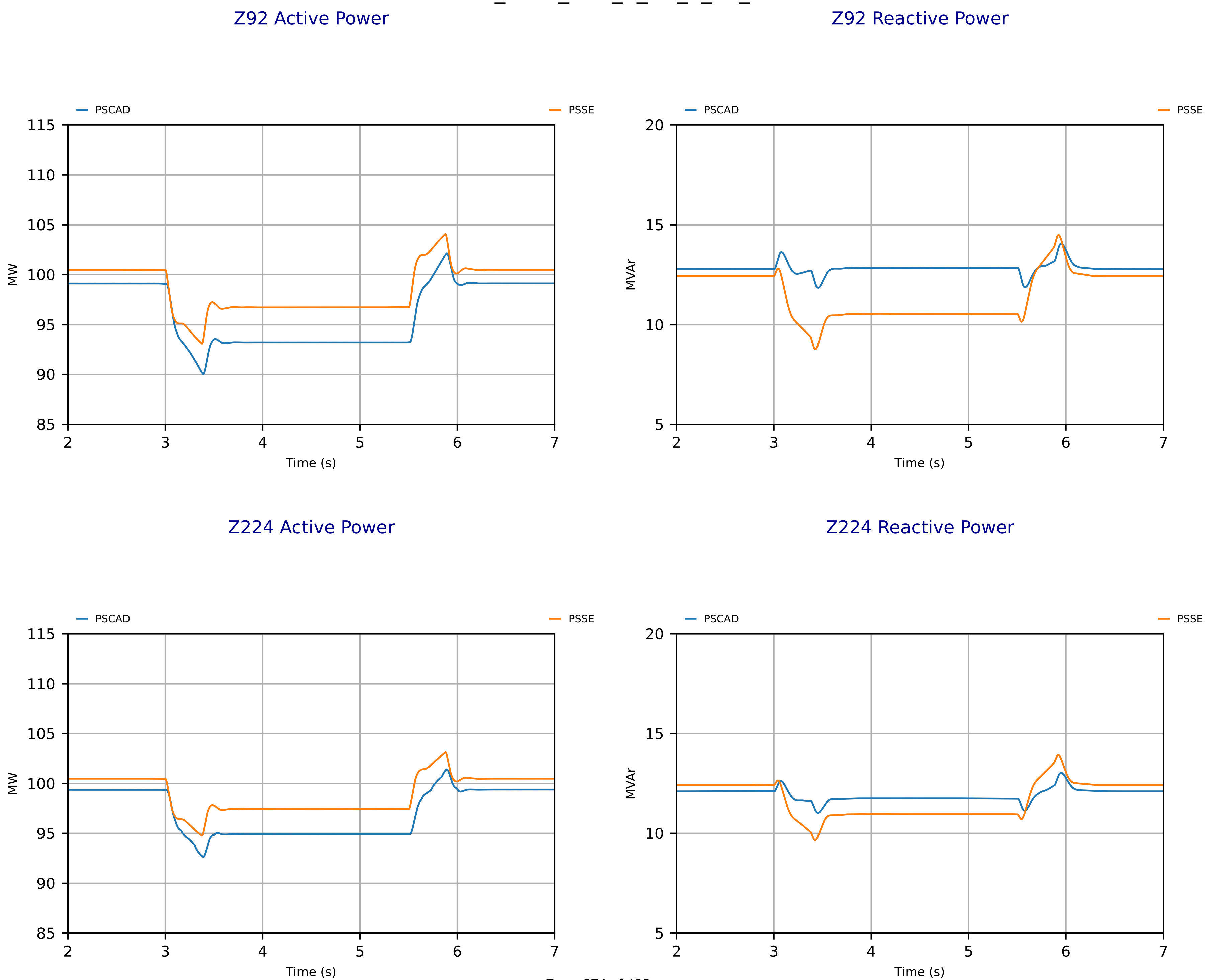








CMLD_SMIB_SCR_3_XR_3_T8_4

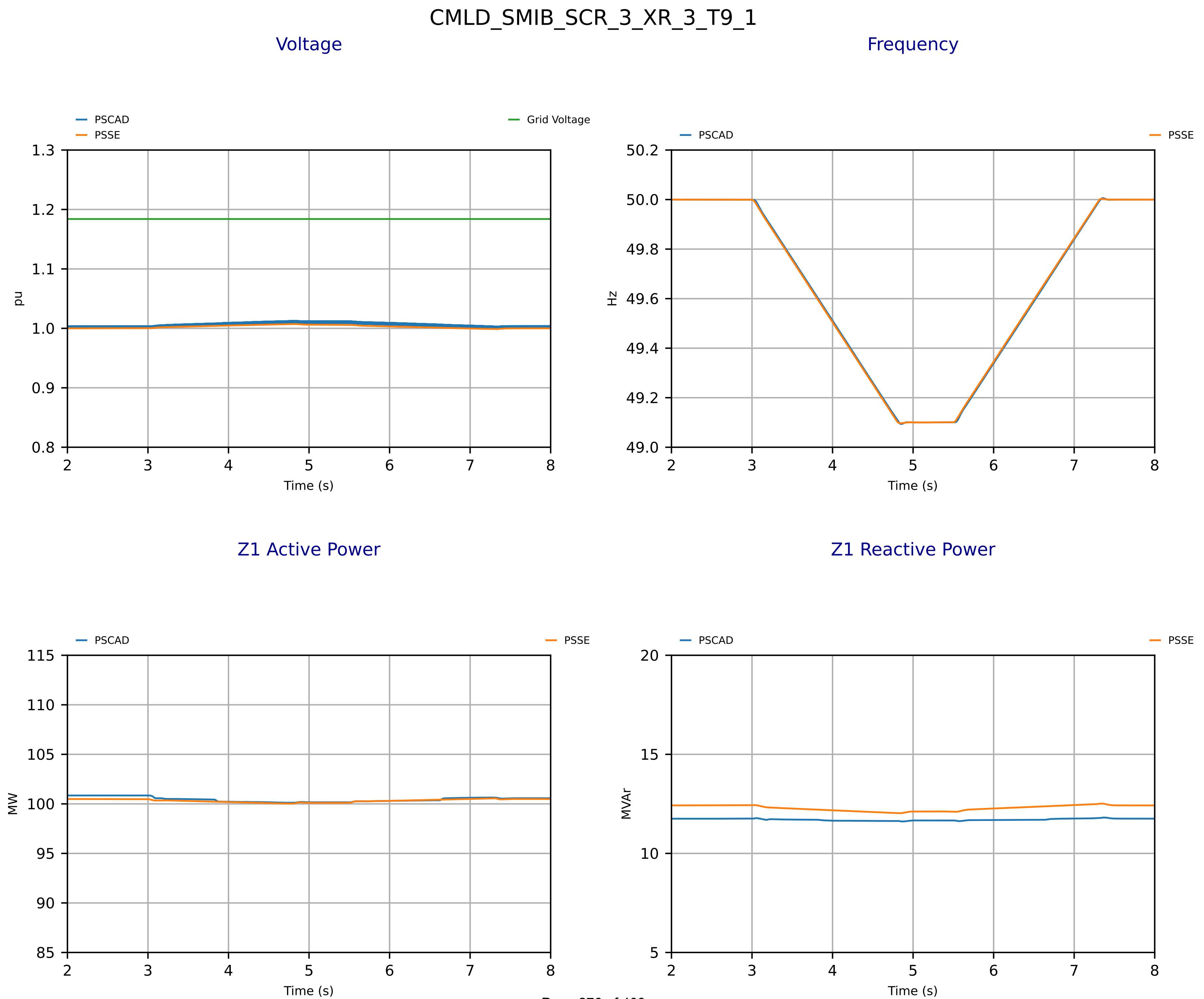


CMLD SMIB

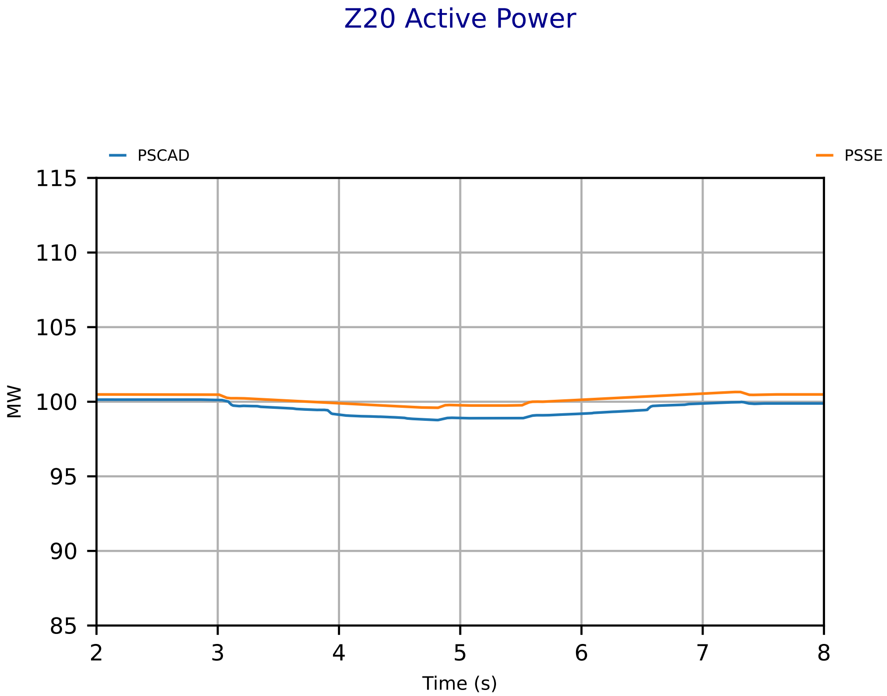
SCR = 3, X/R = 3

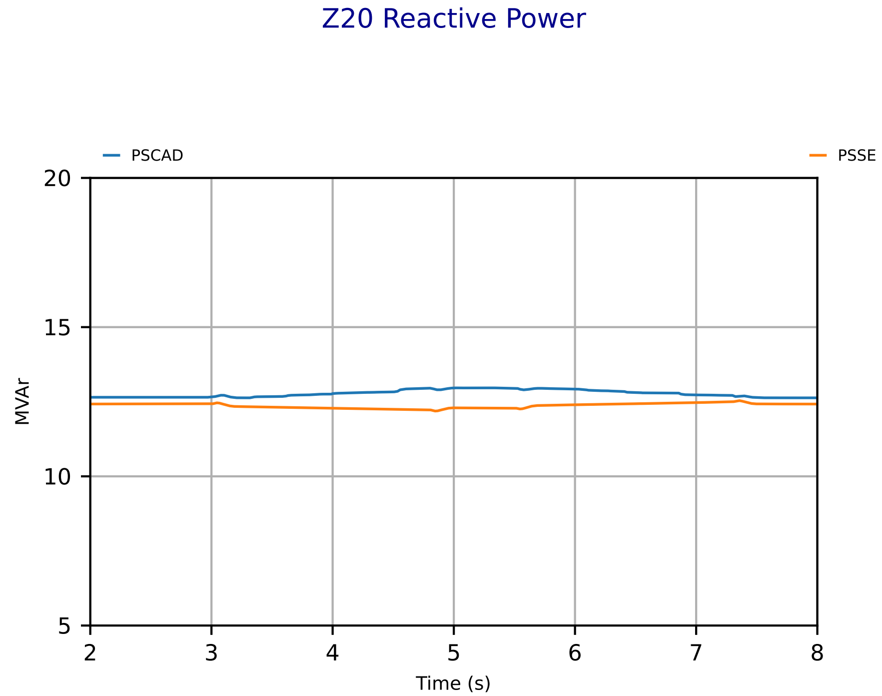
Test #9:

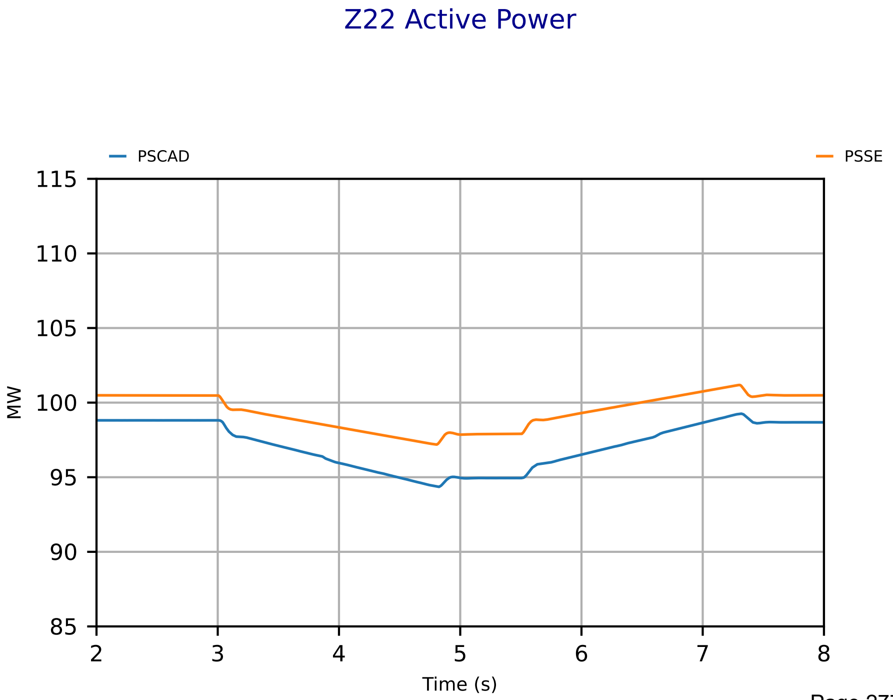
49.1 Hz slow frequency ramp (0.5 Hz/s)

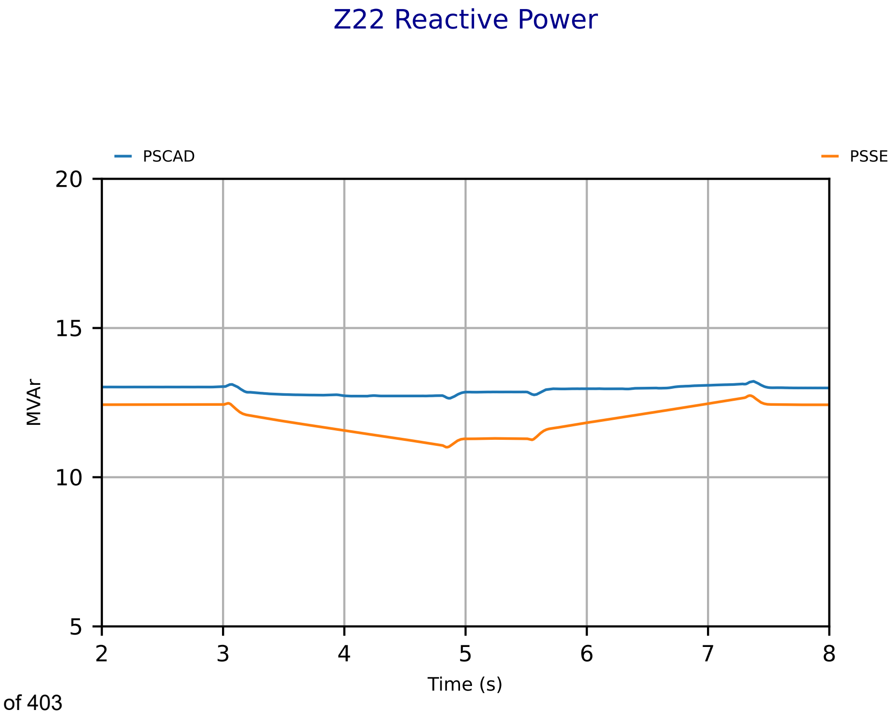

CMLD_SMIB_SCR_3_XR_3_T9_1
Voltage
PSCAD
PSSE
Grid Voltage
pu
Time (s)
Frequency
Hz
Z1 Active Power
MW
Z1 Reactive Power
MVAr

CMLD_SMIB_SCR_3_XR_3_T9_2

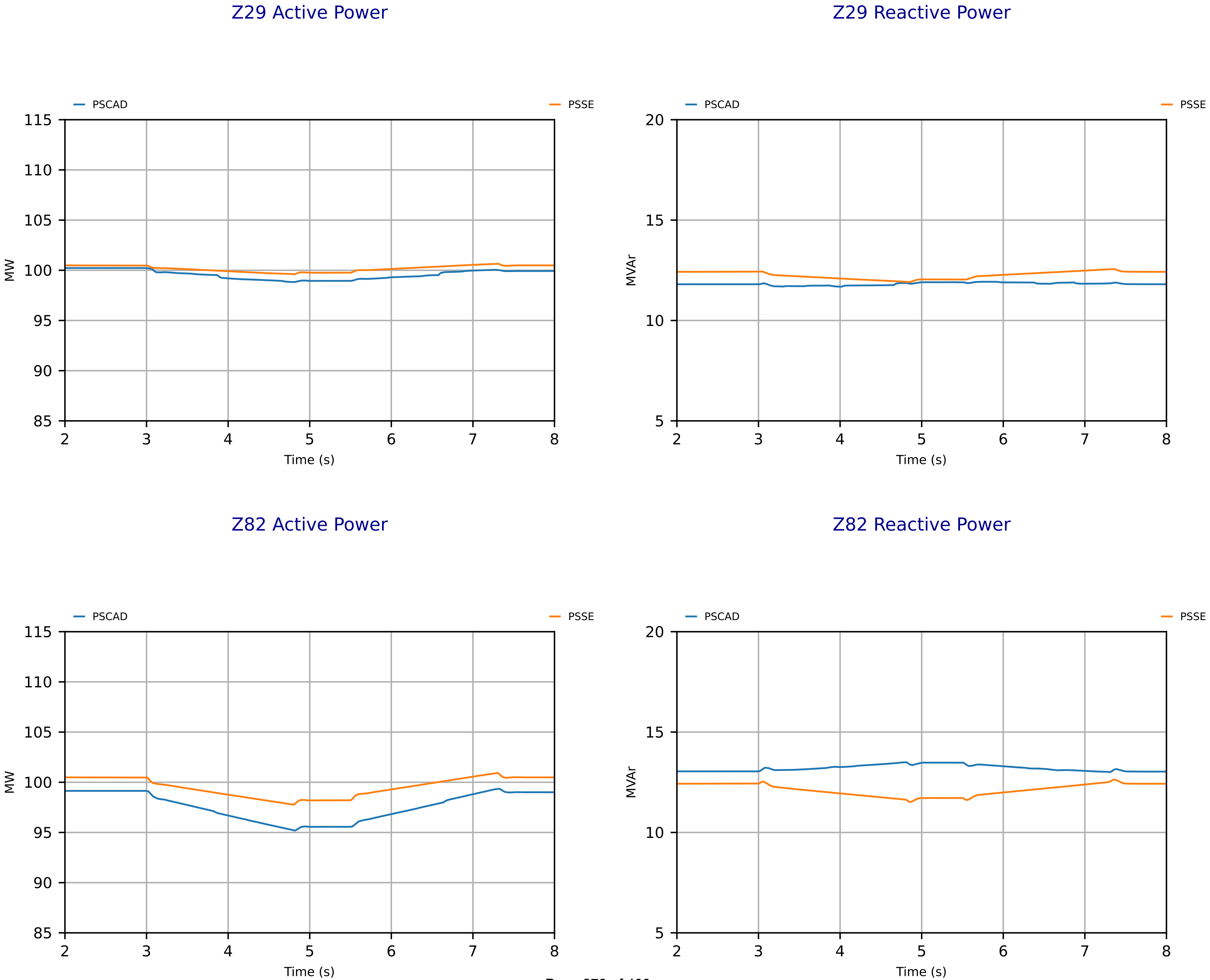




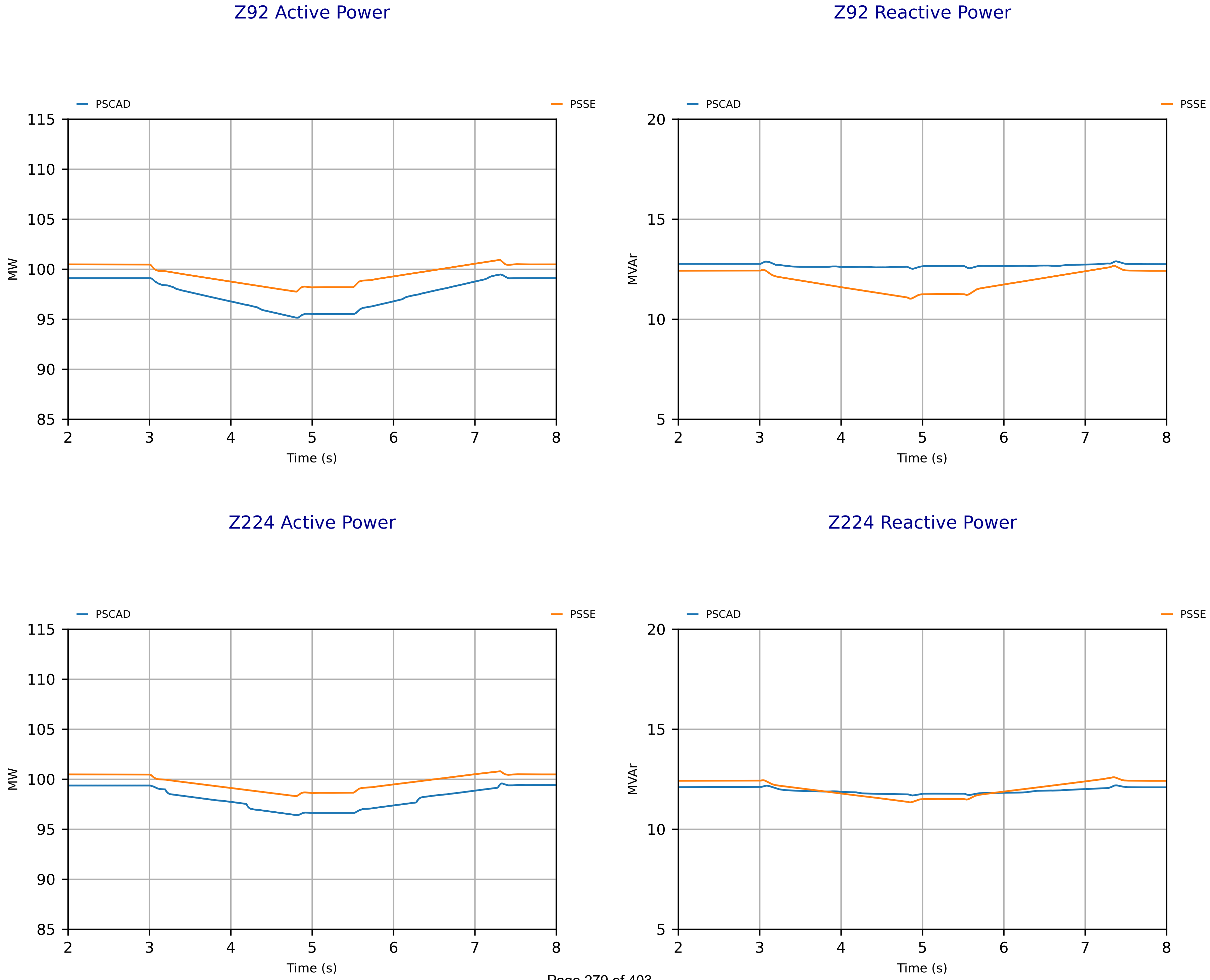




CMLD_SMIB_SCR_3_XR_3_T9_3



CMLD_SMIB_SCR_3_XR_3_T9_4



CMLD SMIB

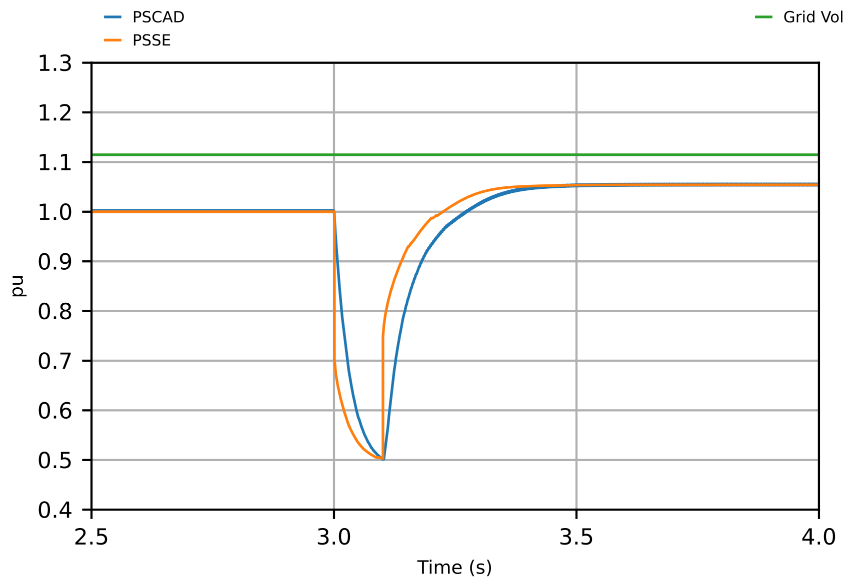
SCR = 3, X/R = 14

Test #2:

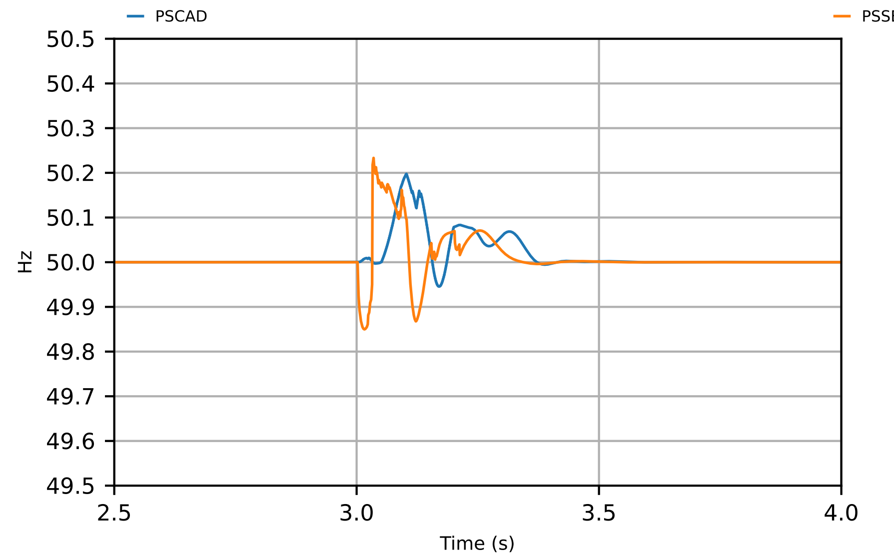
LLG fault for 100 ms

CMLD_SMIB_SCR_3_XR_14_T2_1

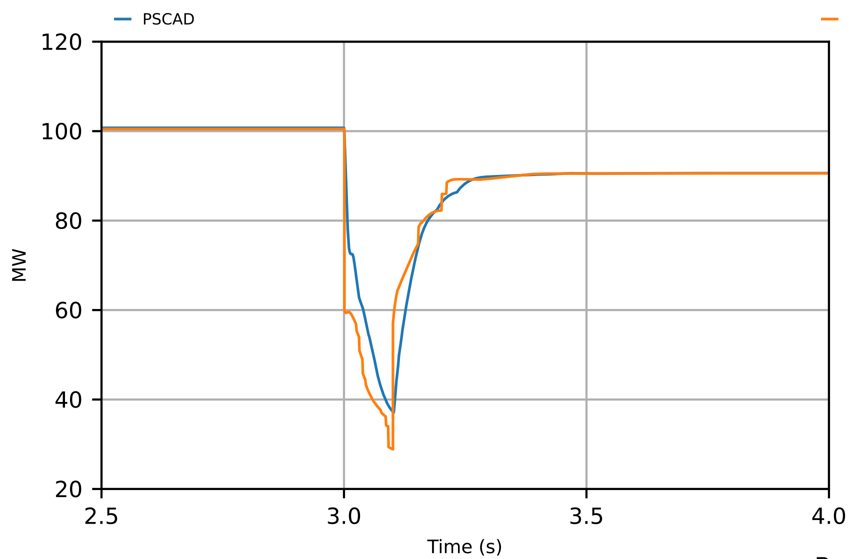
Voltage



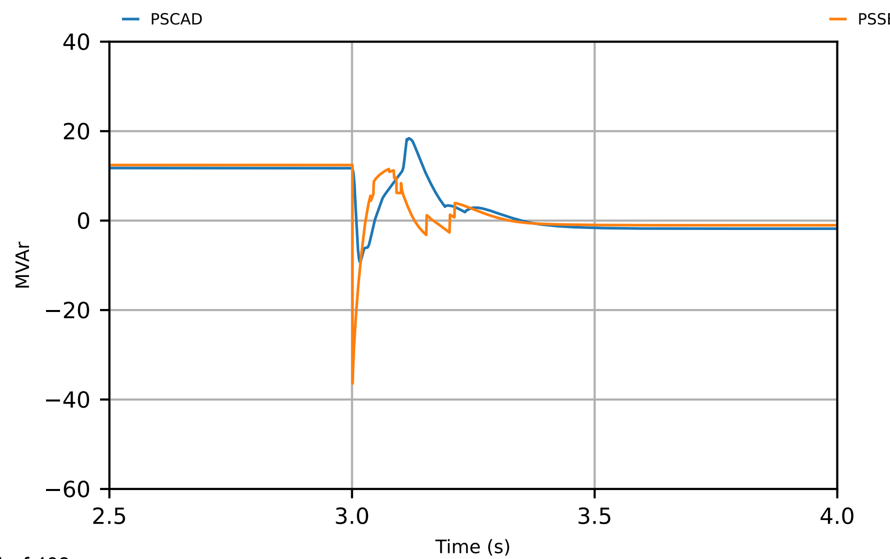
Frequency



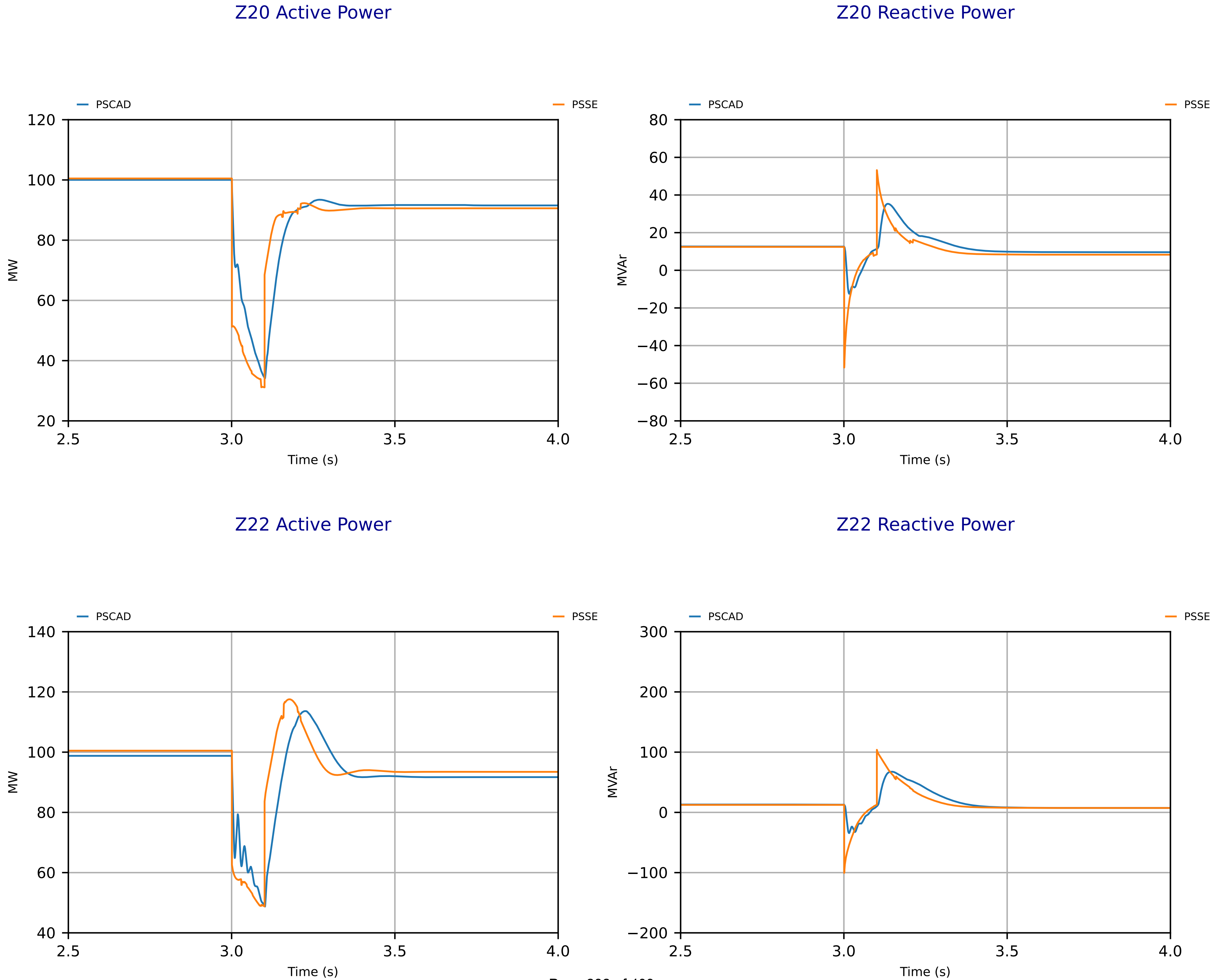
Z1 Active Power



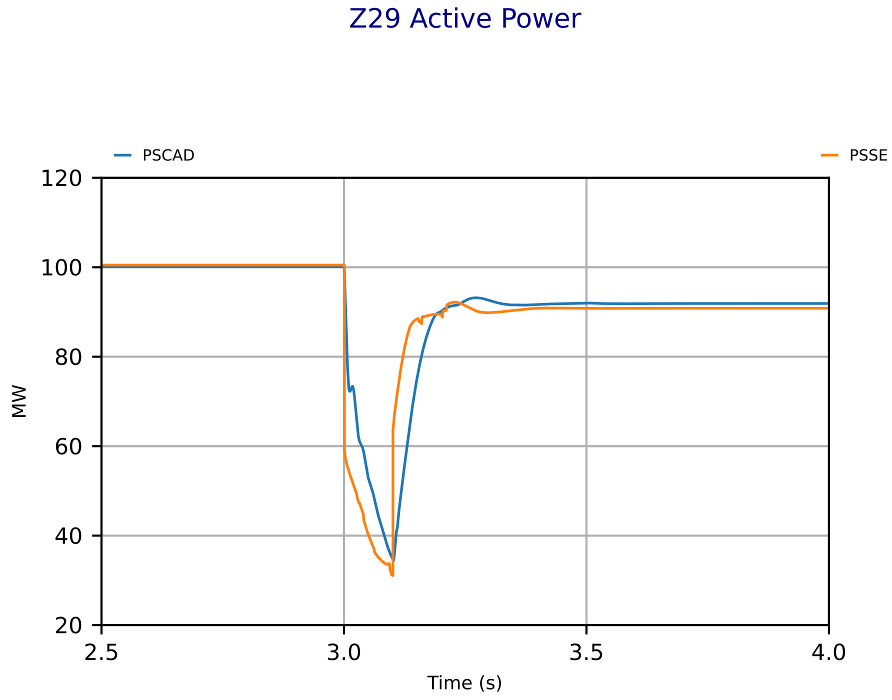
Z1 Reactive Power

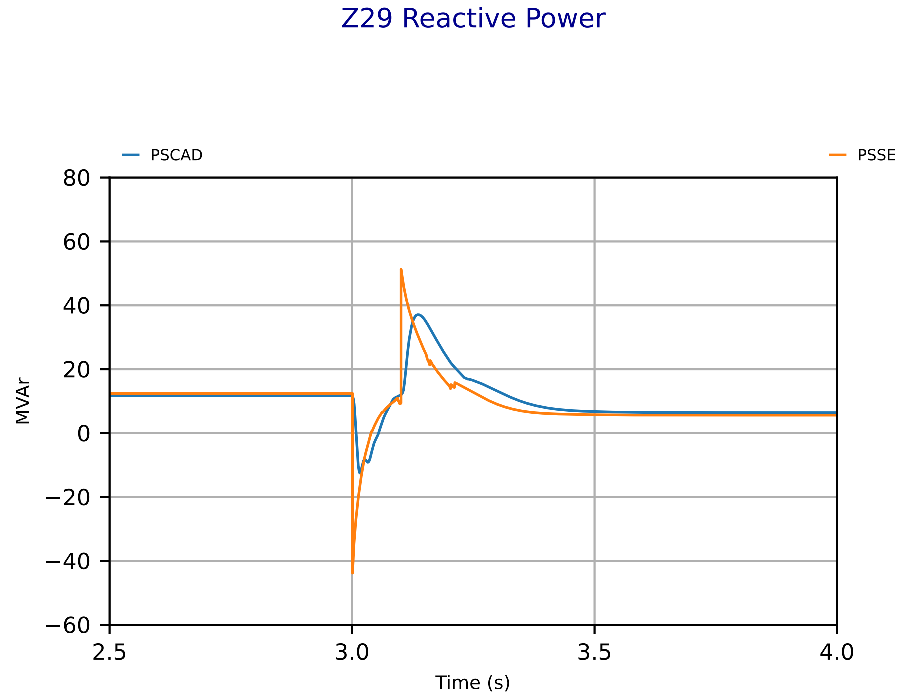


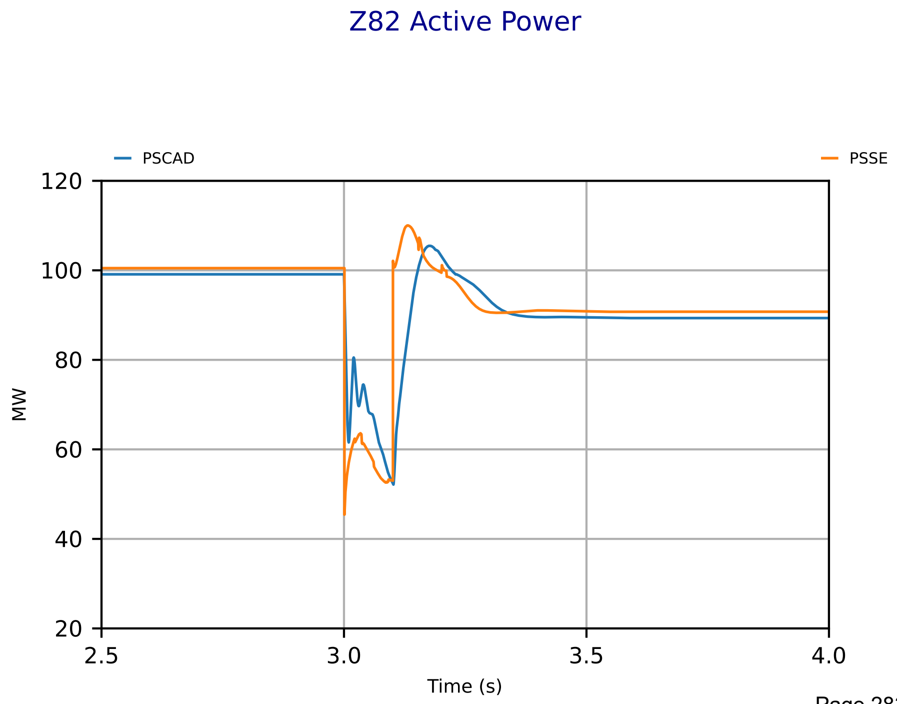
CMLD_SMIB_SCR_3_XR_14_T2_2

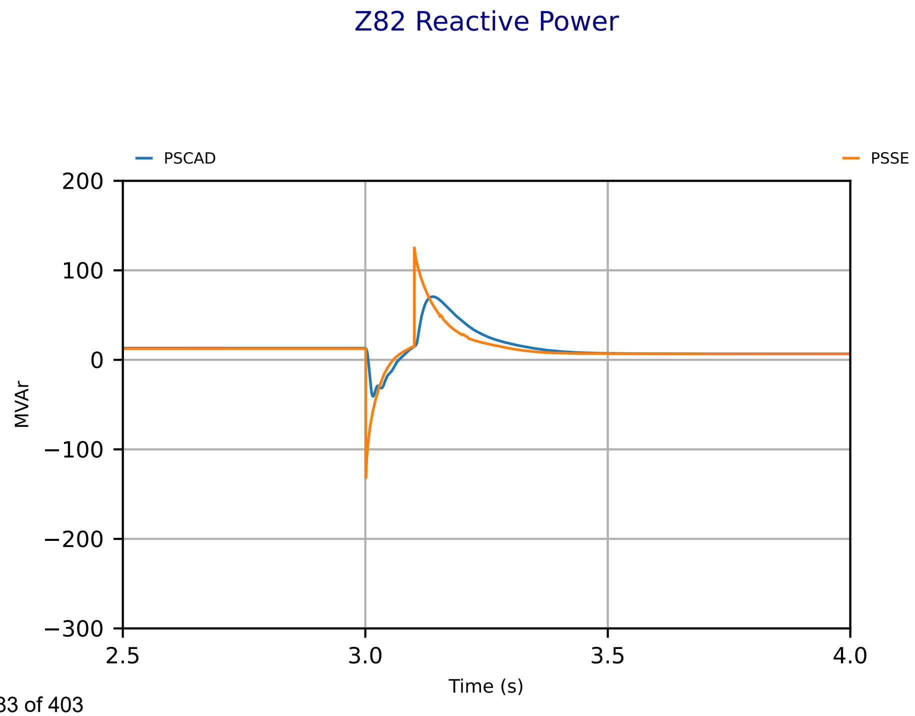


CMLD_SMIB_SCR_3_XR_14_T2_3

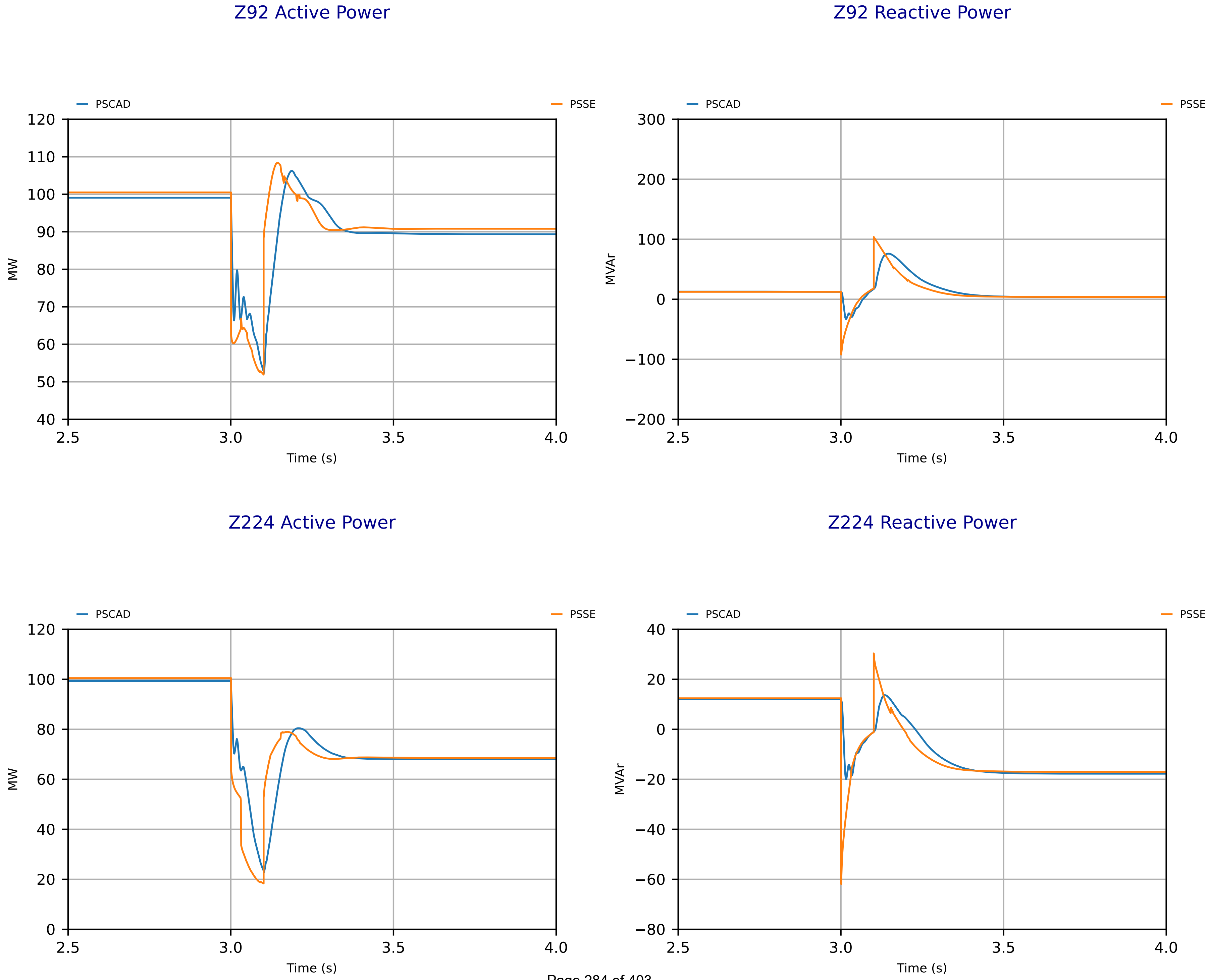








CMLD_SMIB_SCR_3_XR_14_T2_4



CMLD SMIB

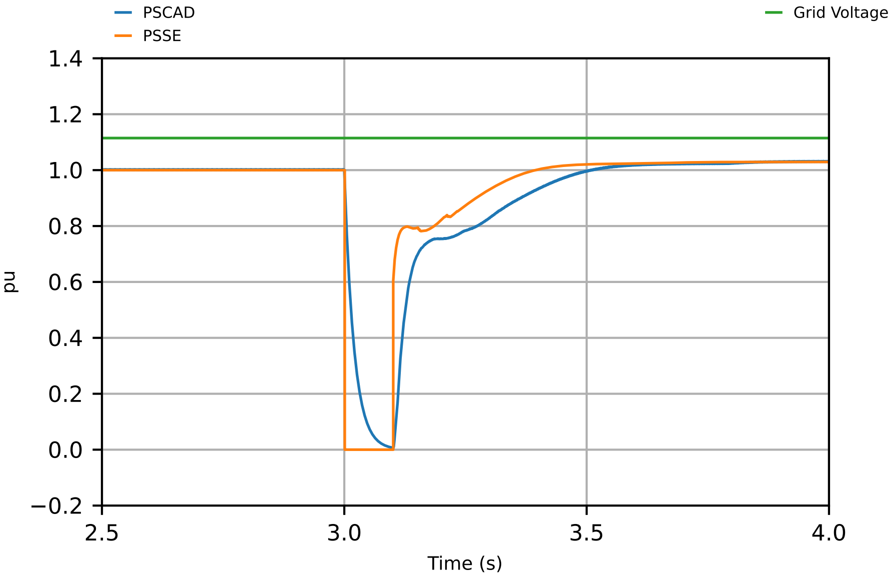
SCR = 3, X/R = 14

Test #3:

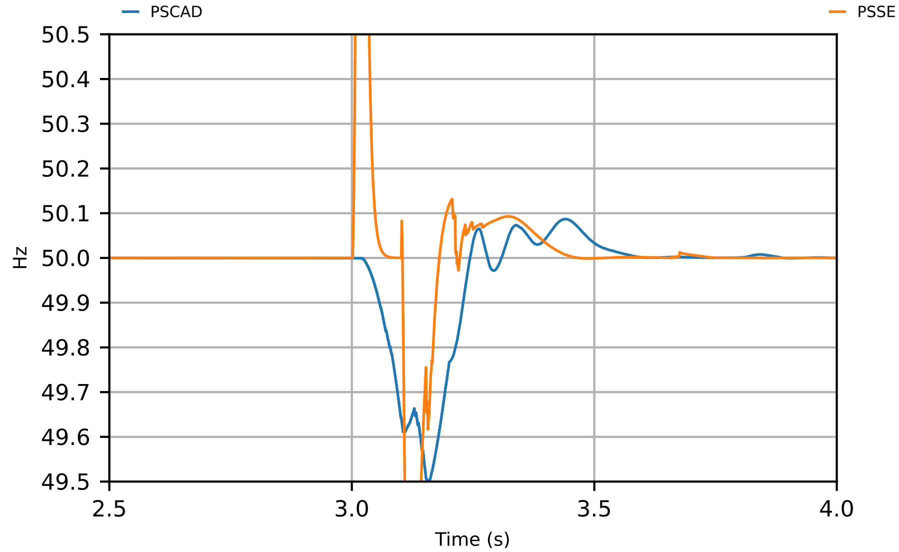
3PH-G fault for 100 ms

CMLD_SMIB_SCR_3_XR_14_T3_1

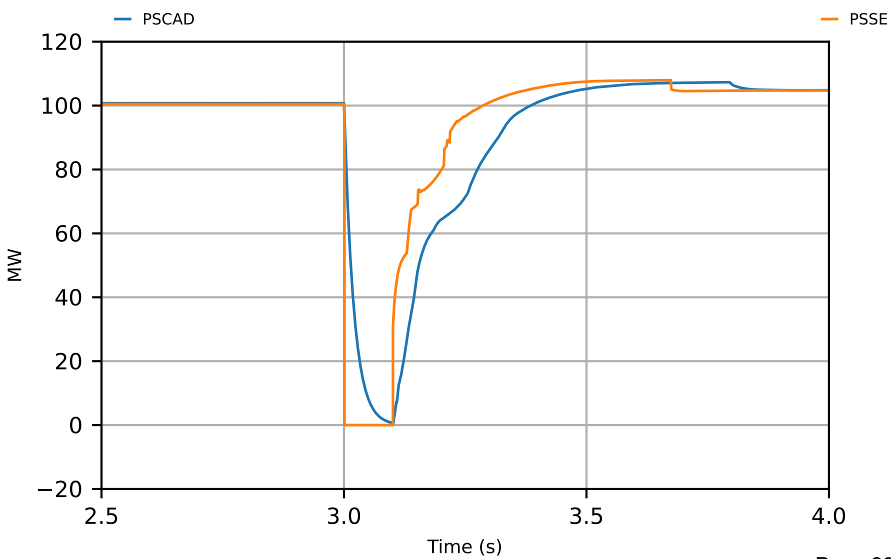
Voltage



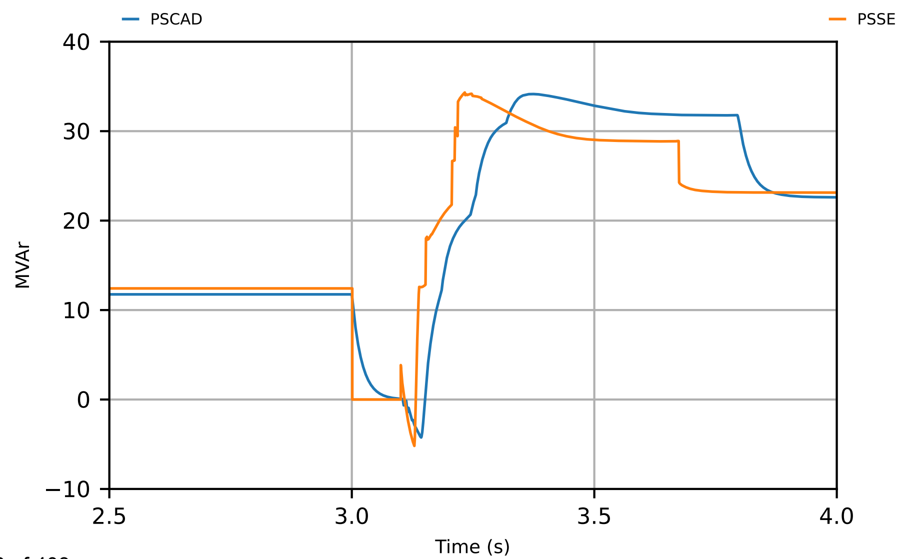
Frequency



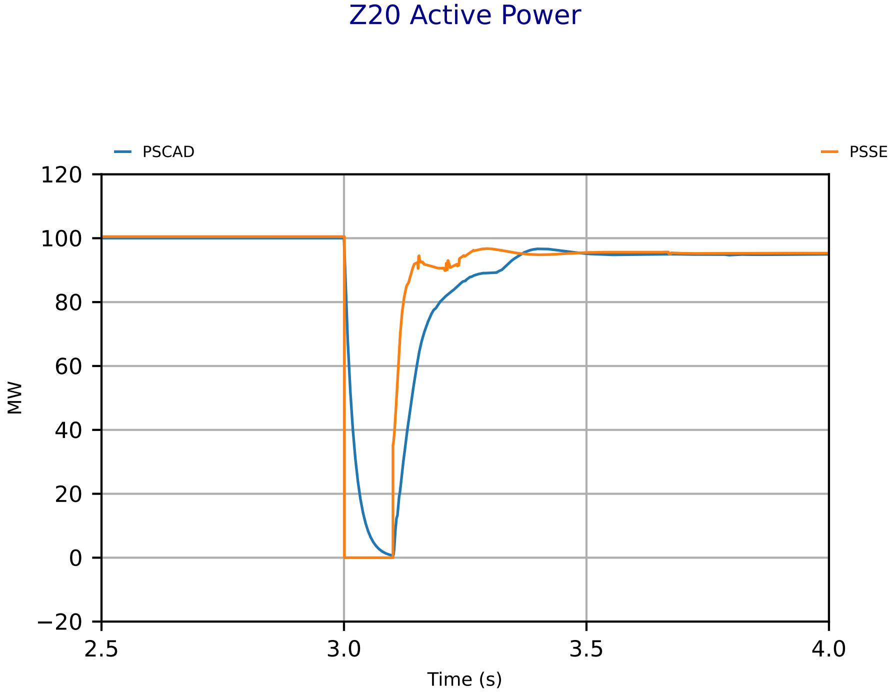
Z1 Active Power

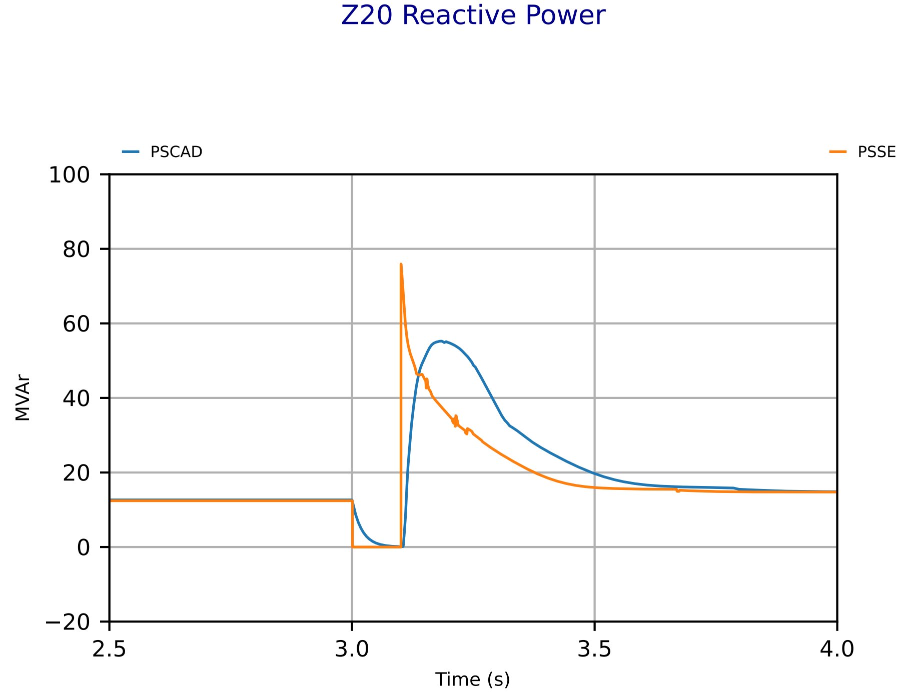


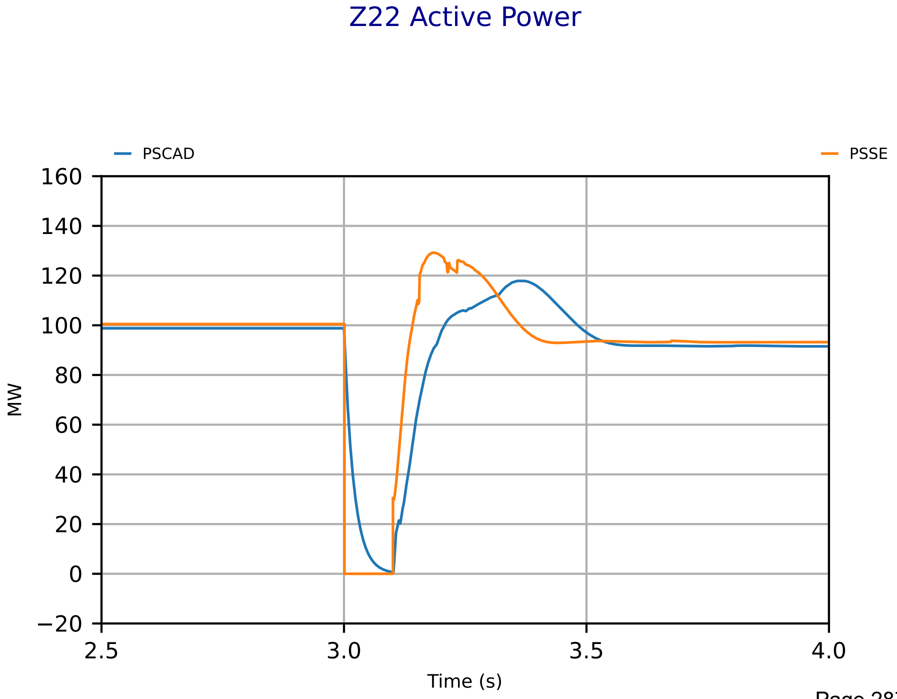
Z1 Reactive Power

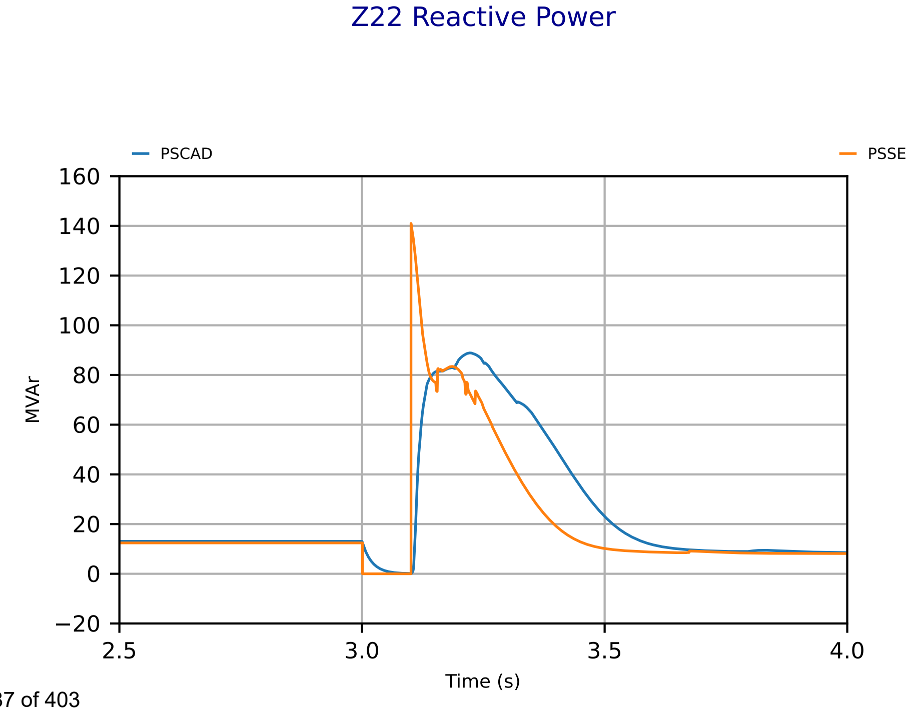


CMLD_SMIB_SCR_3_XR_14_T3_2

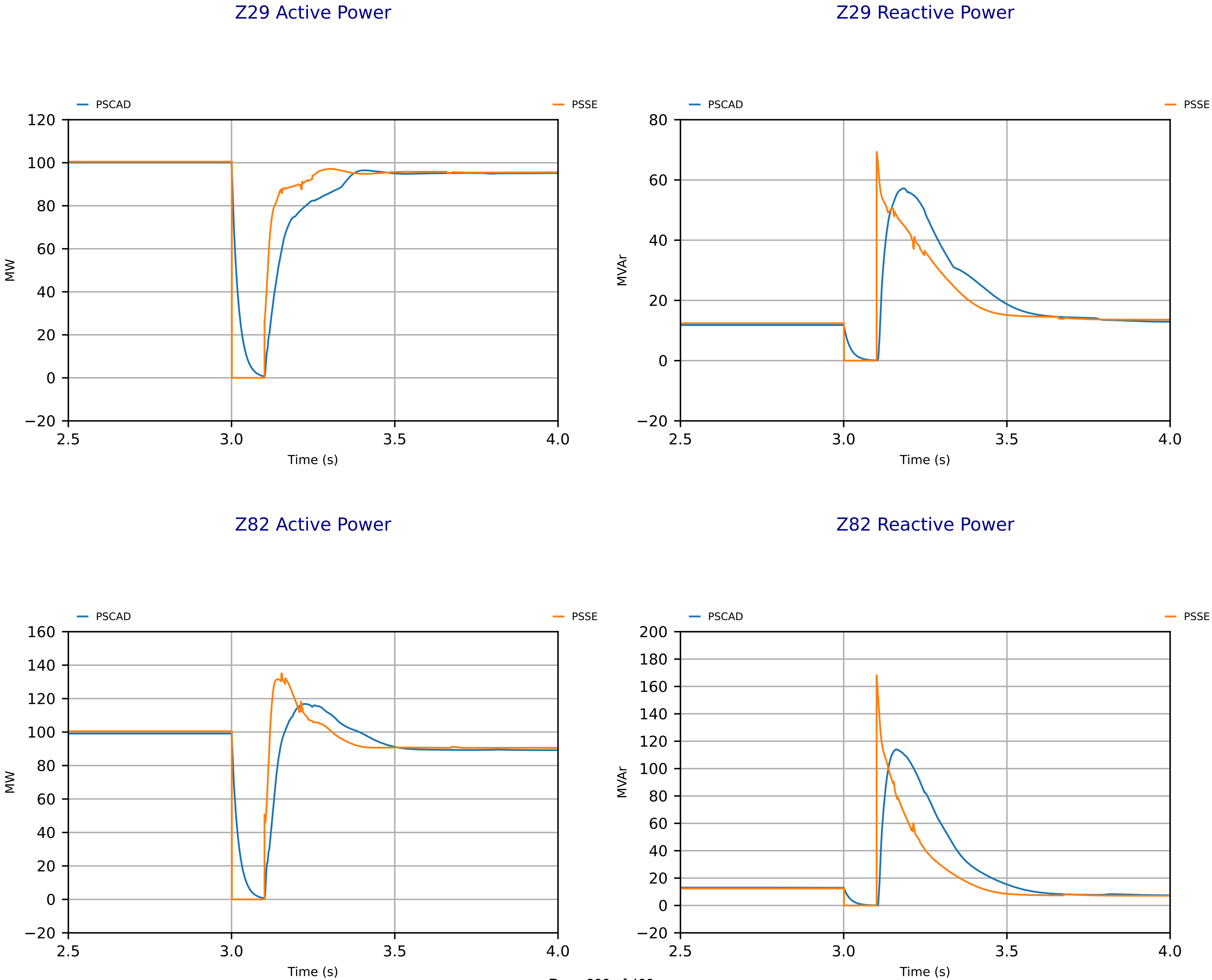




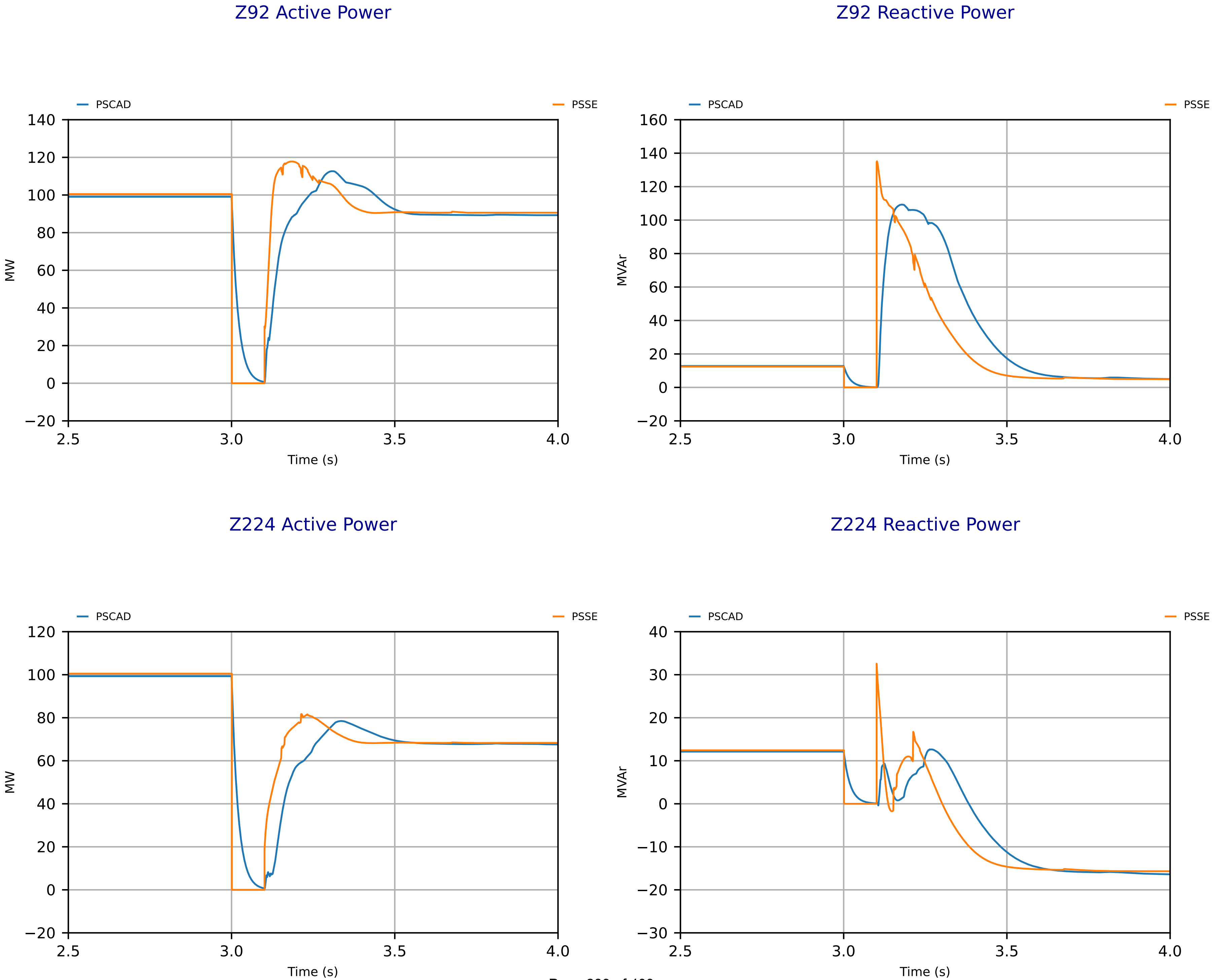




CMLD_SMIB_SCR_3_XR_14_T3_3



CMLD_SMIB_SCR_3_XR_14_T3_4



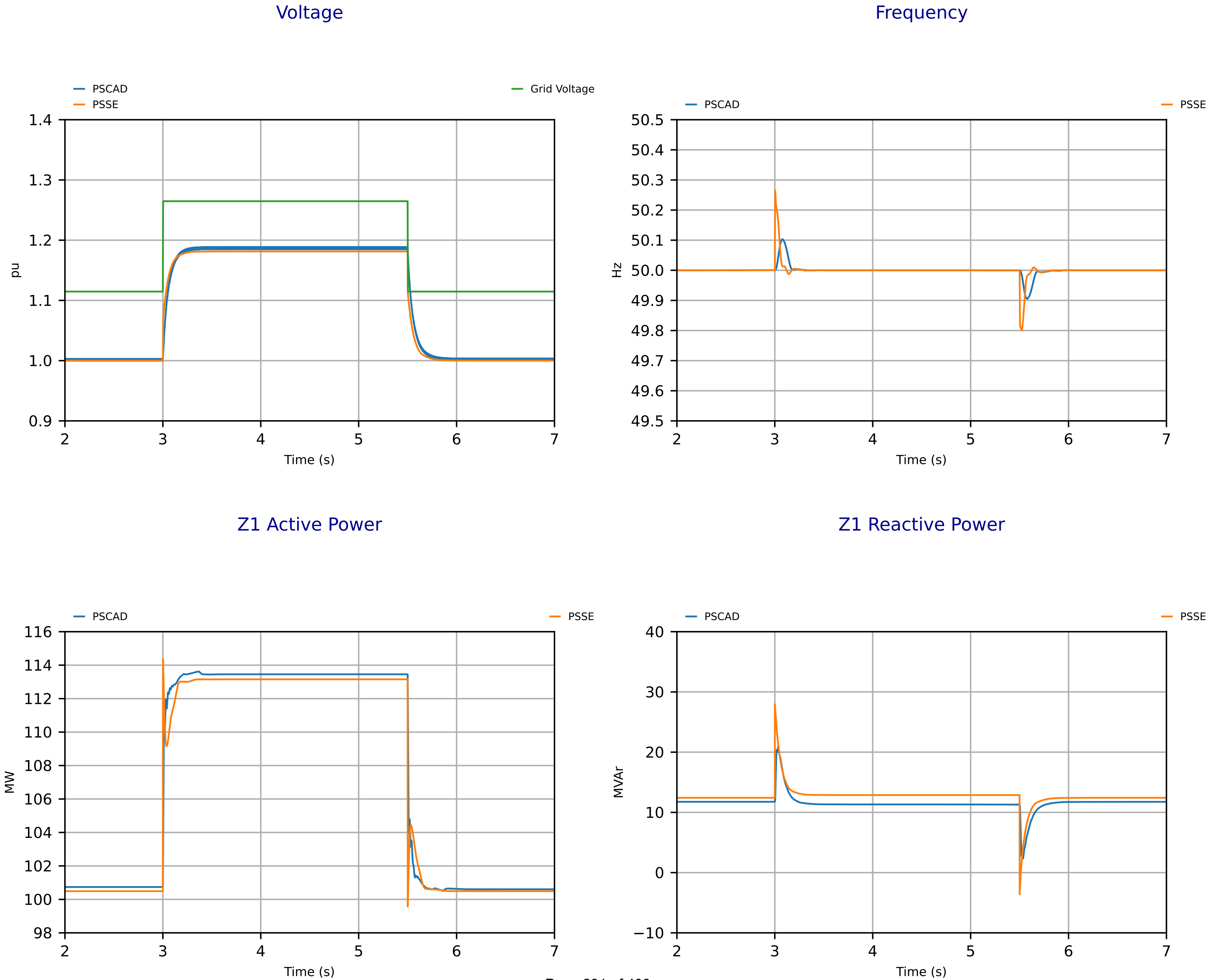
CMLD SMIB

SCR = 3, X/R = 14

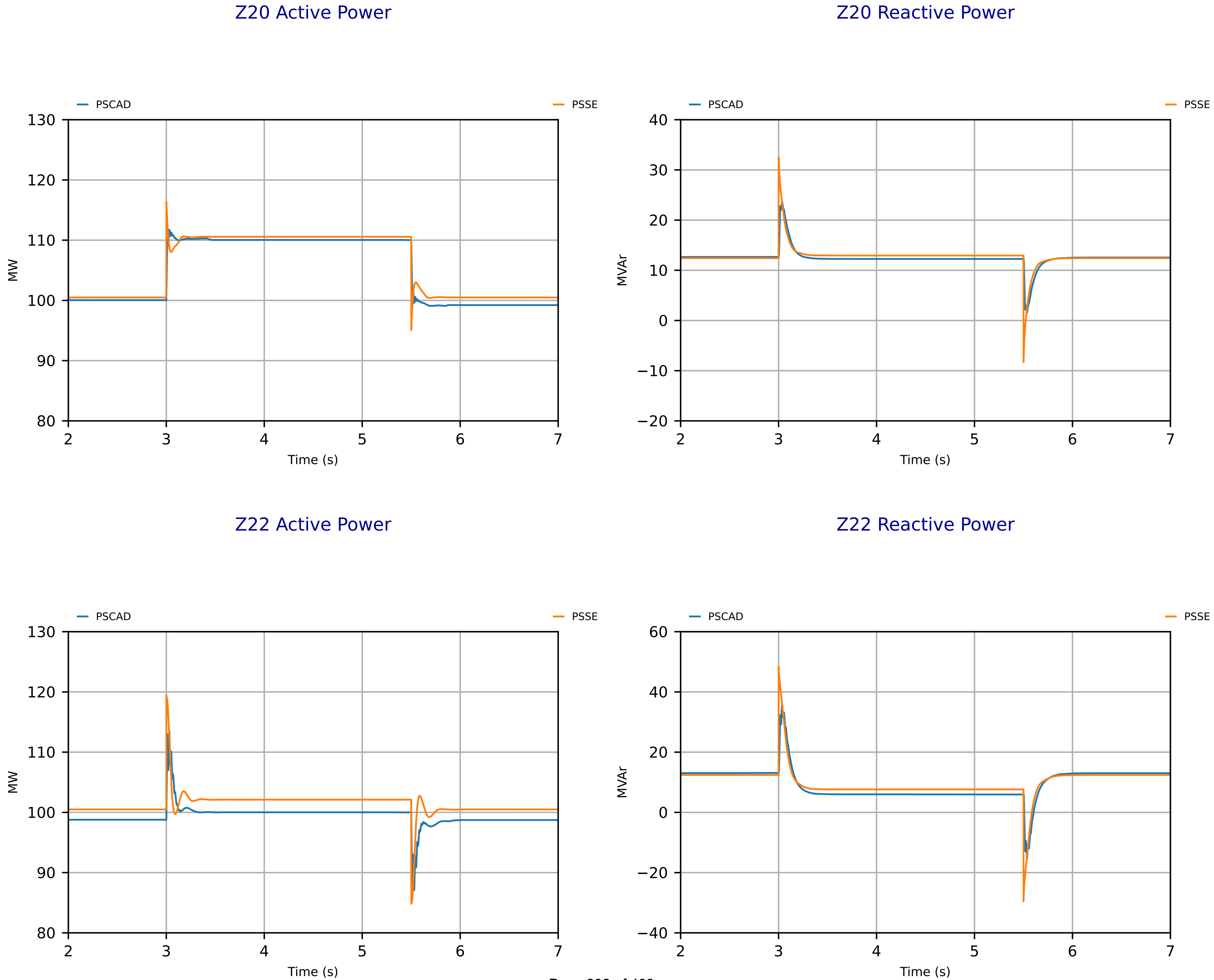
Test #4:

~115% Voltage disturbance for 2.5 s

CMLD_SMIB_SCR_3_XR_14_T4_1

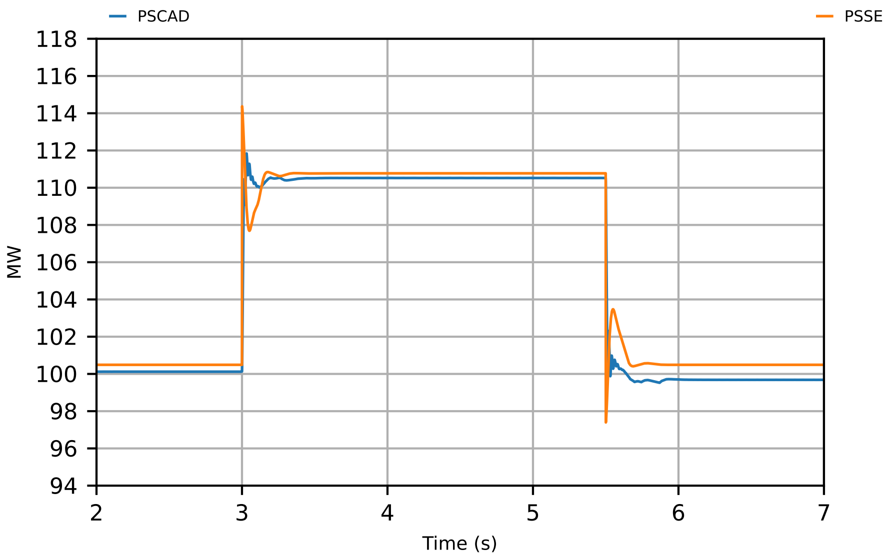


CMLD_SMIB_SCR_3_XR_14_T4_2

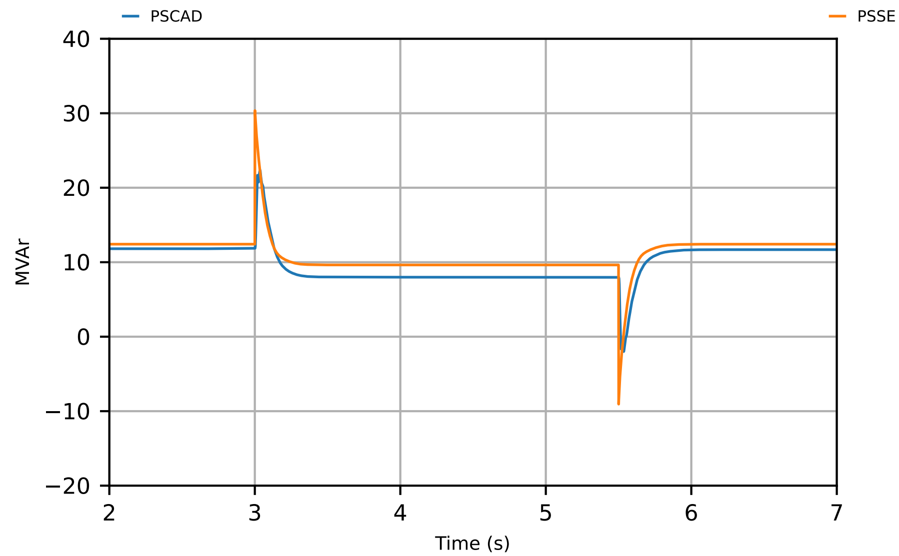


CMLD_SMIB_SCR_3_XR_14_T4_3

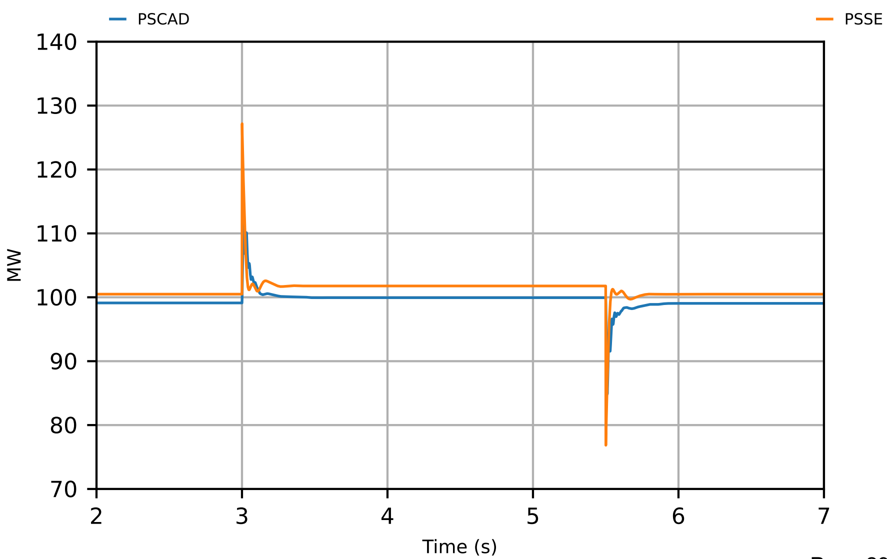
Z29 Active Power



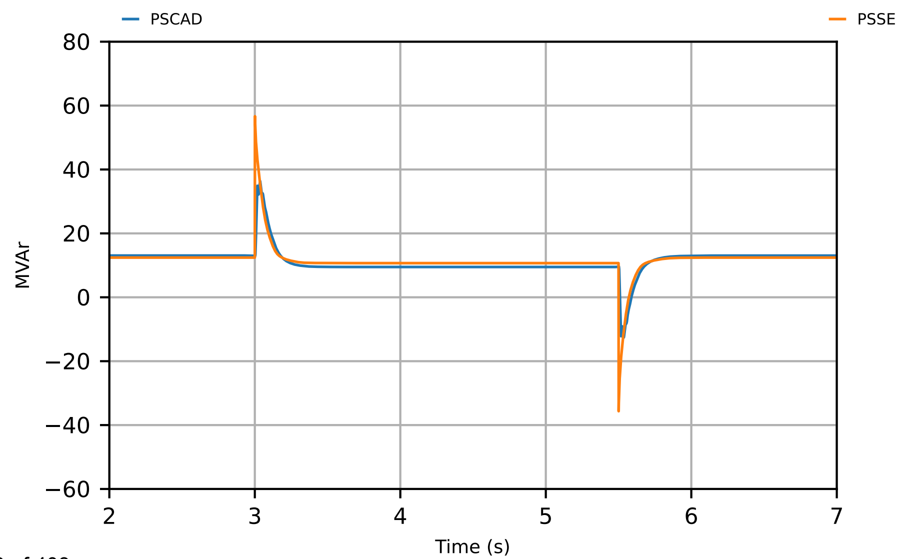
Z29 Reactive Power



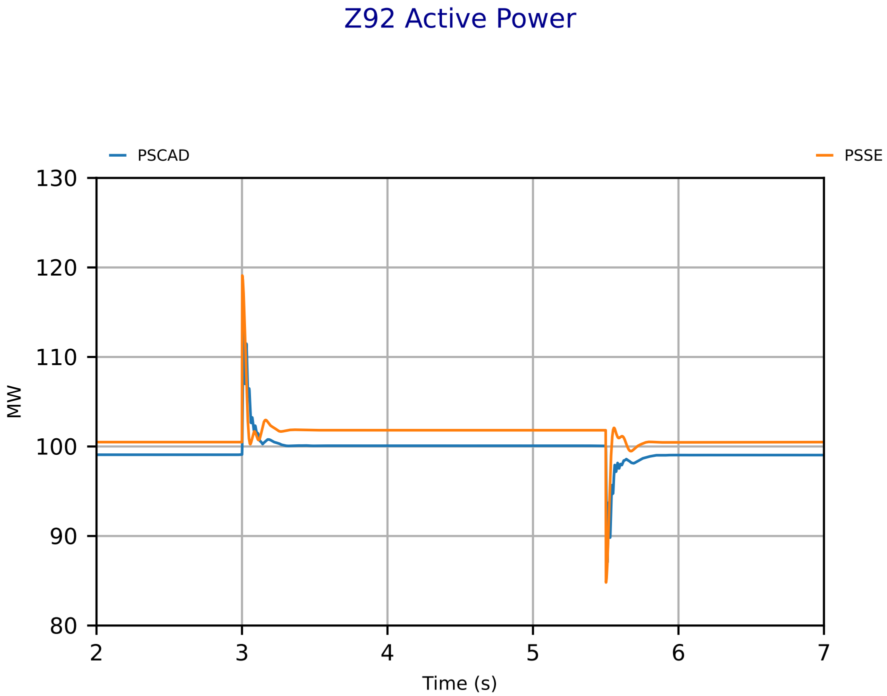
Z82 Active Power

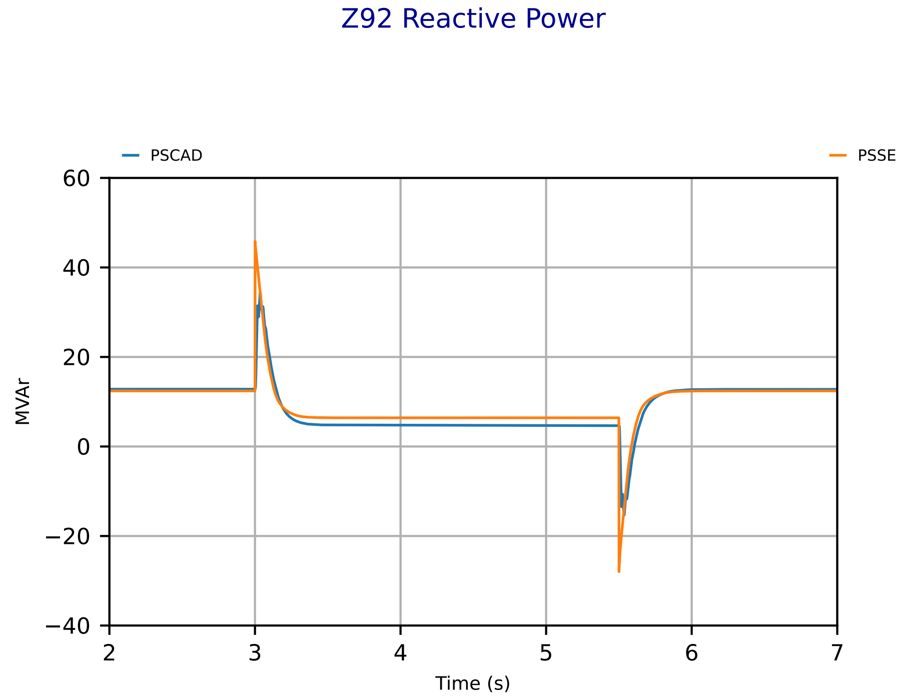


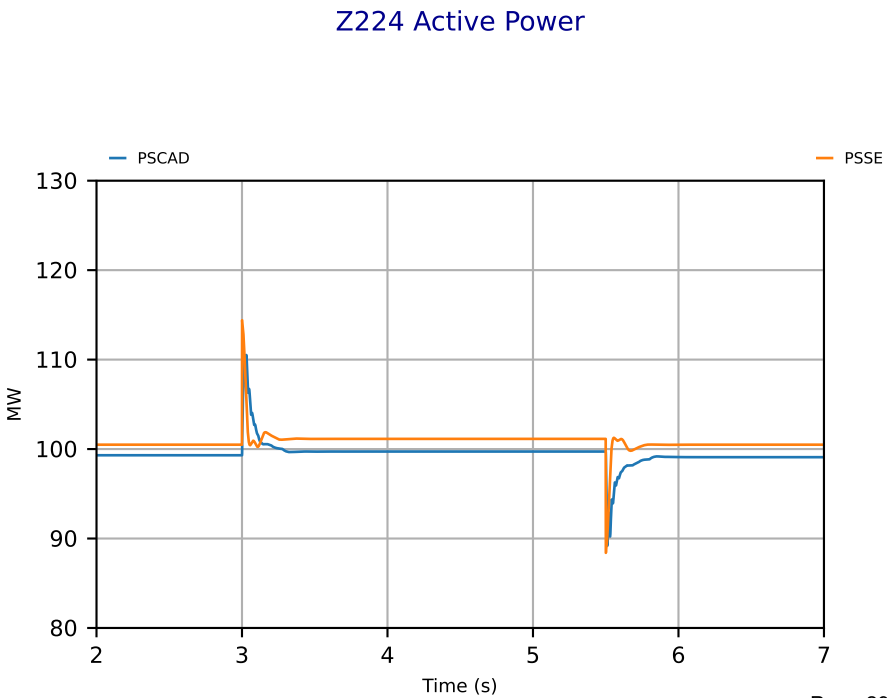
Z82 Reactive Power

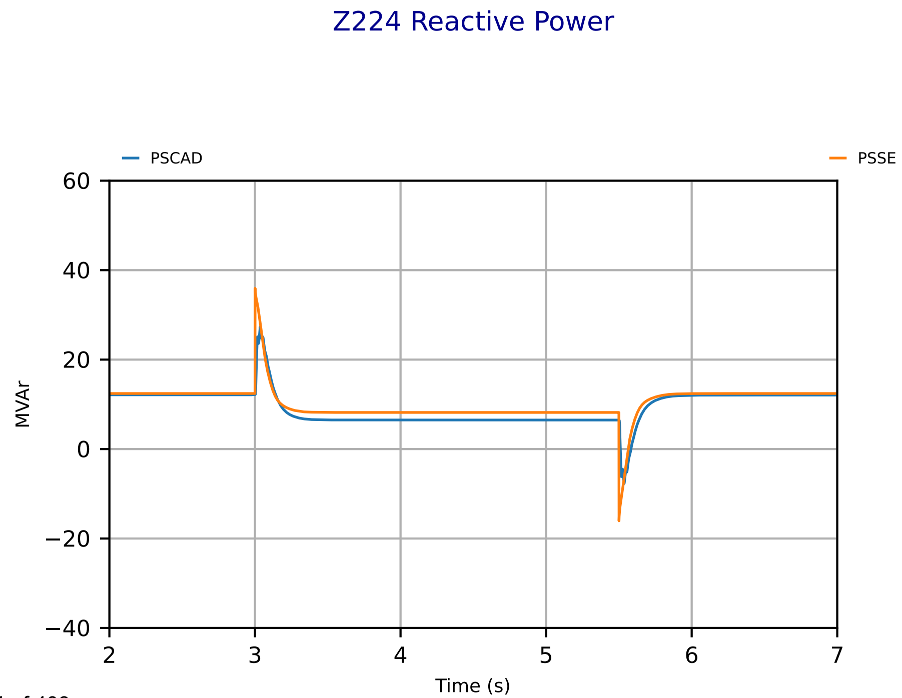


CMLD_SMIB_SCR_3_XR_14_T4_4









CMLD SMIB

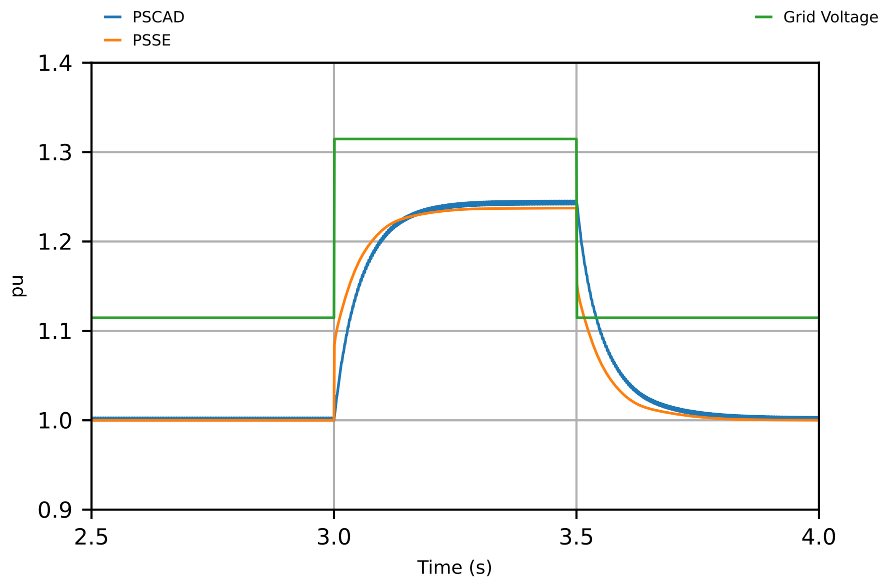
SCR = 3, X/R = 14

Test #5:

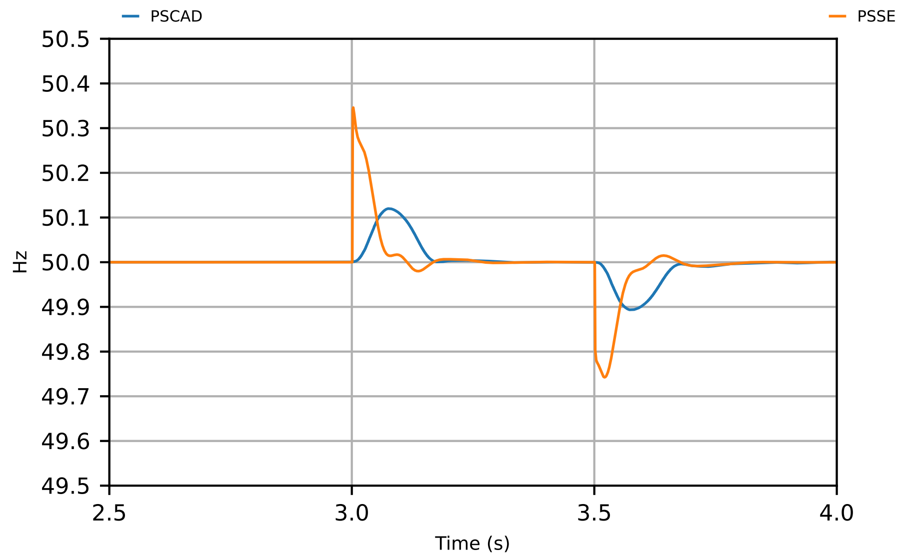
~120% Voltage disturbance for 500 ms

CMLD_SMIB_SCR_3_XR_14_T5_1

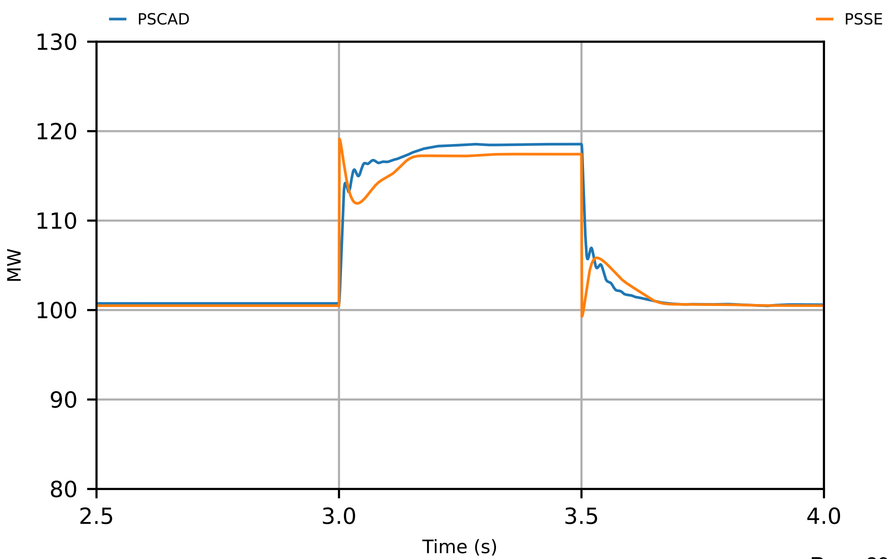
Voltage



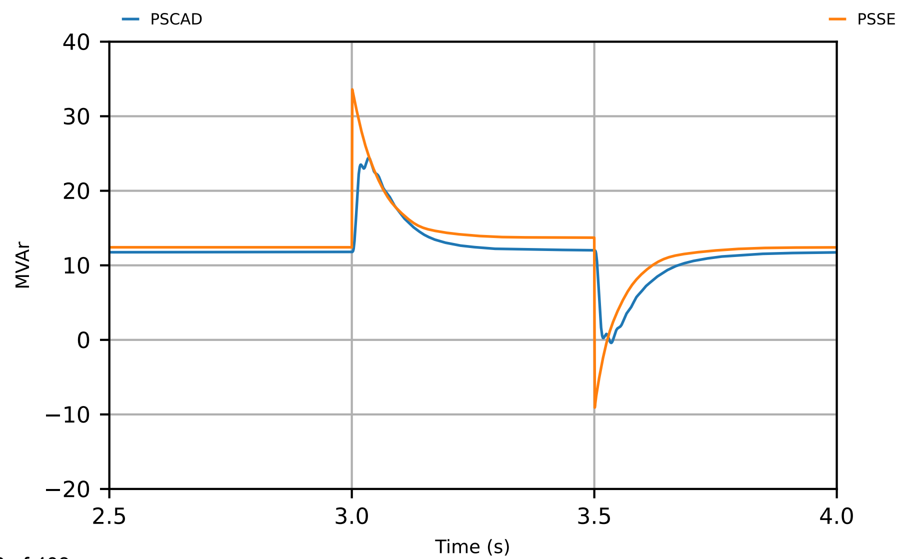
Frequency



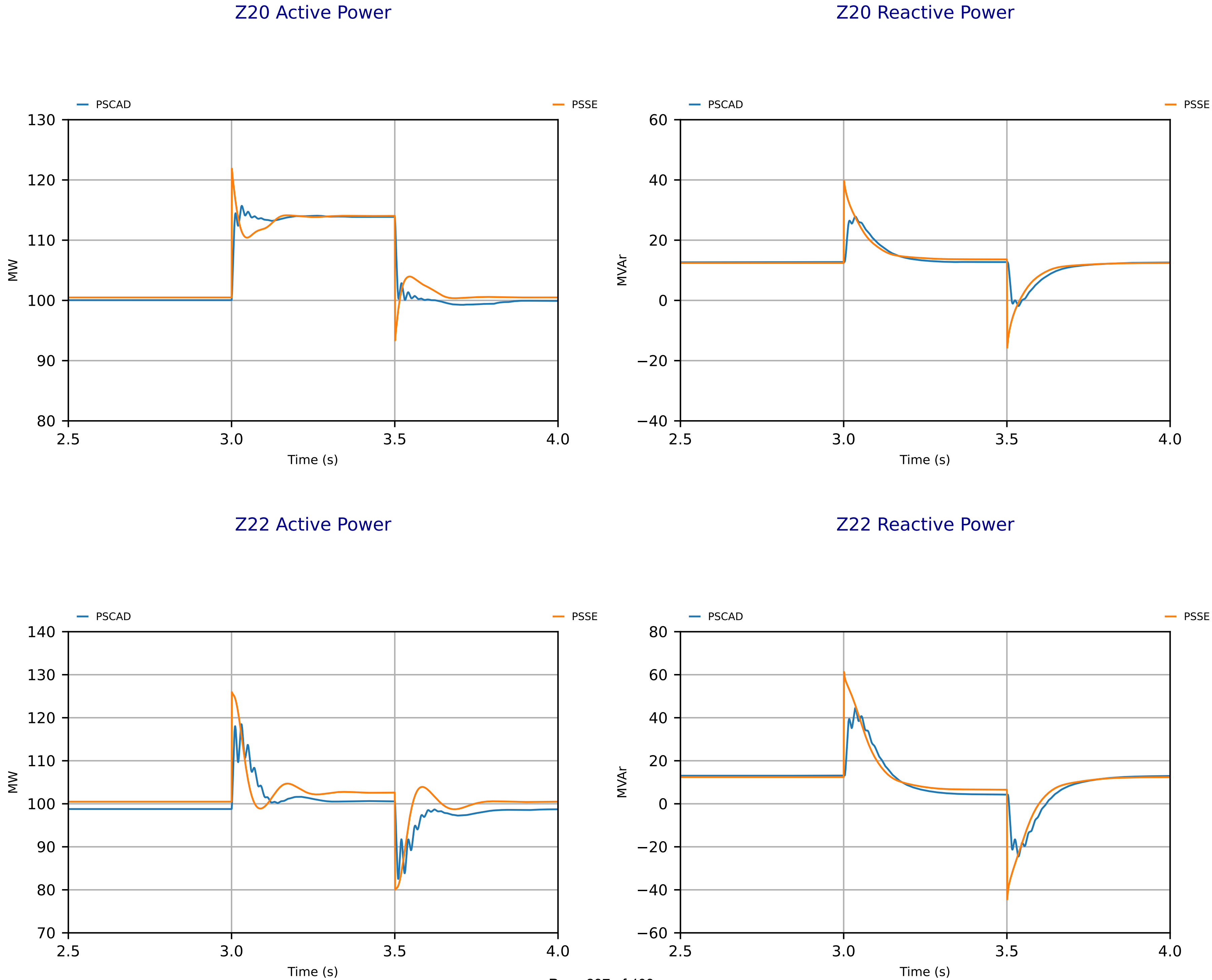
Z1 Active Power



Z1 Reactive Power

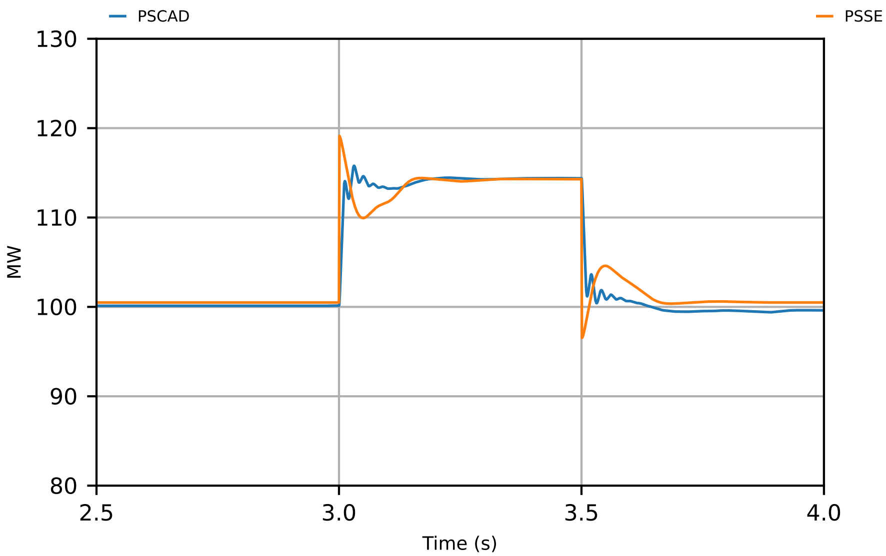


CMLD_SMIB_SCR_3_XR_14_T5_2

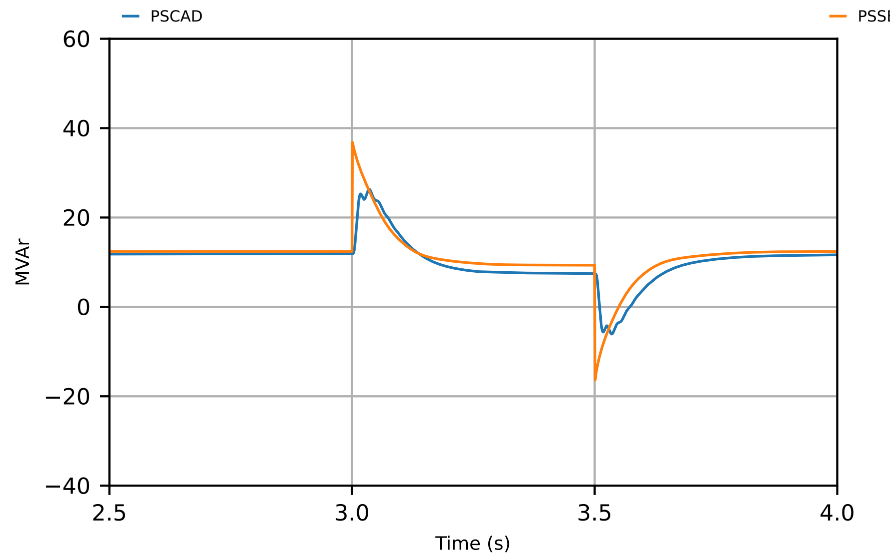


CMLD_SMIB_SCR_3_XR_14_T5_3

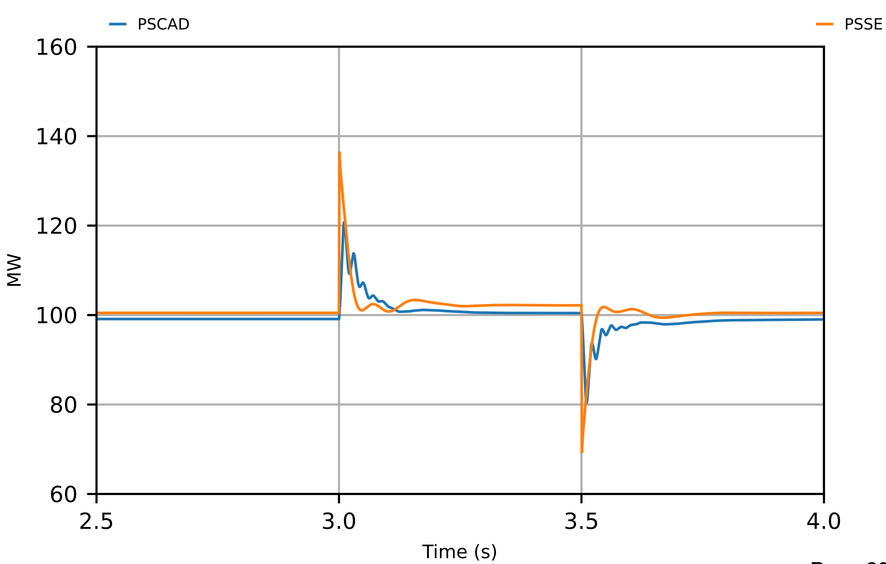
Z29 Active Power



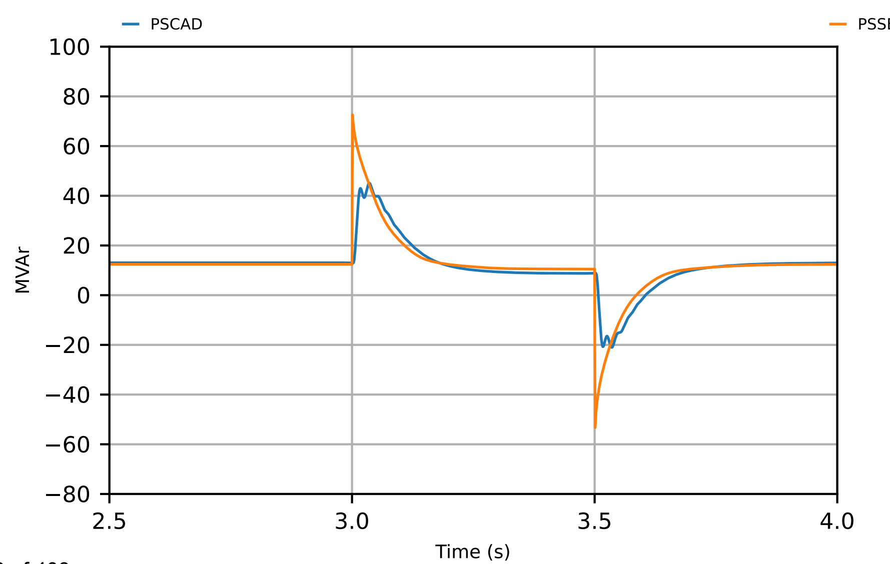
Z29 Reactive Power



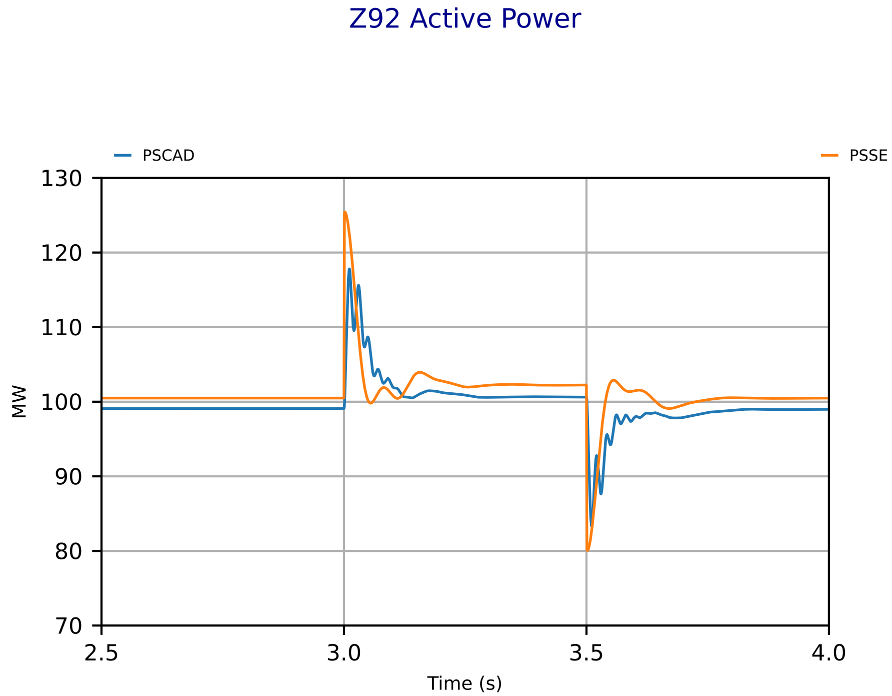
Z82 Active Power

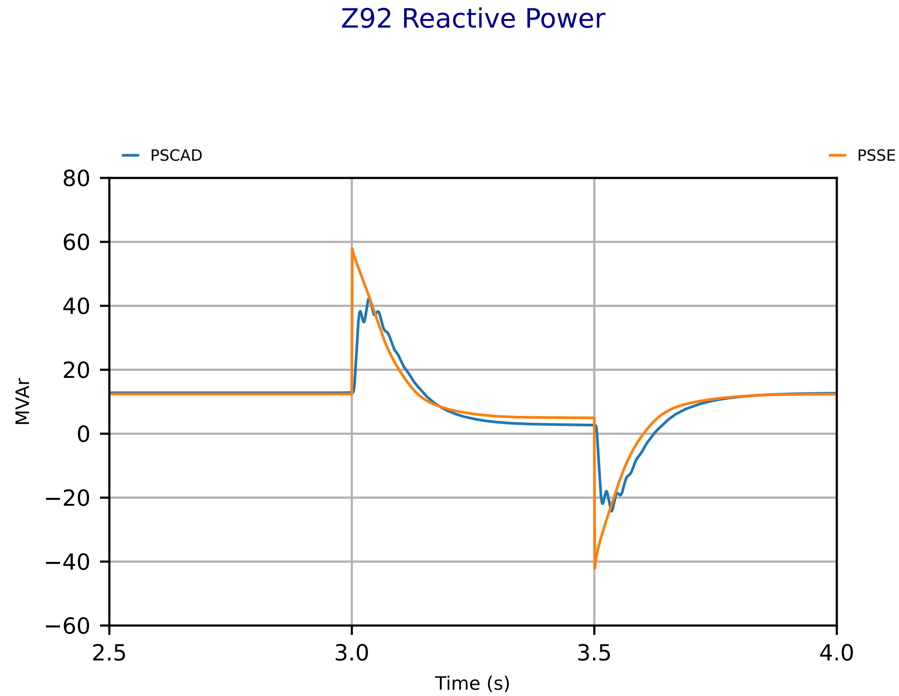


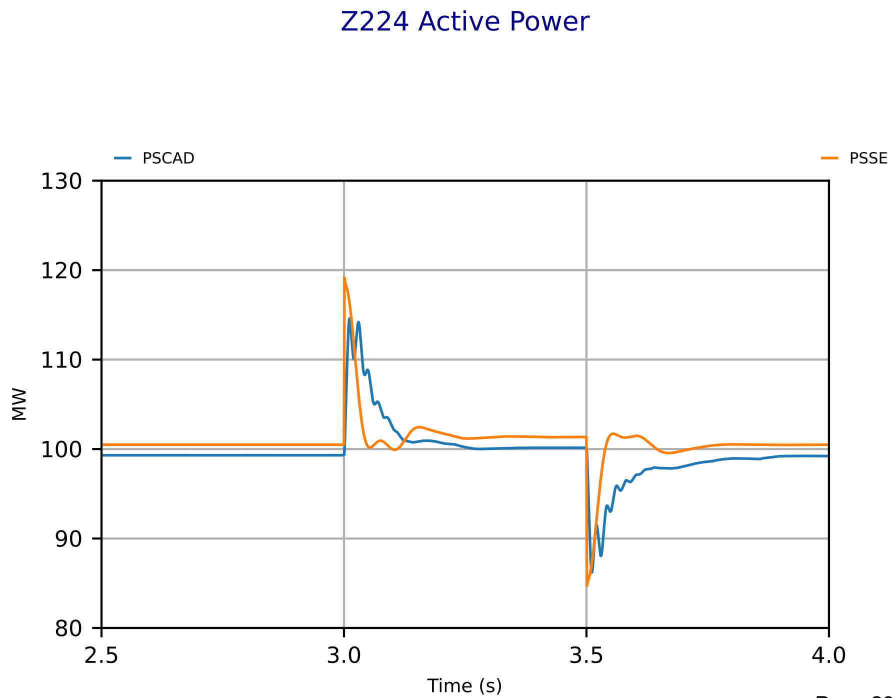
Z82 Reactive Power

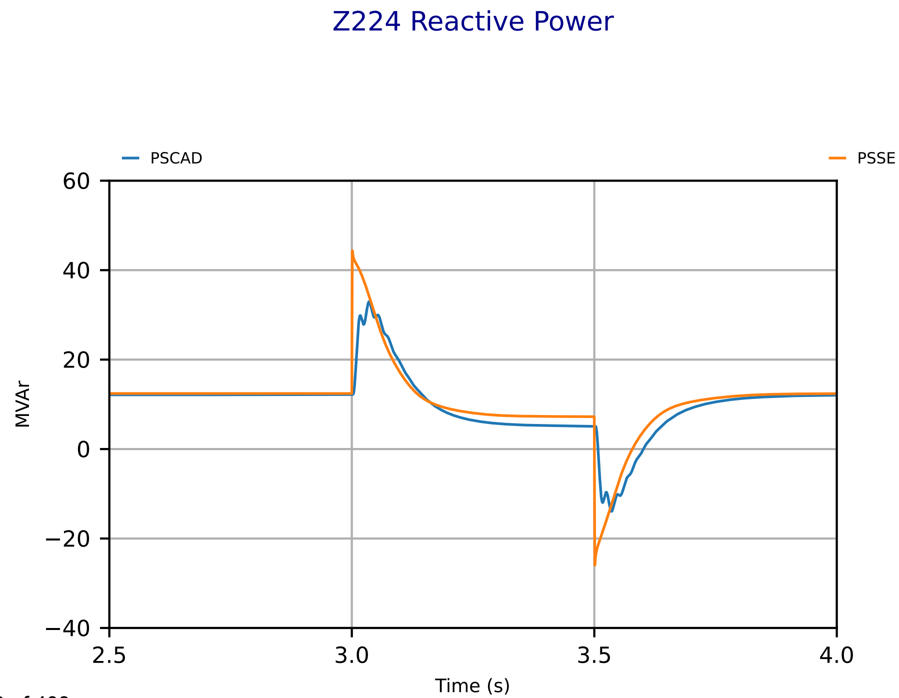


CMLD_SMIB_SCR_3_XR_14_T5_4









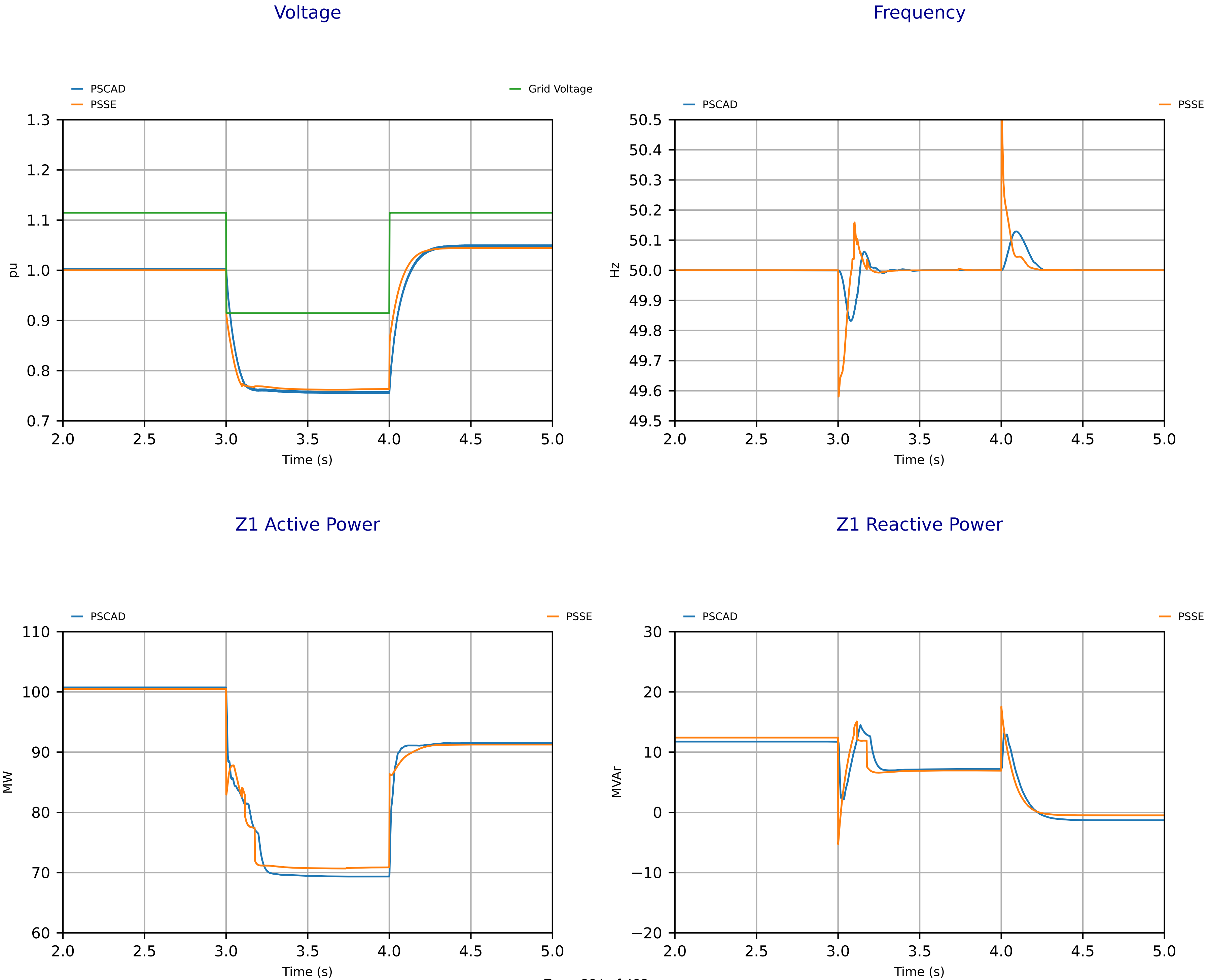
CMLD SMIB

SCR = 3, X/R = 14

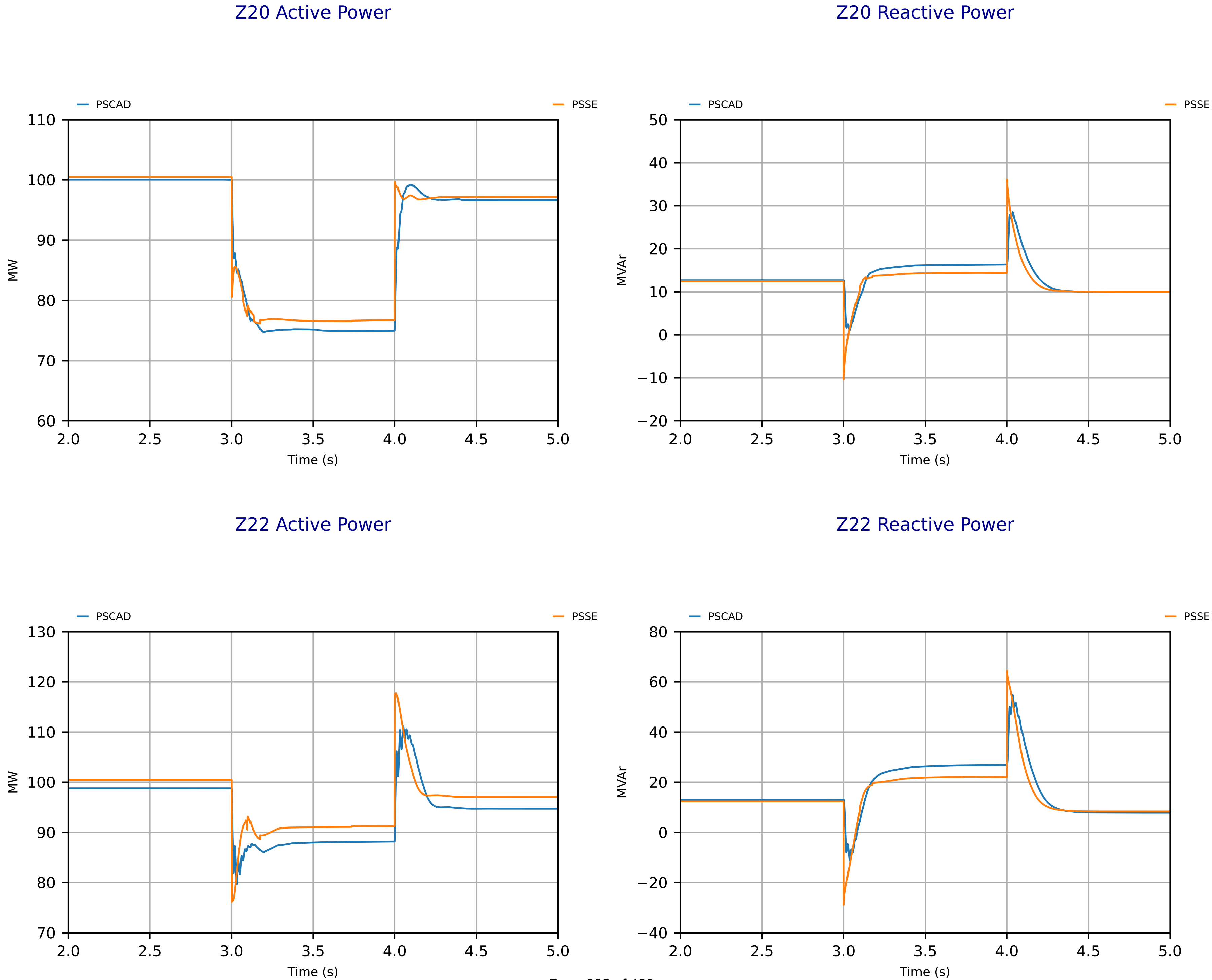
Test #6:

~80% Voltage disturbance for 1 sec

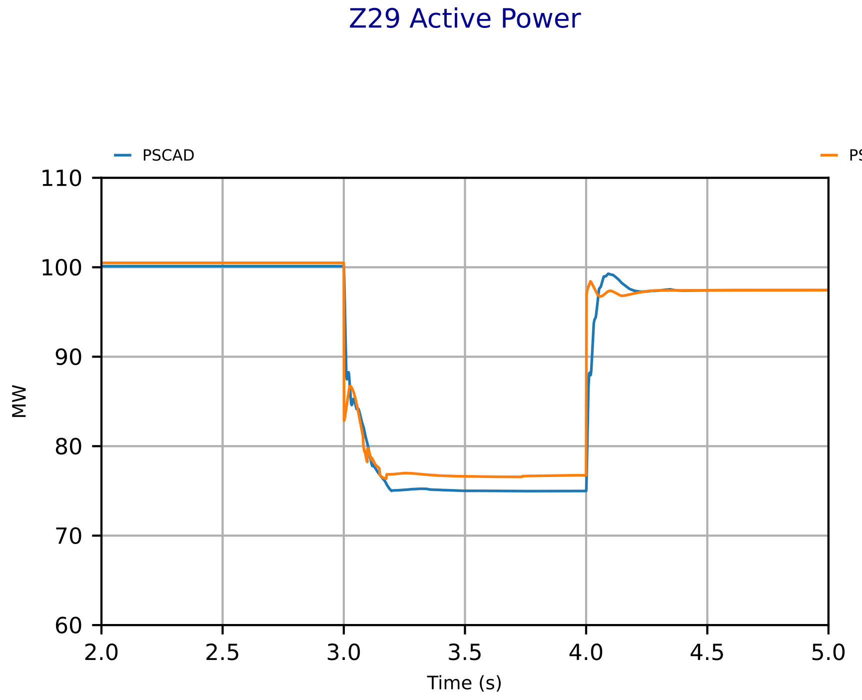
CMLD_SMIB_SCR_3_XR_14_T6_1

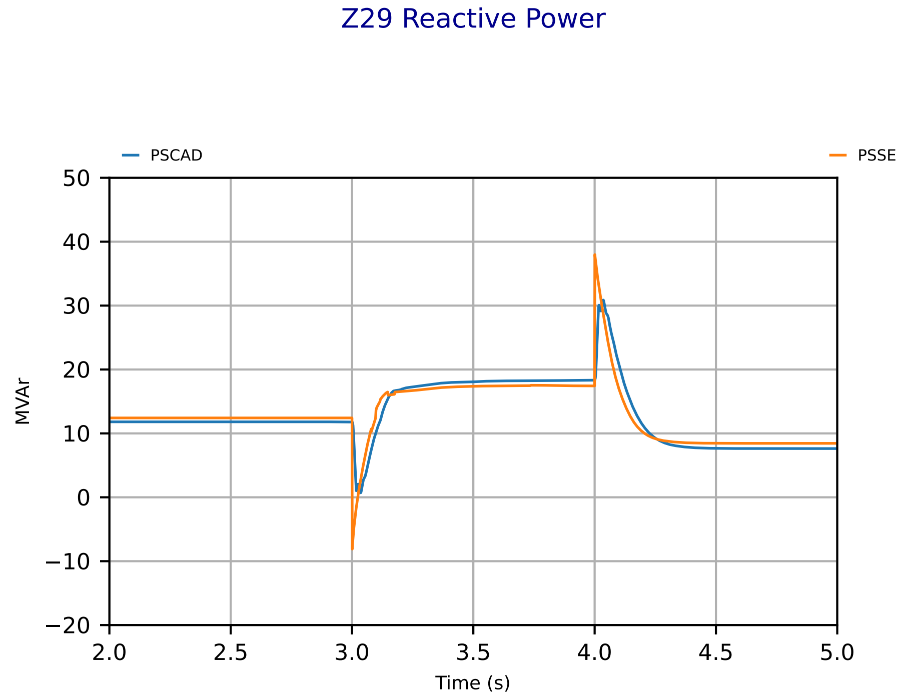


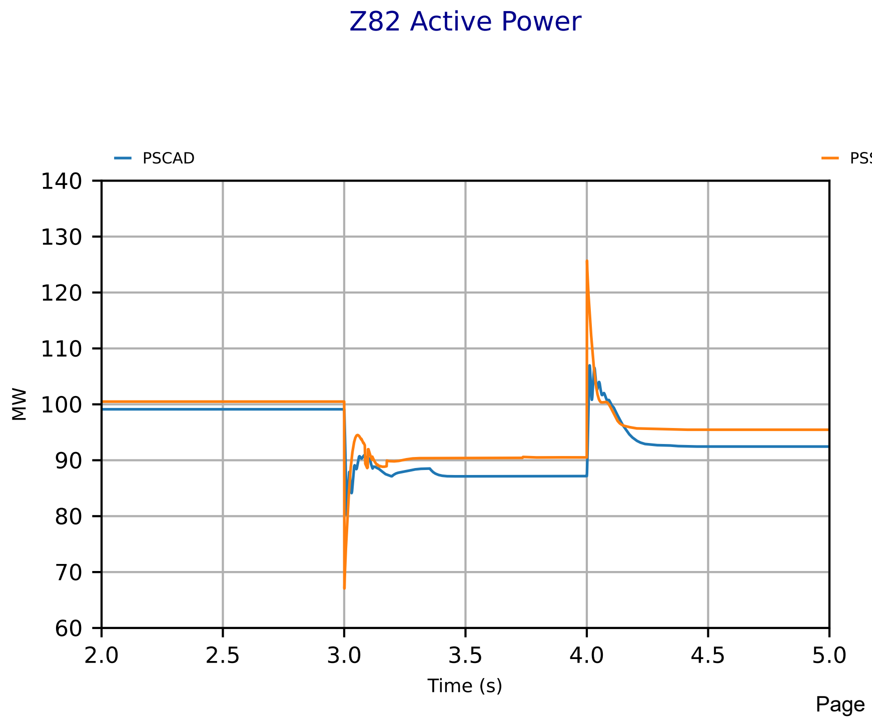
CMLD_SMIB_SCR_3_XR_14_T6_2

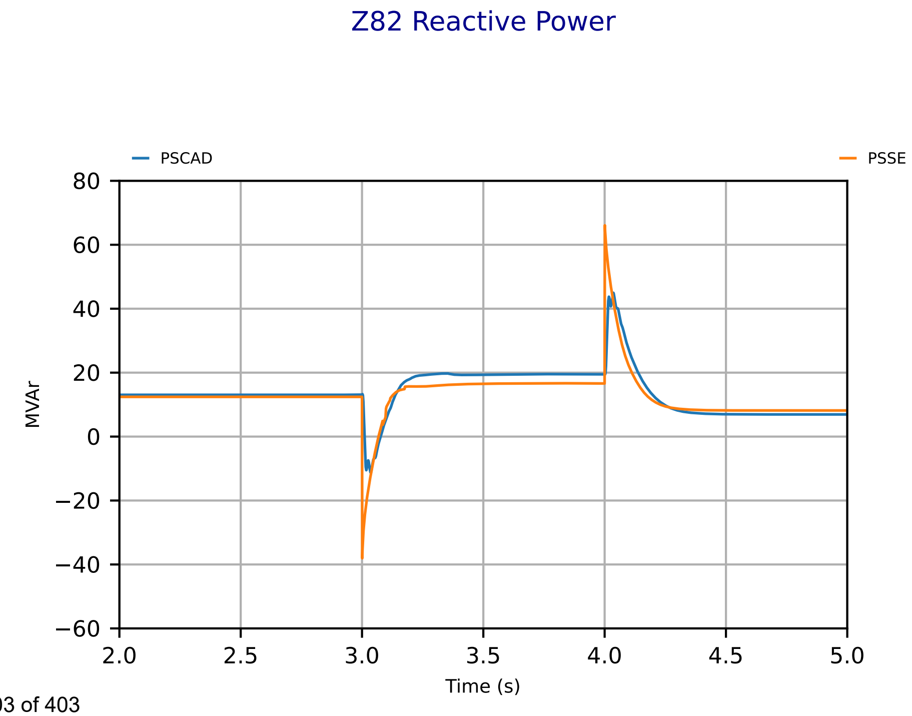


CMLD_SMIB_SCR_3_XR_14_T6_3

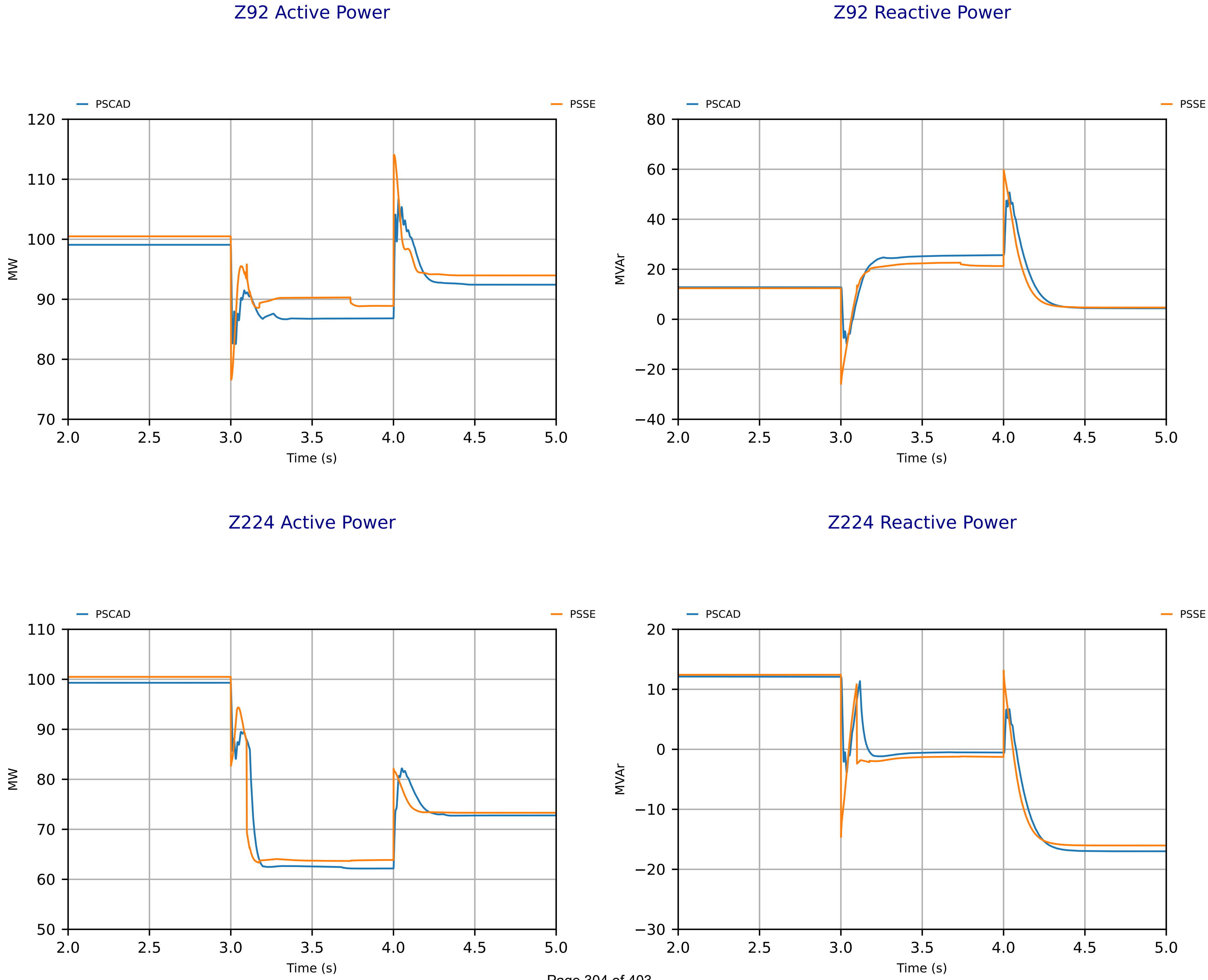








CMLD_SMIB_SCR_3_XR_14_T6_4



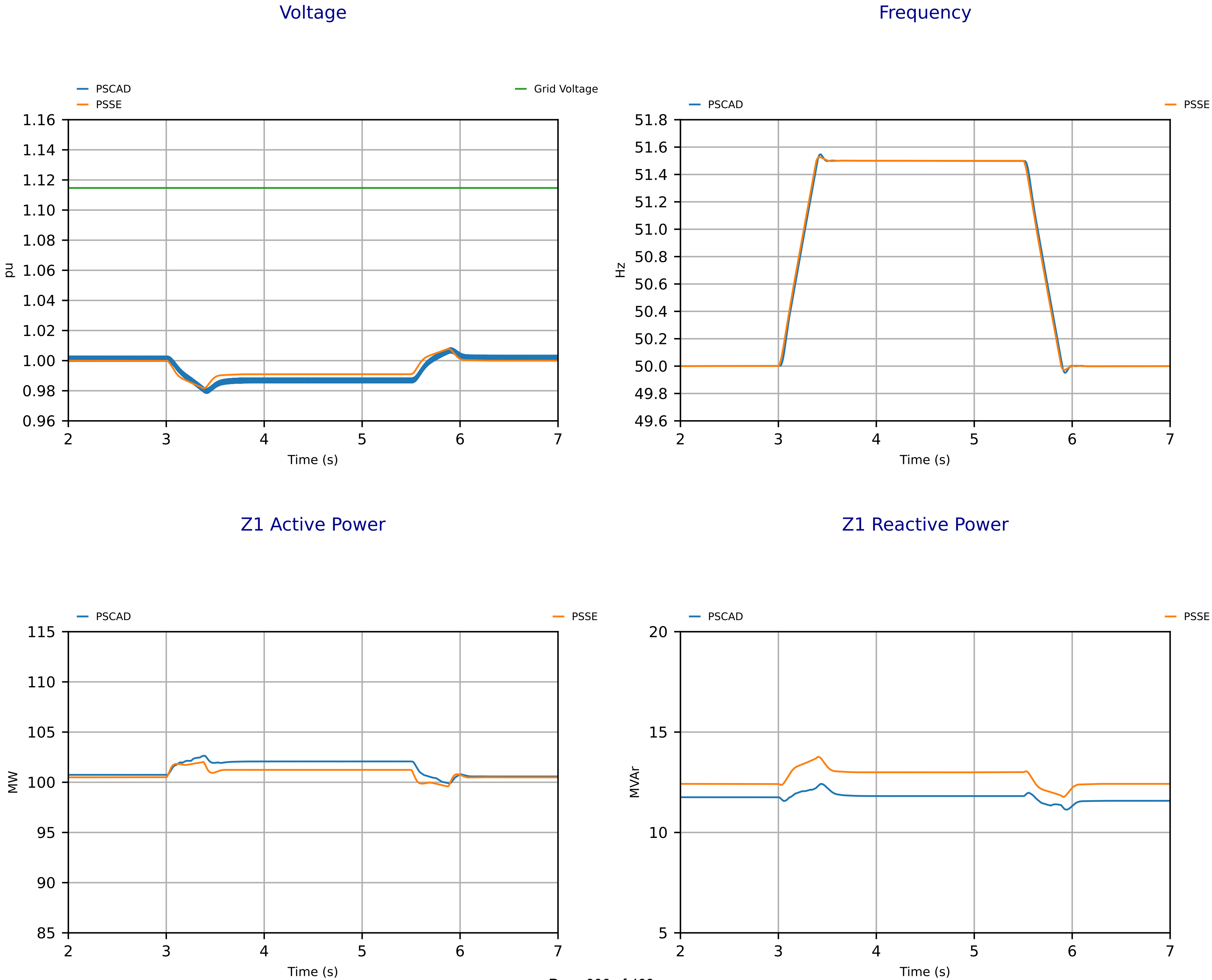
CMLD SMIB

SCR = 3, X/R = 14

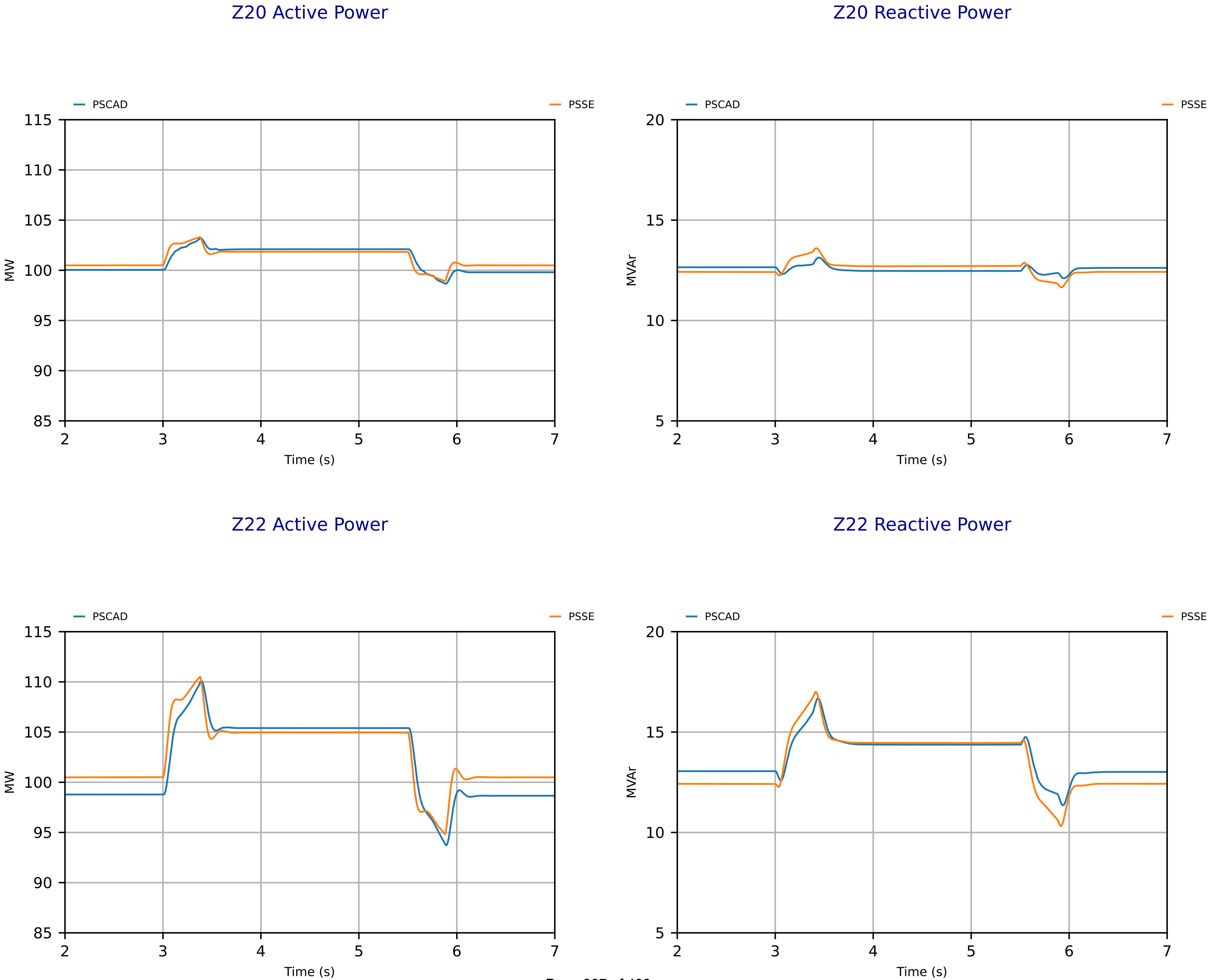
Test #7:

51.5 Hz frequency step for 2.5 sec (4 Hz/s)

CMLD_SMIB_SCR_3_XR_14_T7_1

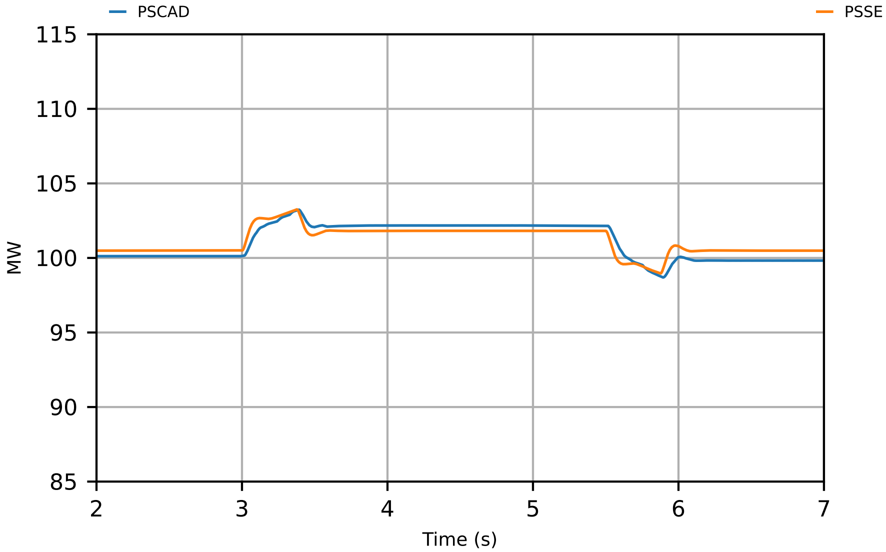


CMLD_SMIB_SCR_3_XR_14_T7_2

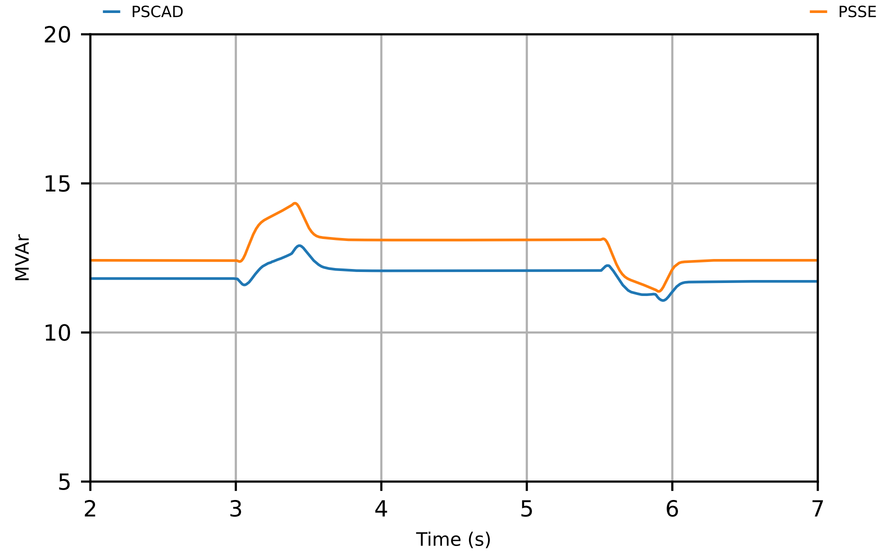


CMLD_SMIB_SCR_3_XR_14_T7_3

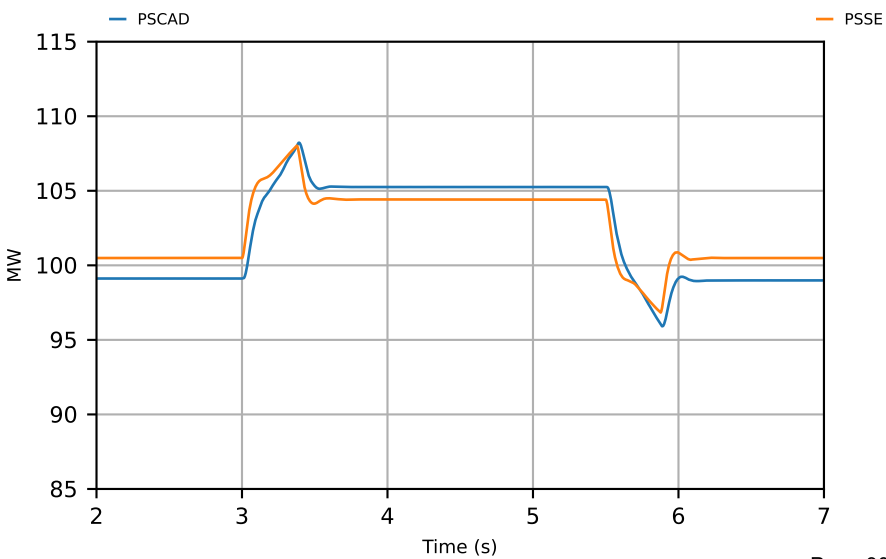
Z29 Active Power



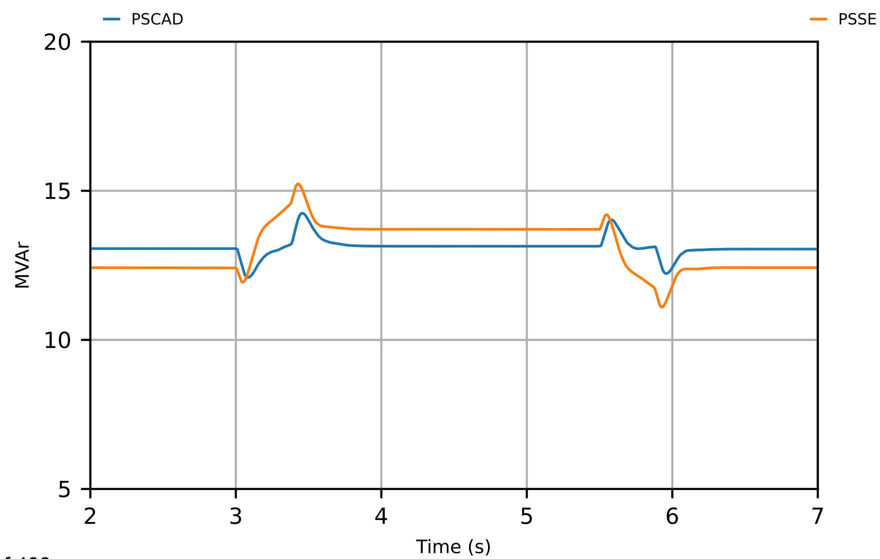
Z29 Reactive Power



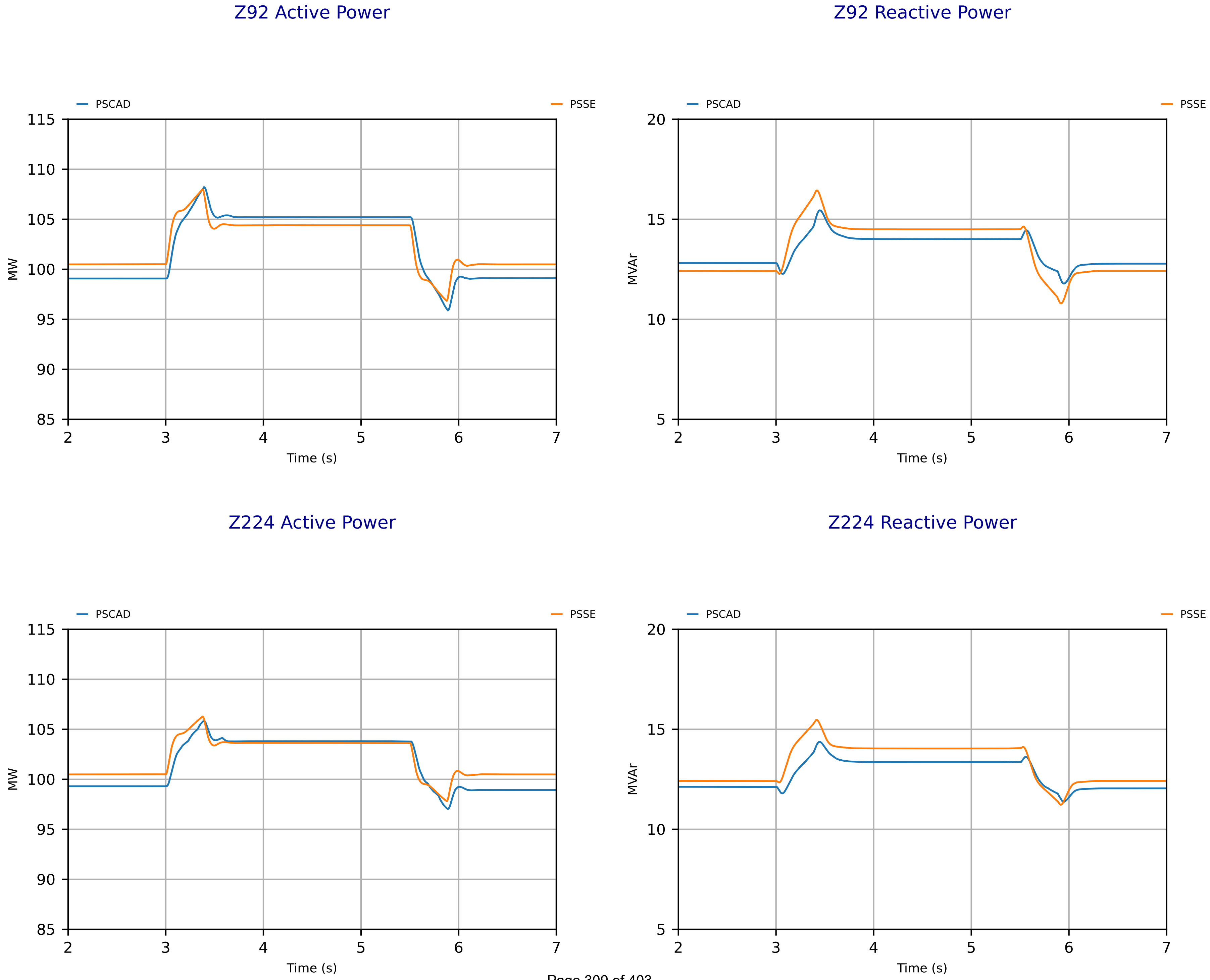
Z82 Active Power



Z82 Reactive Power



CMLD_SMIB_SCR_3_XR_14_T7_4



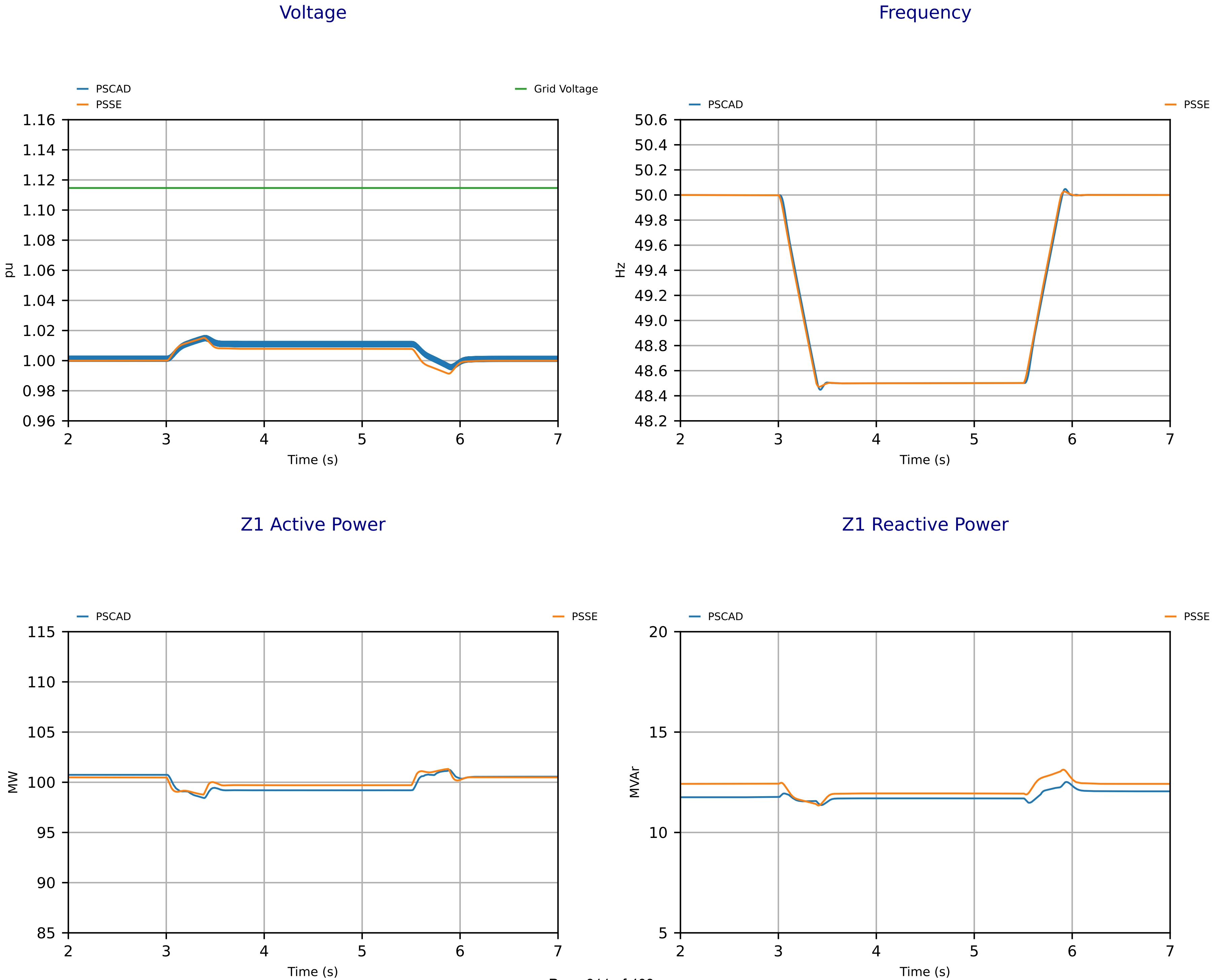
CMLD SMIB

SCR = 3, X/R = 14

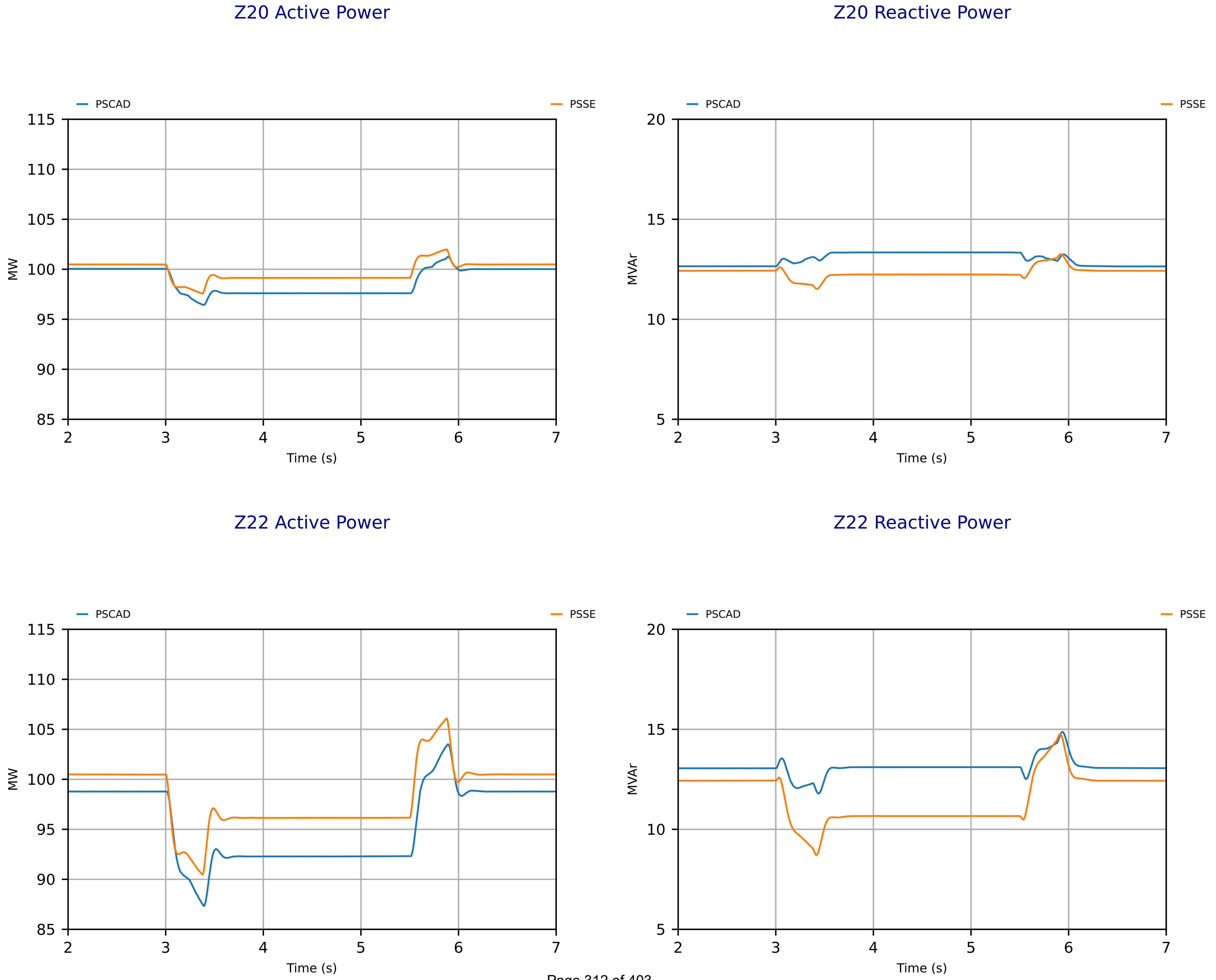
Test #8:

48.5 Hz frequency step for 2.5 sec (4 Hz/s)

CMLD_SMIB_SCR_3_XR_14_T8_1

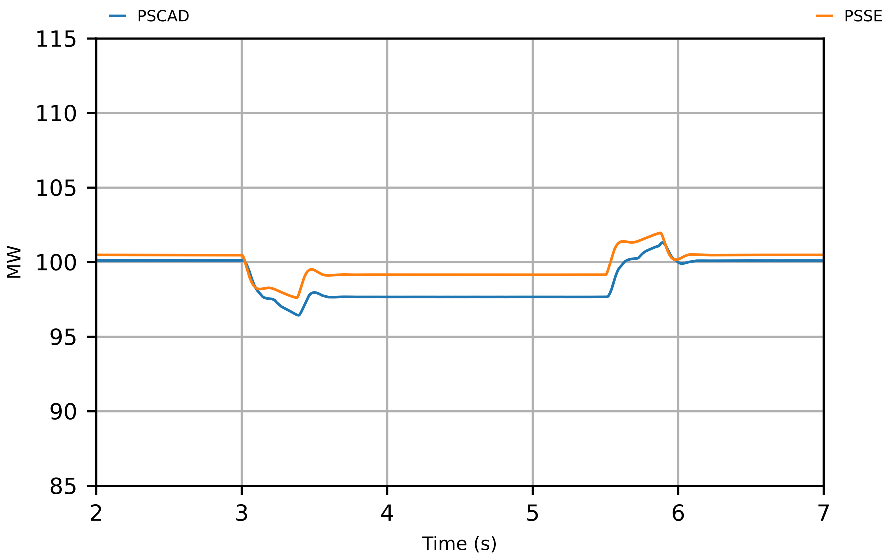


CMLD_SMIB_SCR_3_XR_14_T8_2

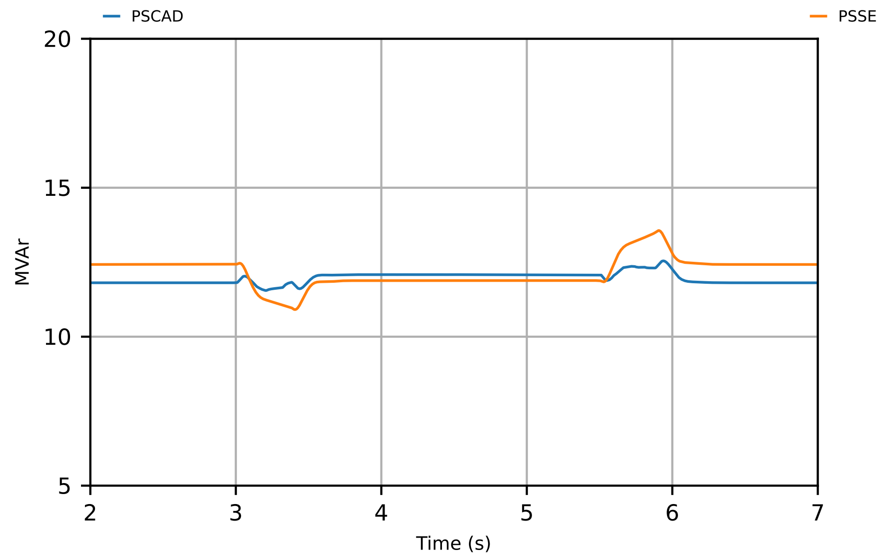


CMLD_SMIB_SCR_3_XR_14_T8_3

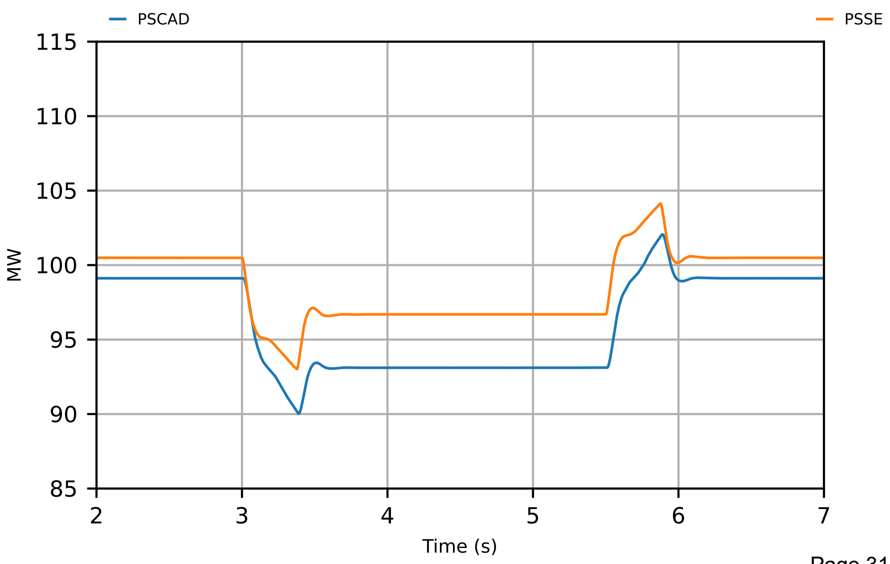
Z29 Active Power



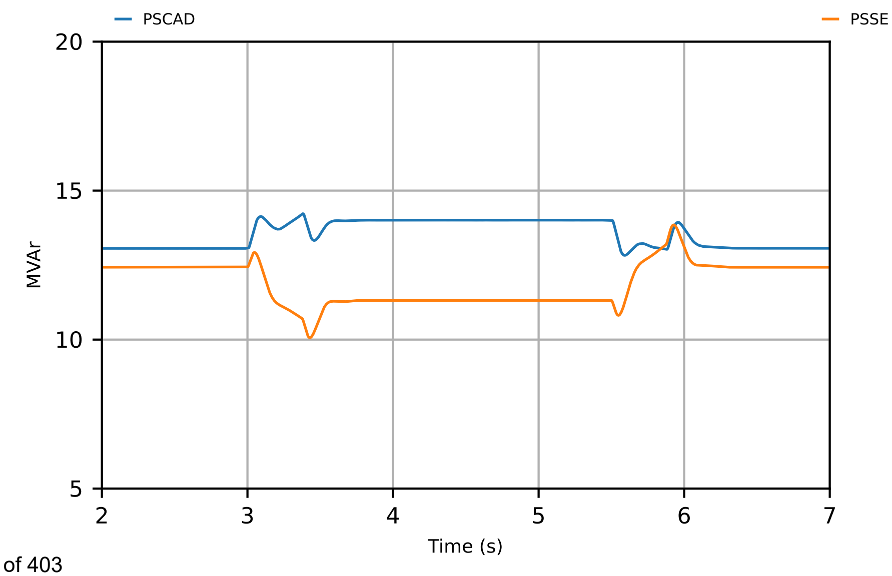
Z29 Reactive Power



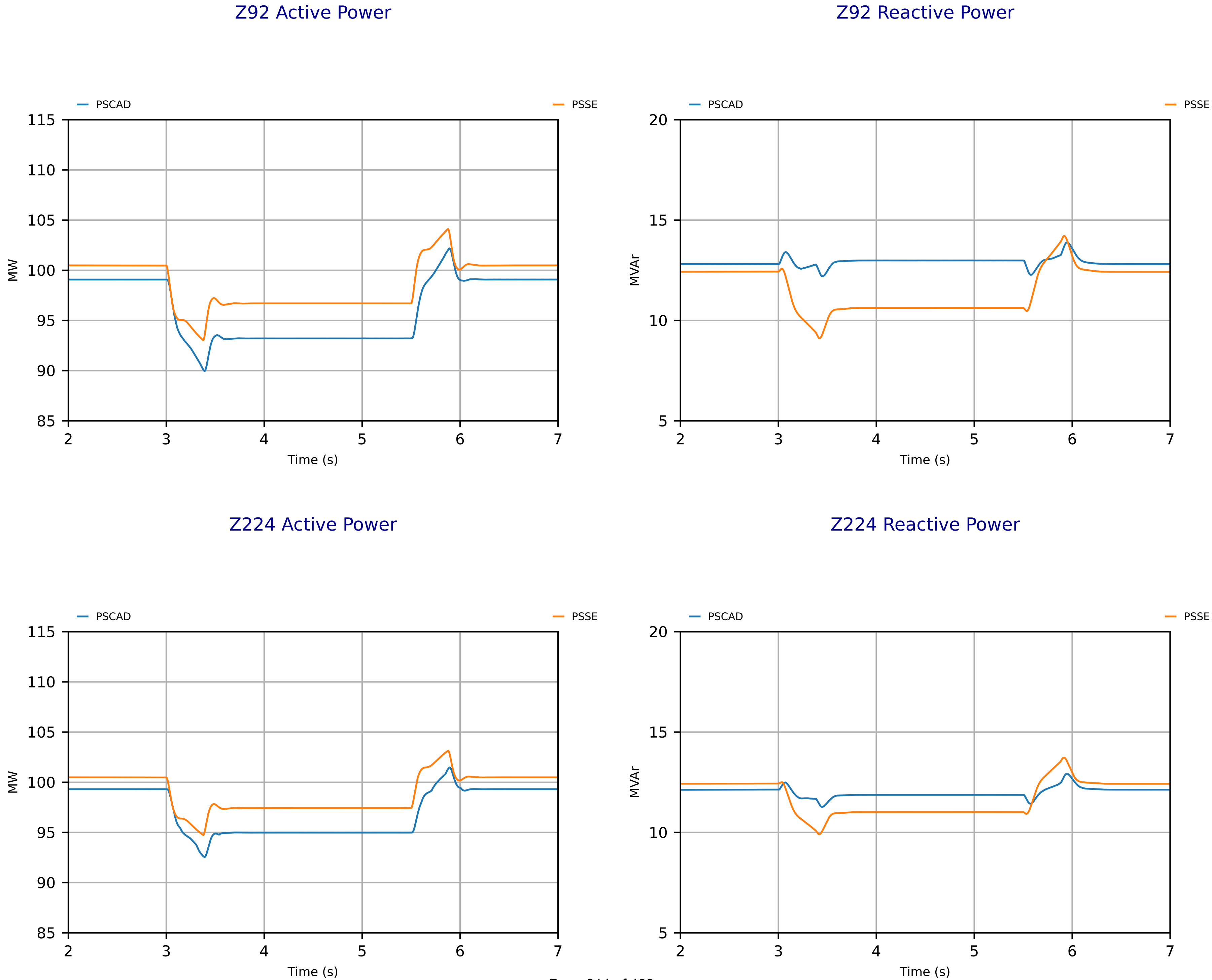
Z82 Active Power



Z82 Reactive Power



CMLD_SMIB_SCR_3_XR_14_T8_4



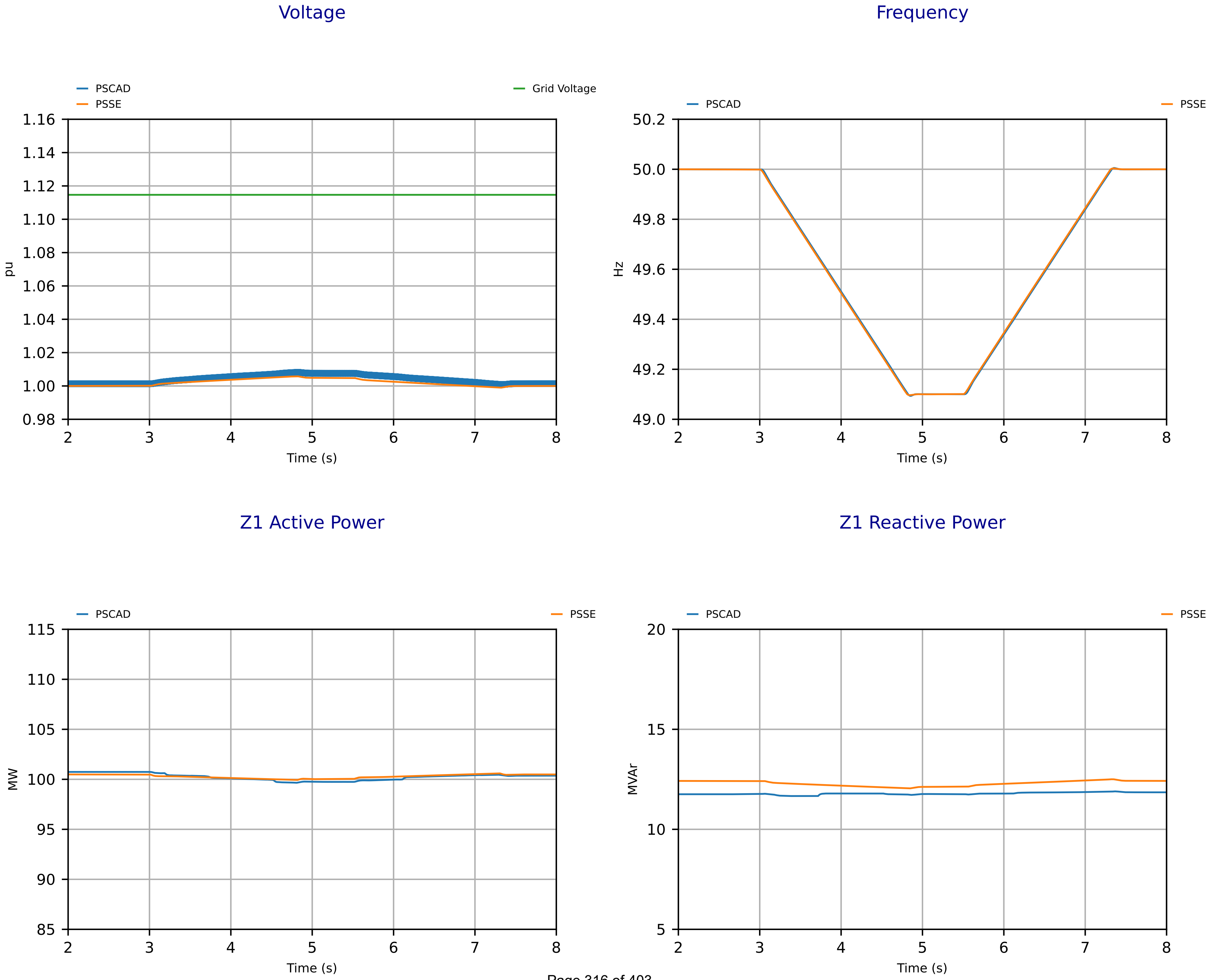
CMLD SMIB

SCR = 3, X/R = 14

Test #9:

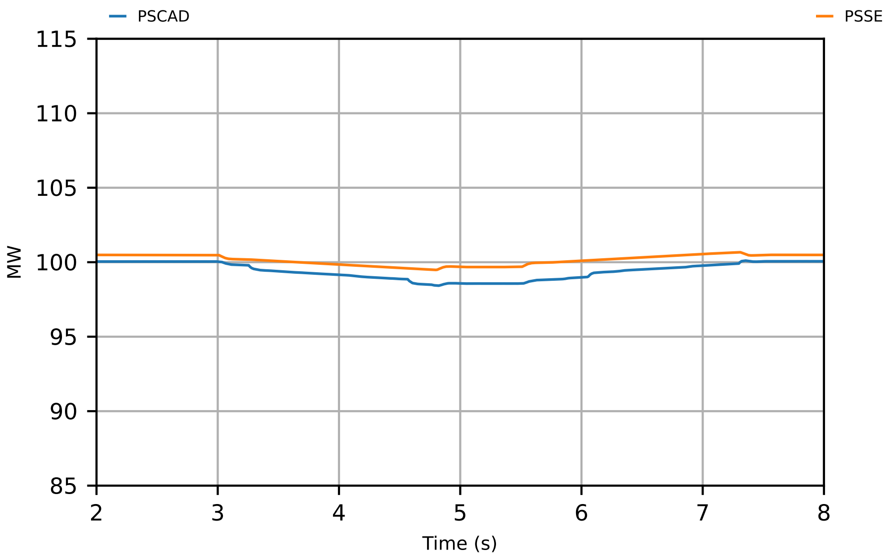
49.1 Hz slow frequency ramp (0.5 Hz/s)

CMLD_SMIB_SCR_3_XR_14_T9_1

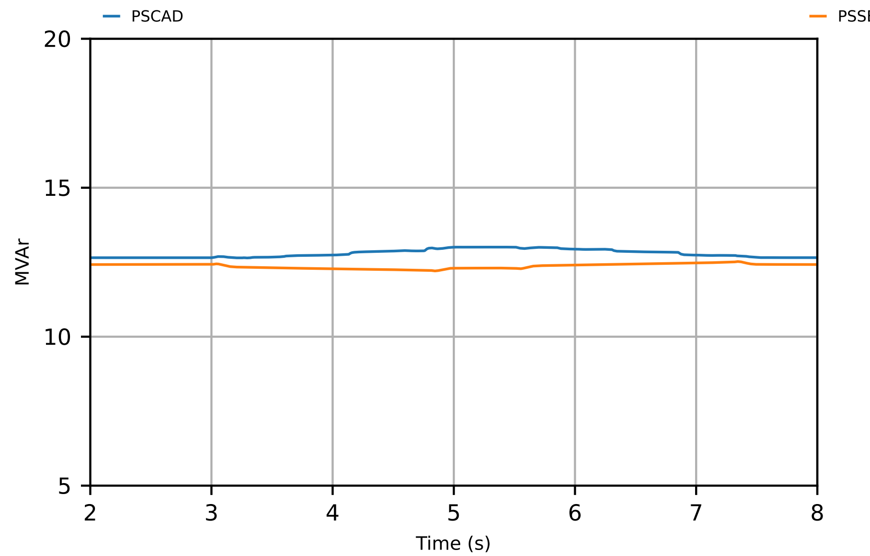


CMLD_SMIB_SCR_3_XR_14_T9_2

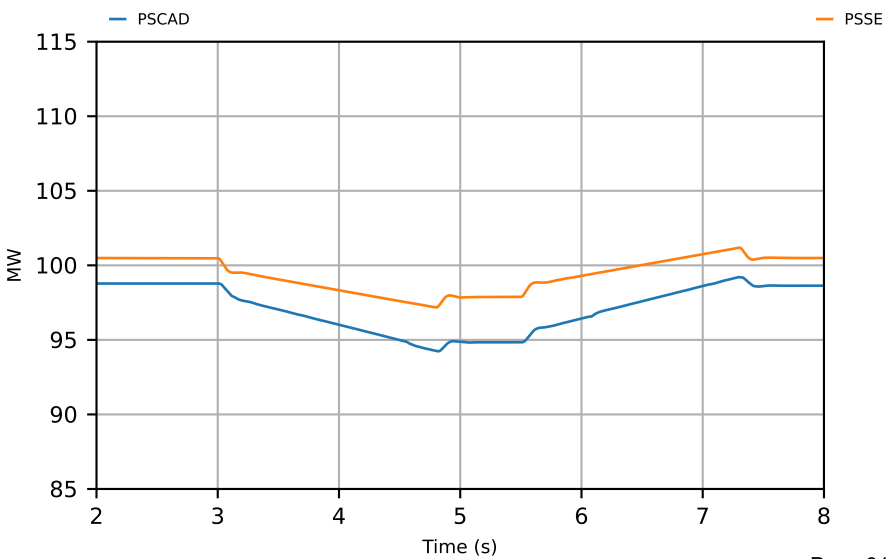
Z20 Active Power



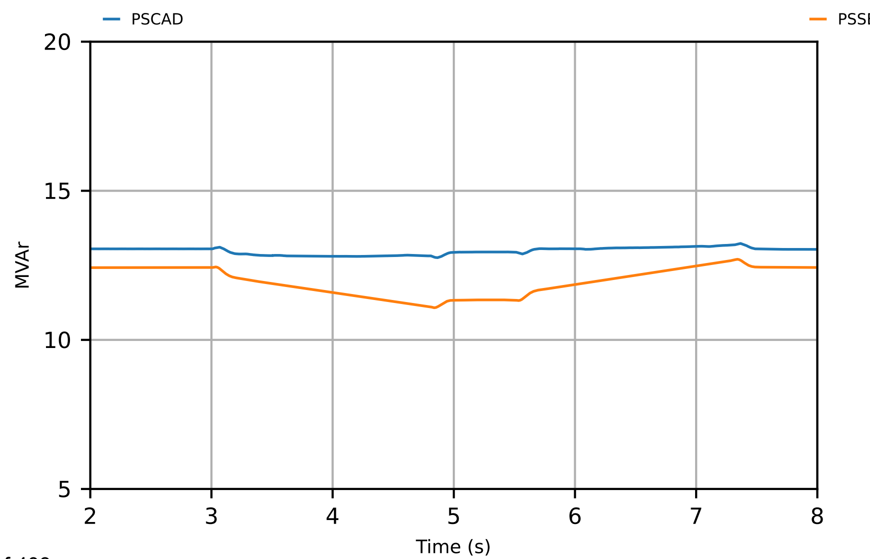
Z20 Reactive Power



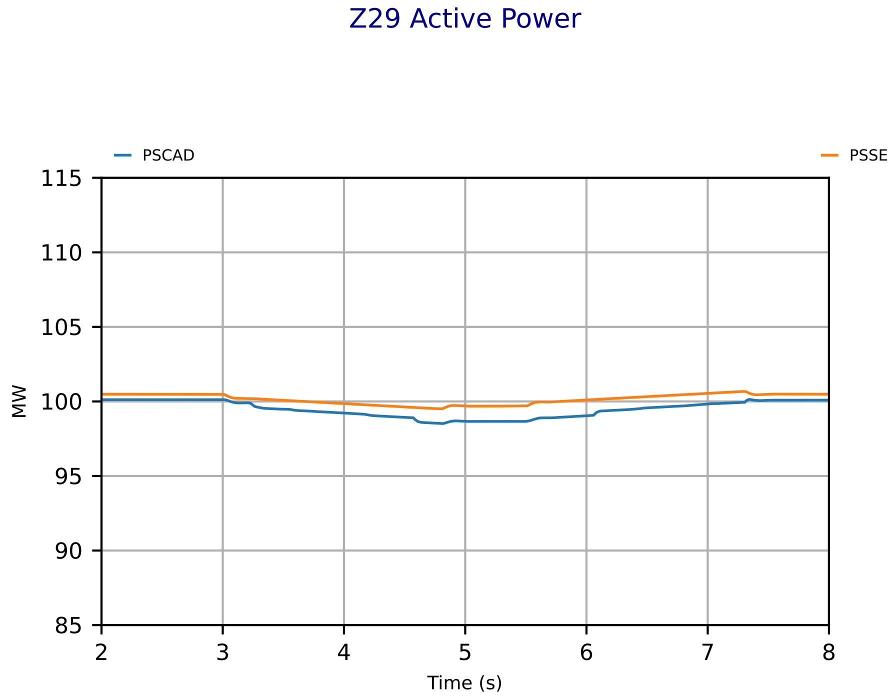
Z22 Active Power

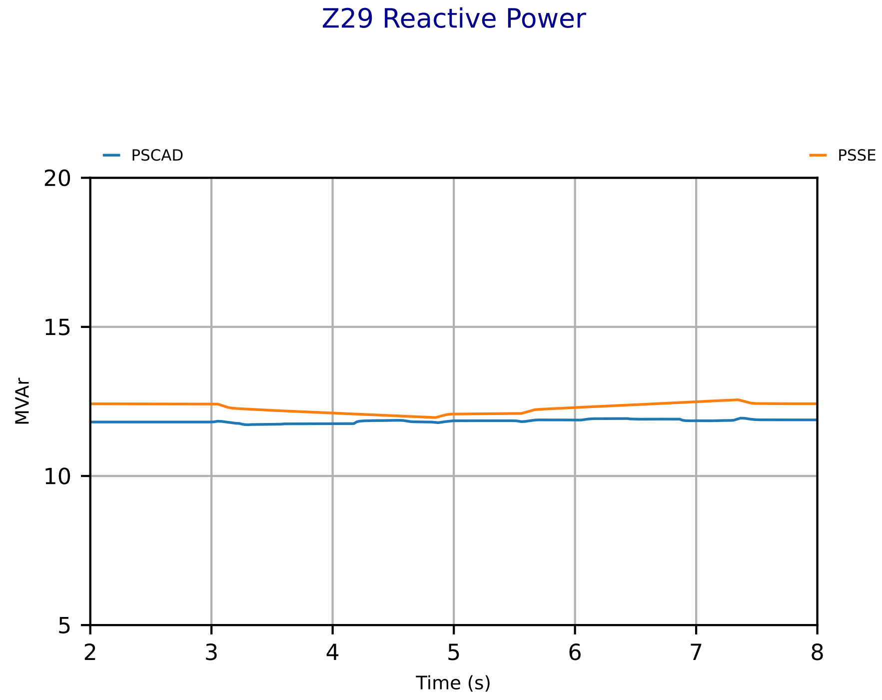


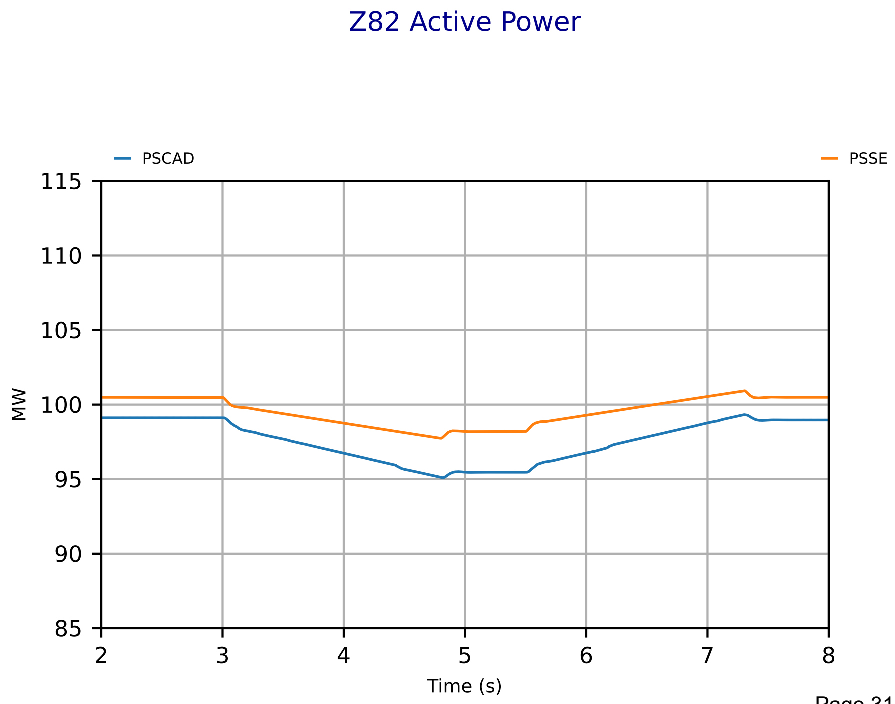
Z22 Reactive Power

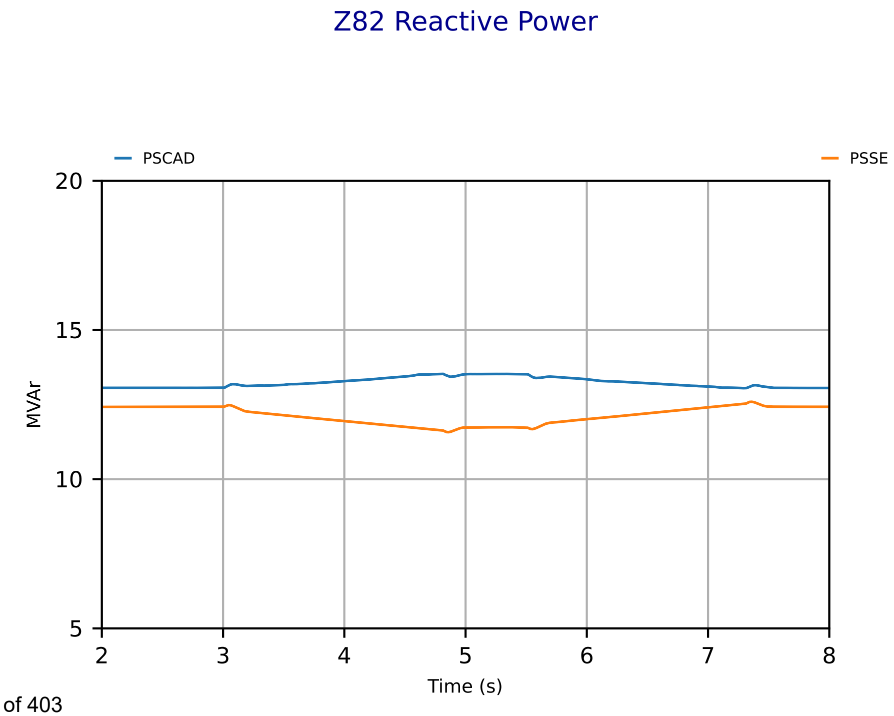


CMLD_SMIB_SCR_3_XR_14_T9_3

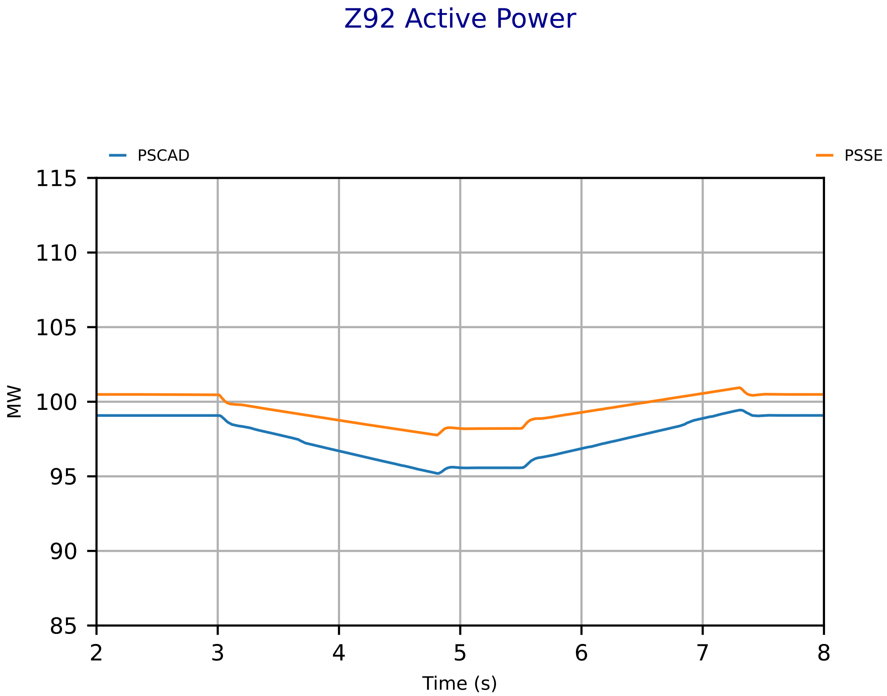


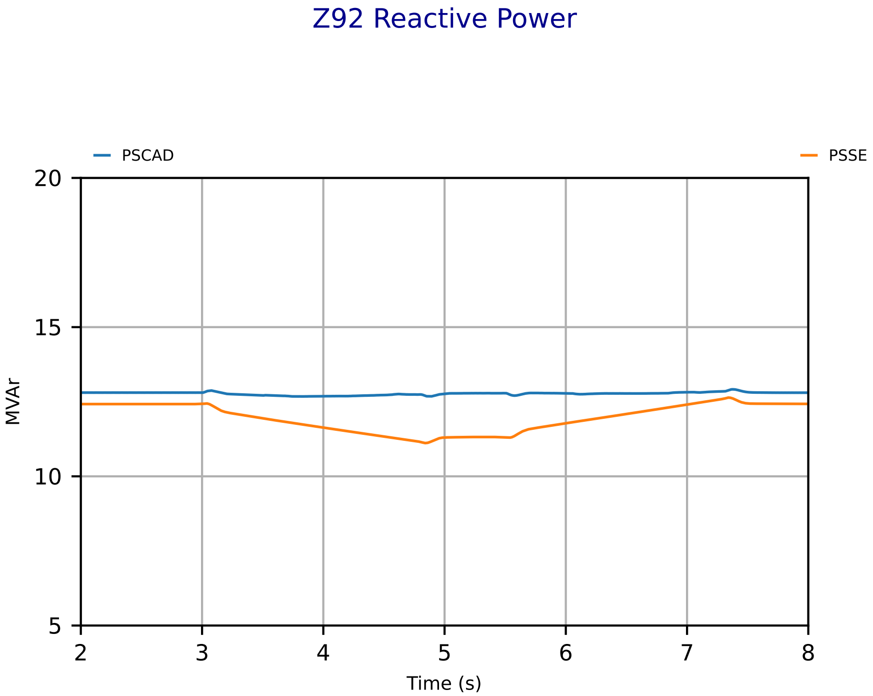


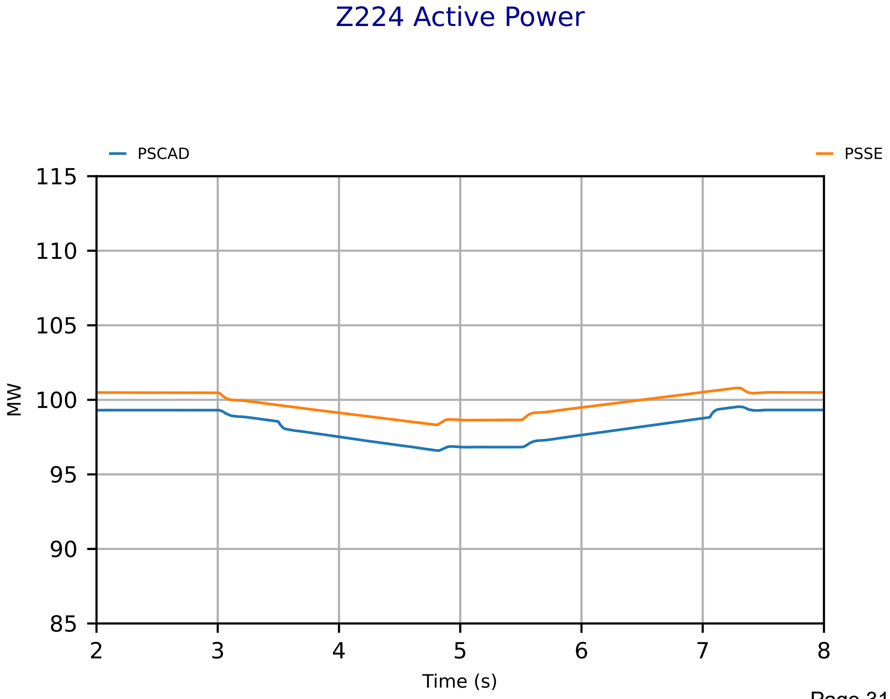


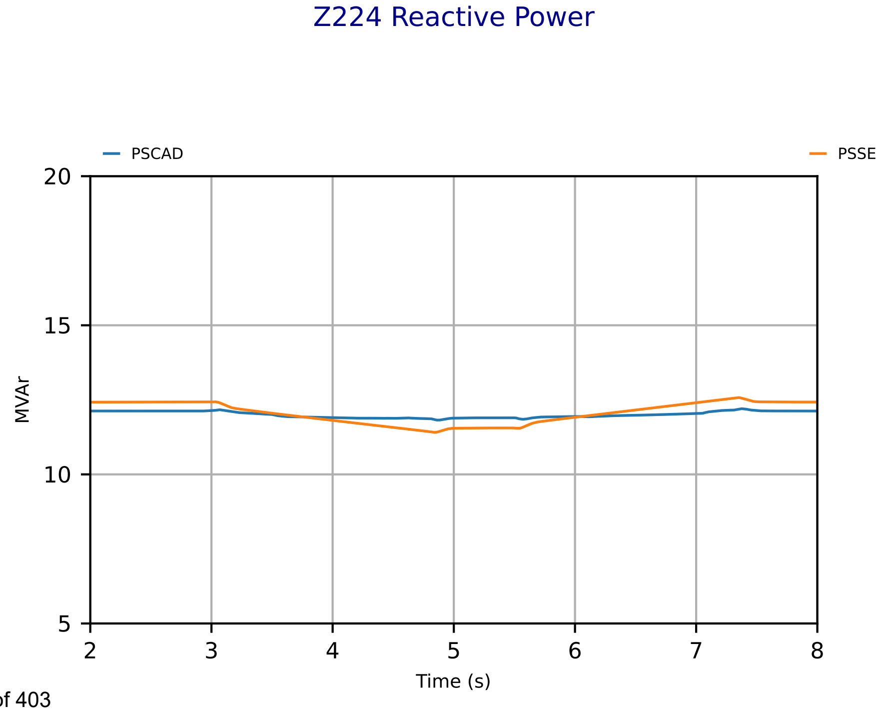


CMLD_SMIB_SCR_3_XR_14_T9_4









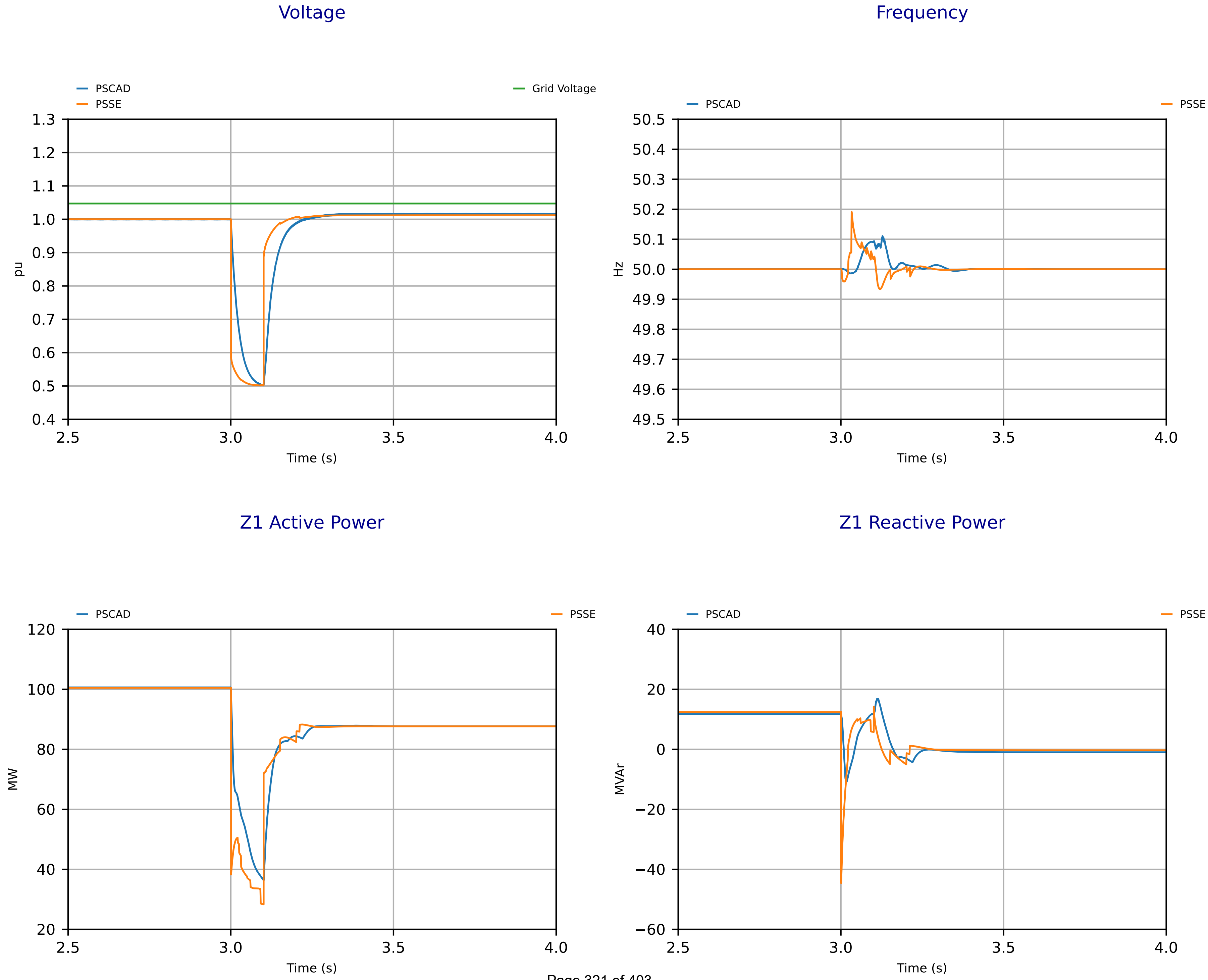
CMLD SMIB

SCR = 10, X/R = 3

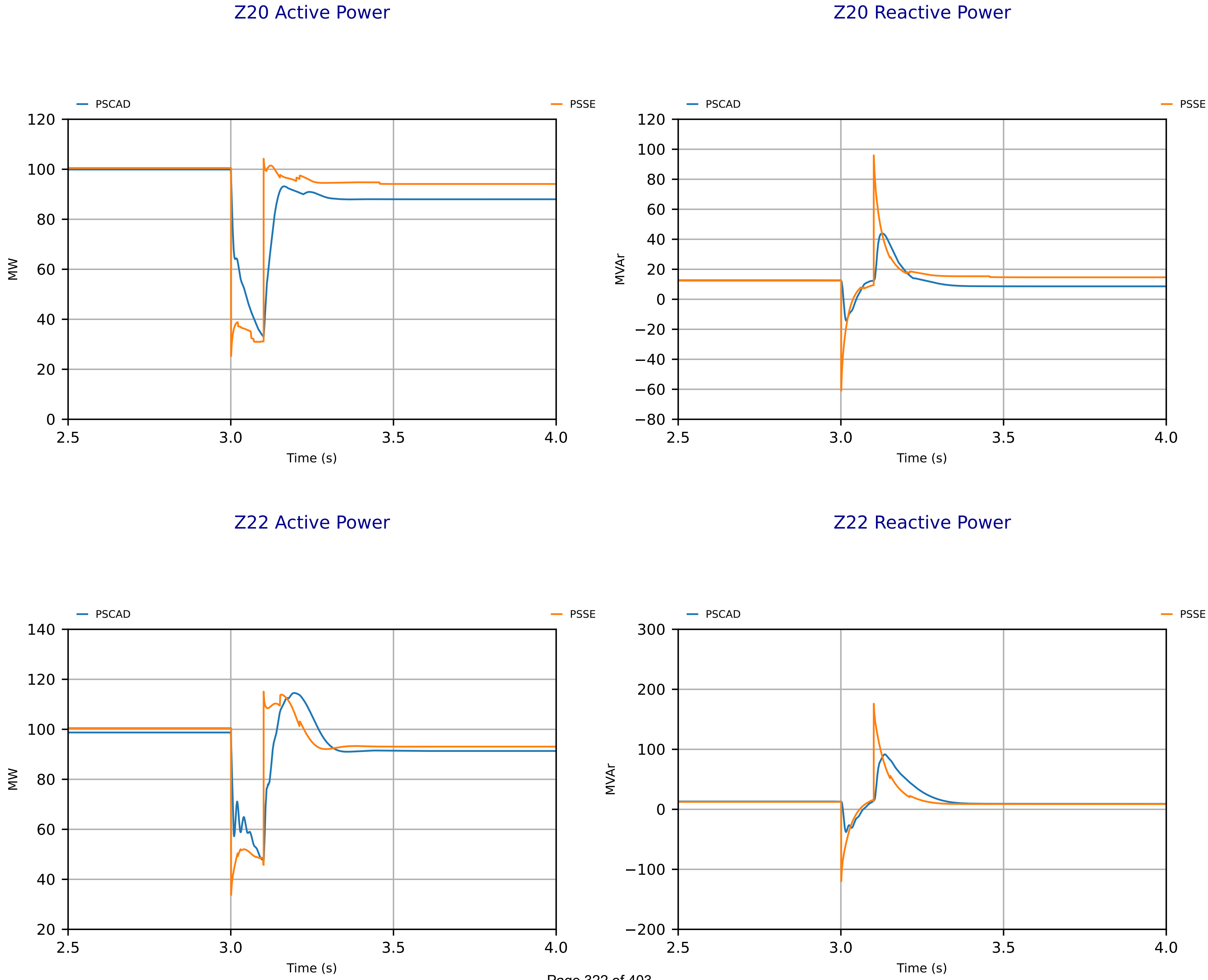
Test #2:

LLG fault for 100 ms

CMLD_SMIB_SCR_10_XR_3_T2_1

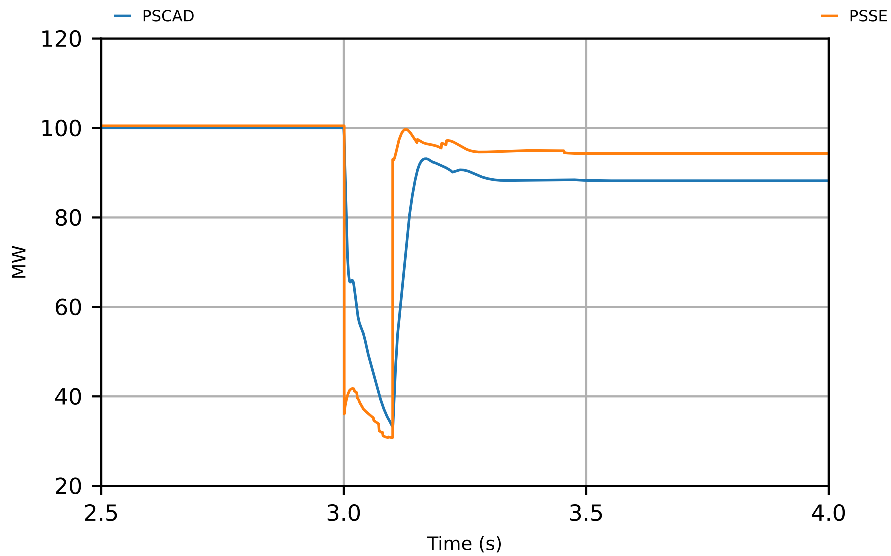


CMLD_SMIB_SCR_10_XR_3_T2_2

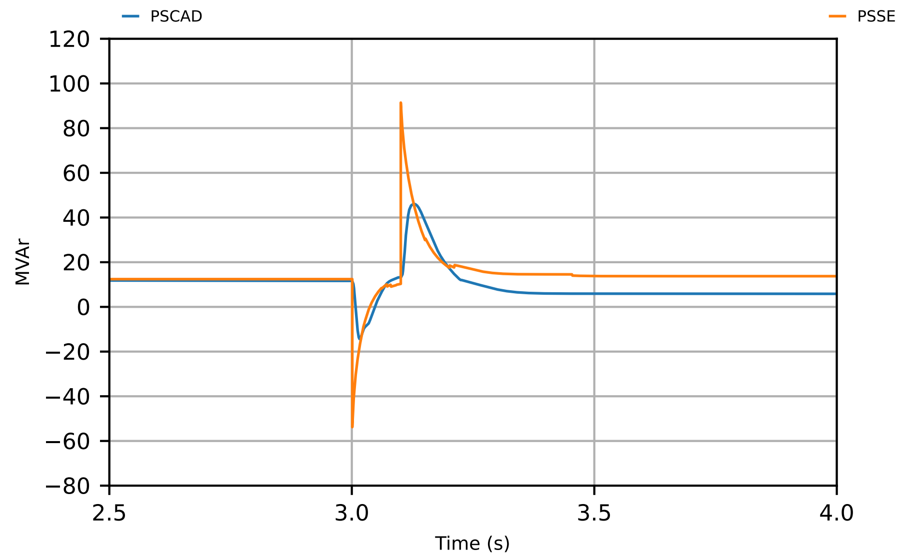


CMLD_SMIB_SCR_10_XR_3_T2_3

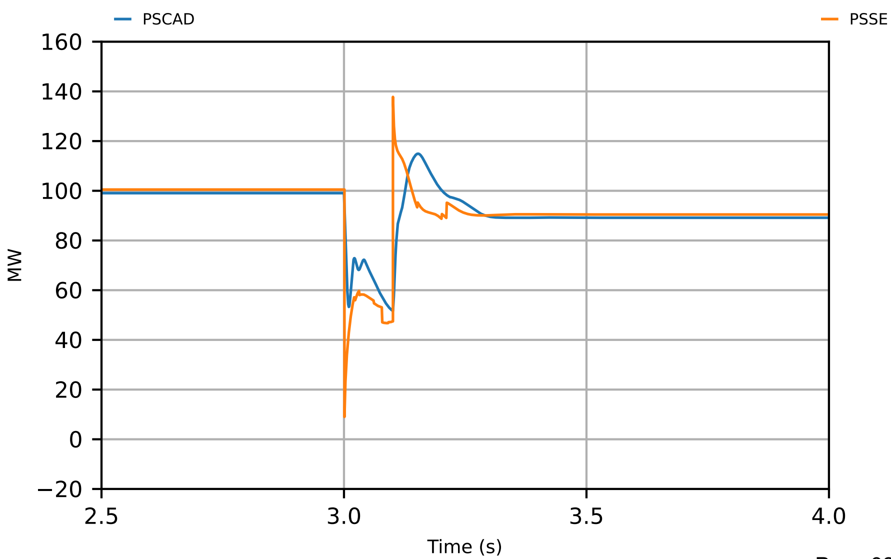
Z29 Active Power



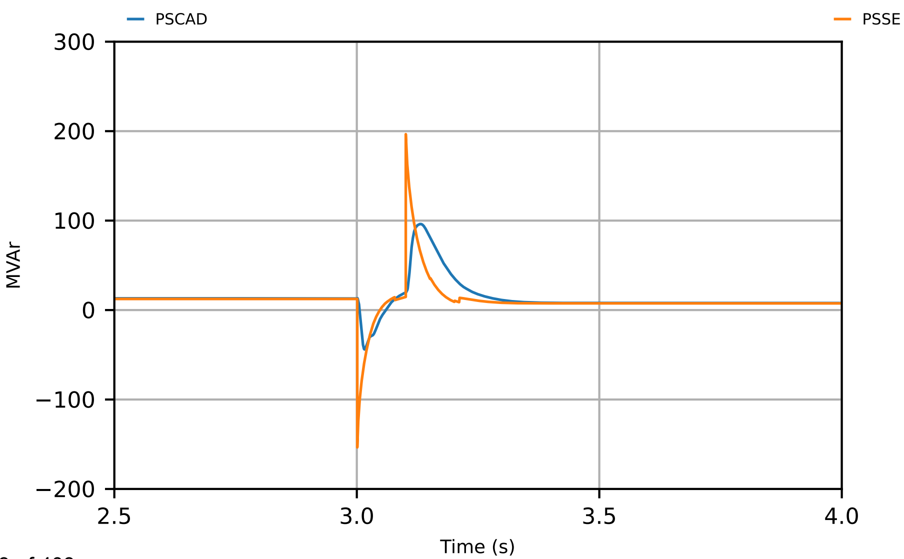
Z29 Reactive Power



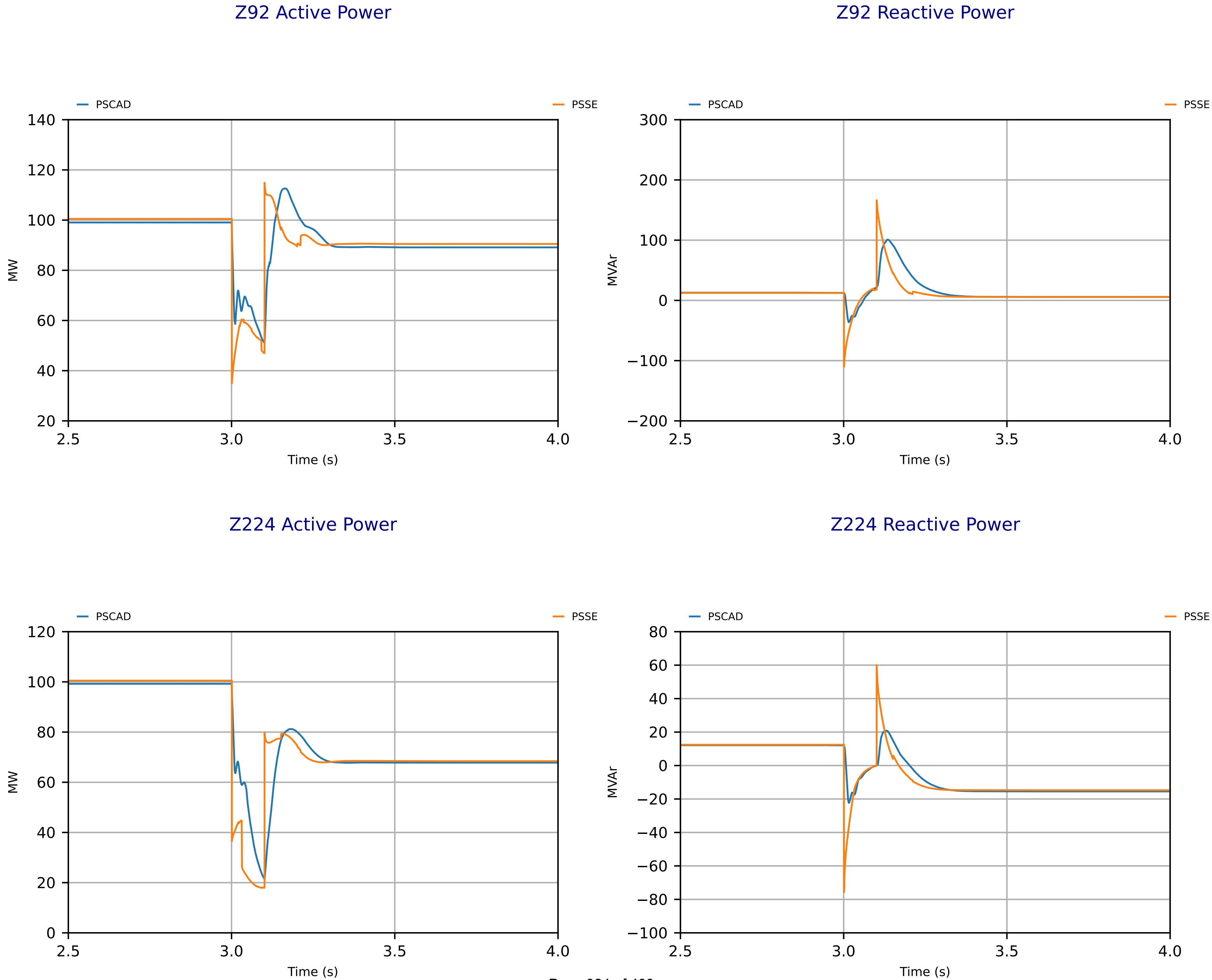
Z82 Active Power



Z82 Reactive Power



CMLD_SMIB_SCR_10_XR_3_T2_4



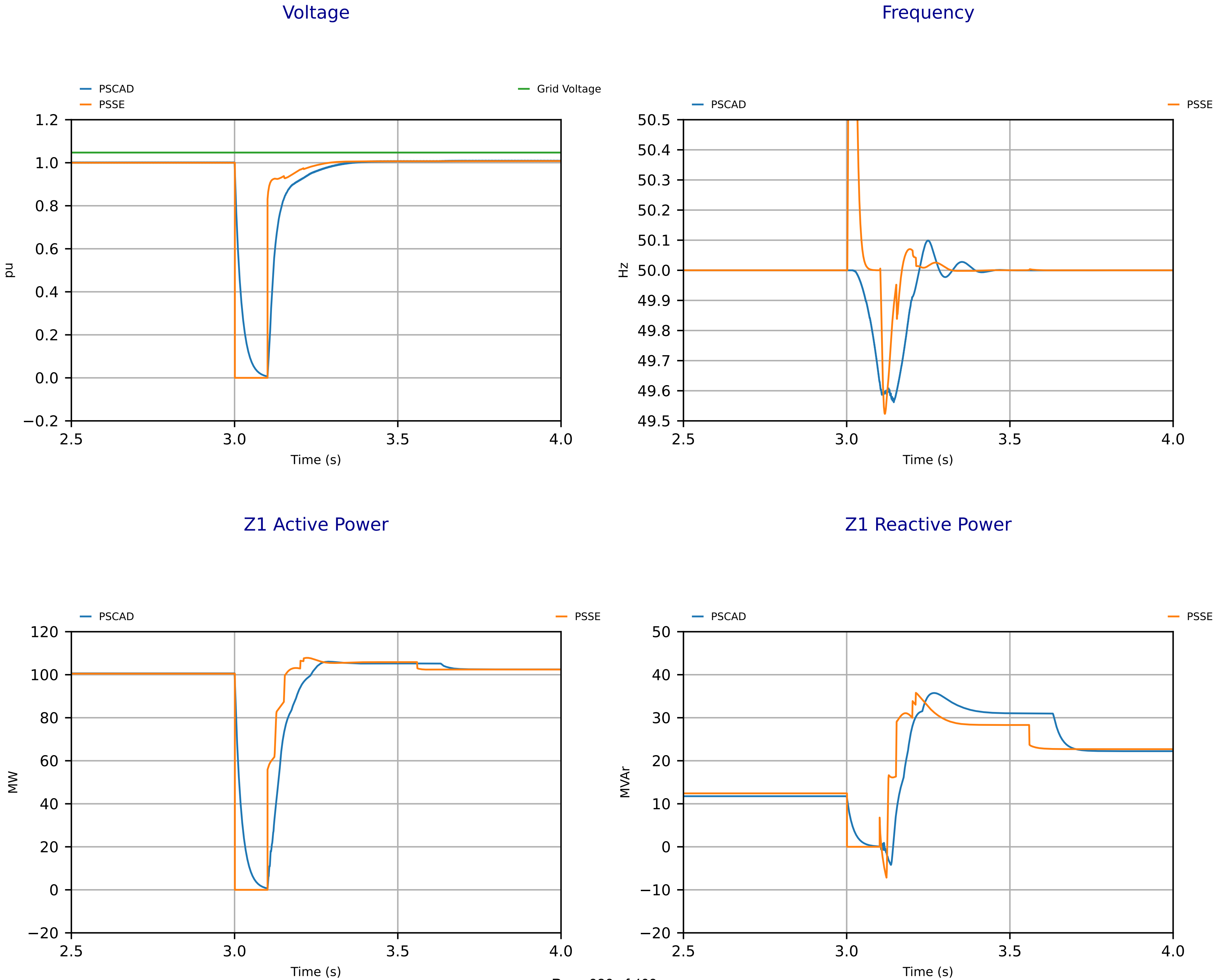
CMLD SMIB

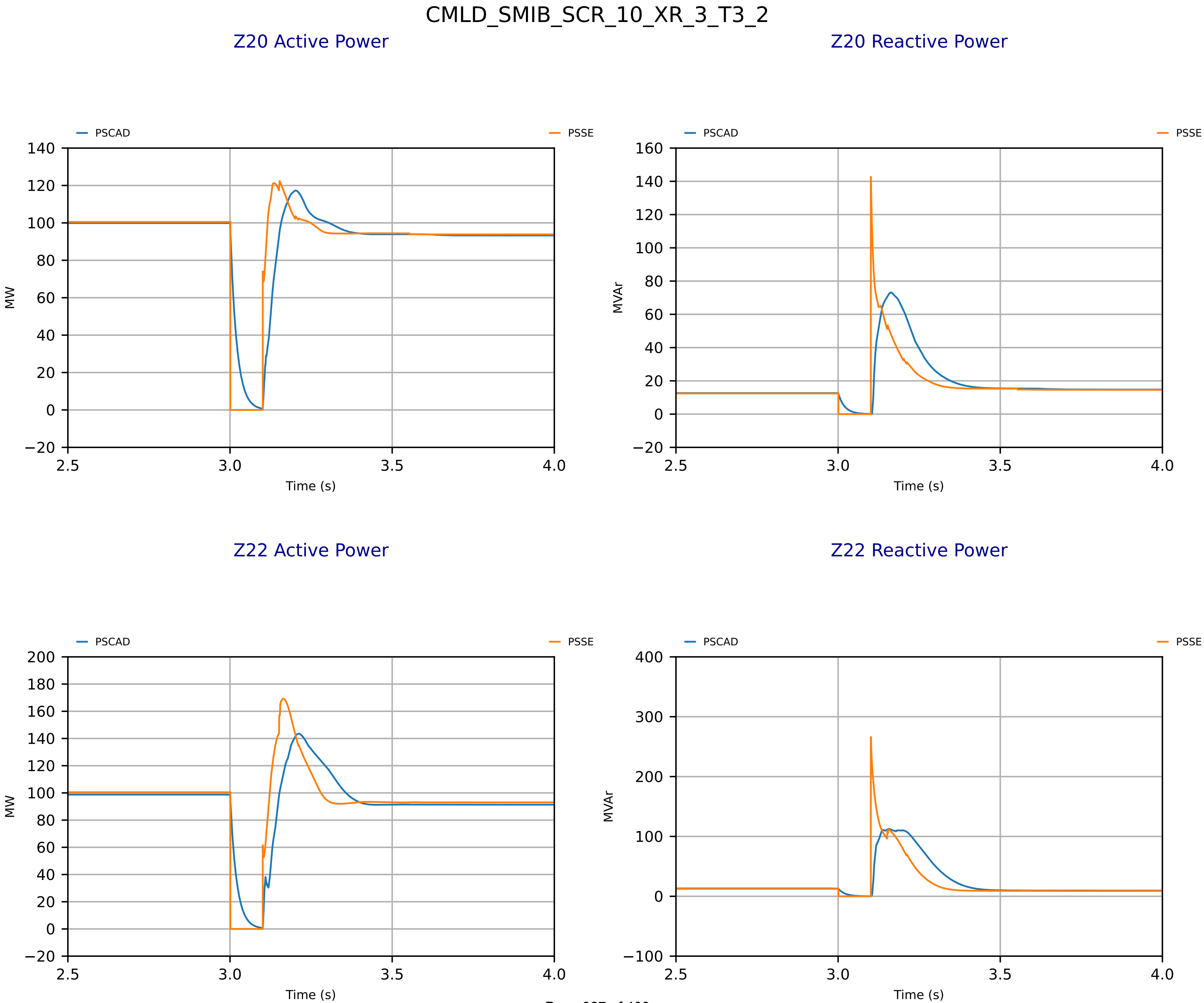
SCR = 10, X/R = 3

Test #3:

3PH-G fault for 100 ms

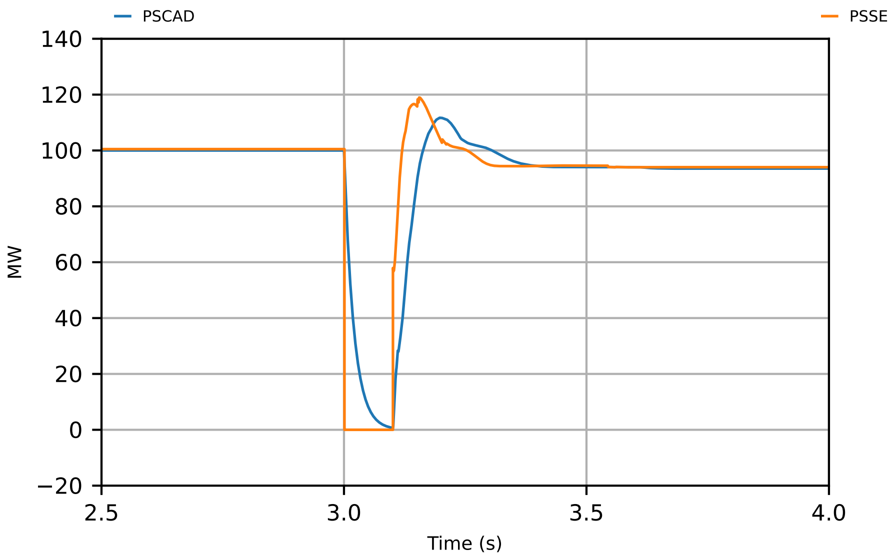
CMLD_SMIB_SCR_10_XR_3_T3_1



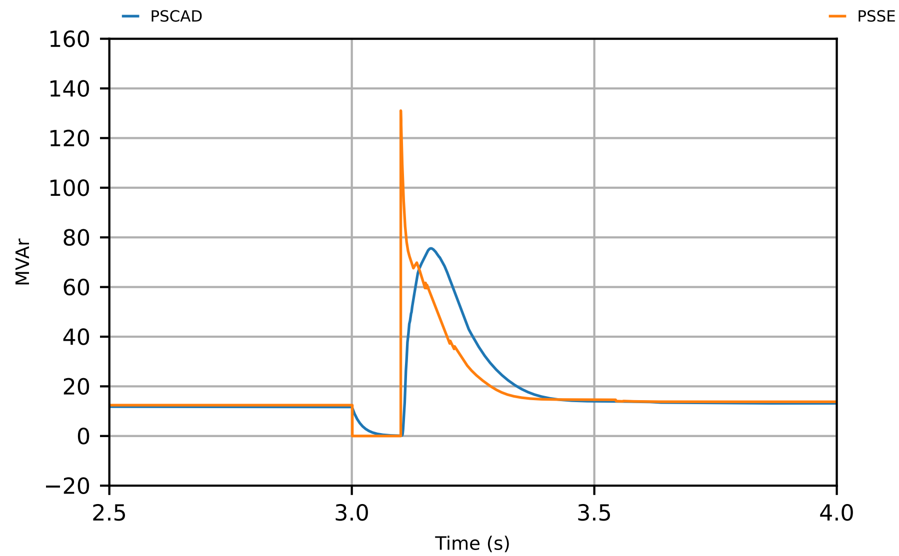

CMLD_SMIB_SCR_10_XR_3_T3_2
Z20 Active Power
PSCAD
PSSE
MW
Time (s)
Z20 Reactive Power
PSCAD
PSSE
MVAr
Time (s)
Z22 Active Power
PSCAD
PSSE
MW
Time (s)
Z22 Reactive Power
PSCAD
PSSE
MVAr
Time (s)

CMLD_SMIB_SCR_10_XR_3_T3_3

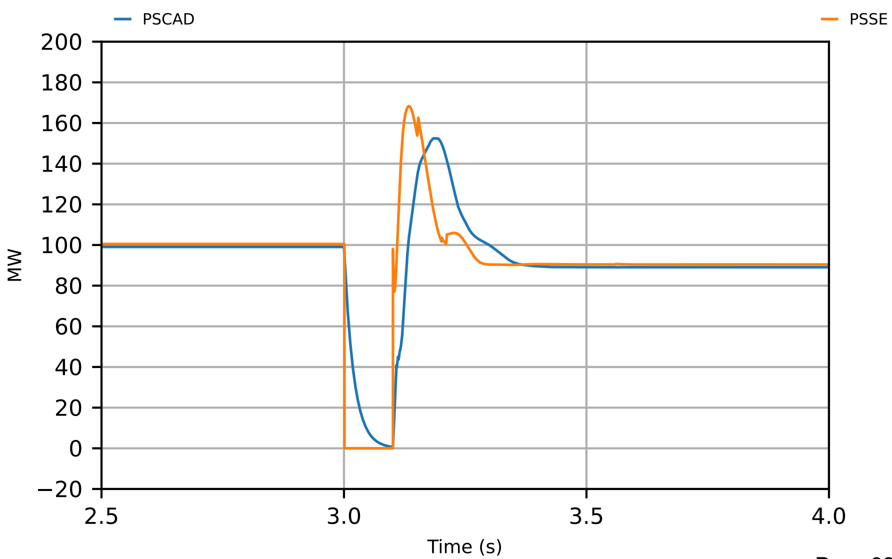
Z29 Active Power



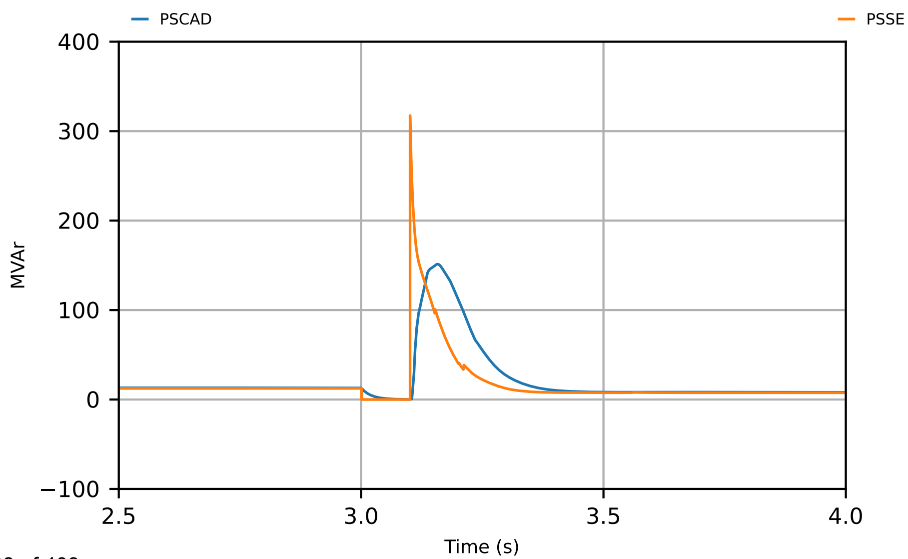
Z29 Reactive Power



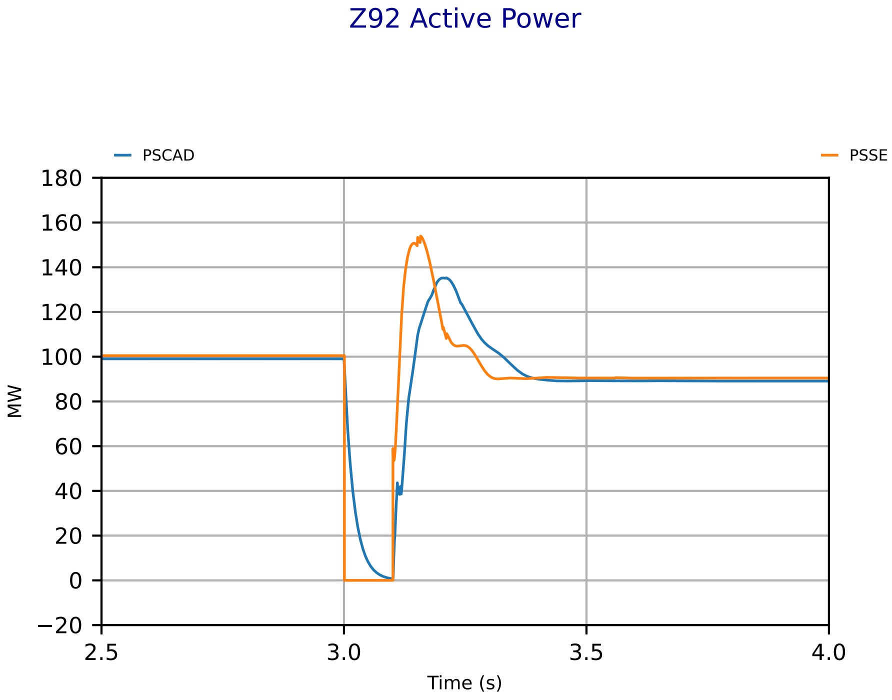
Z82 Active Power

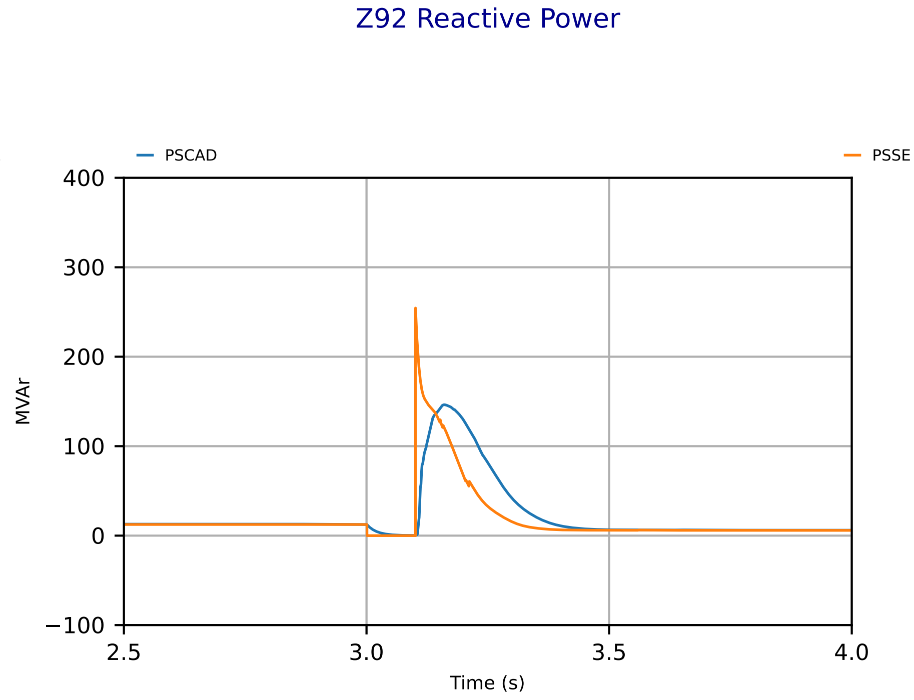


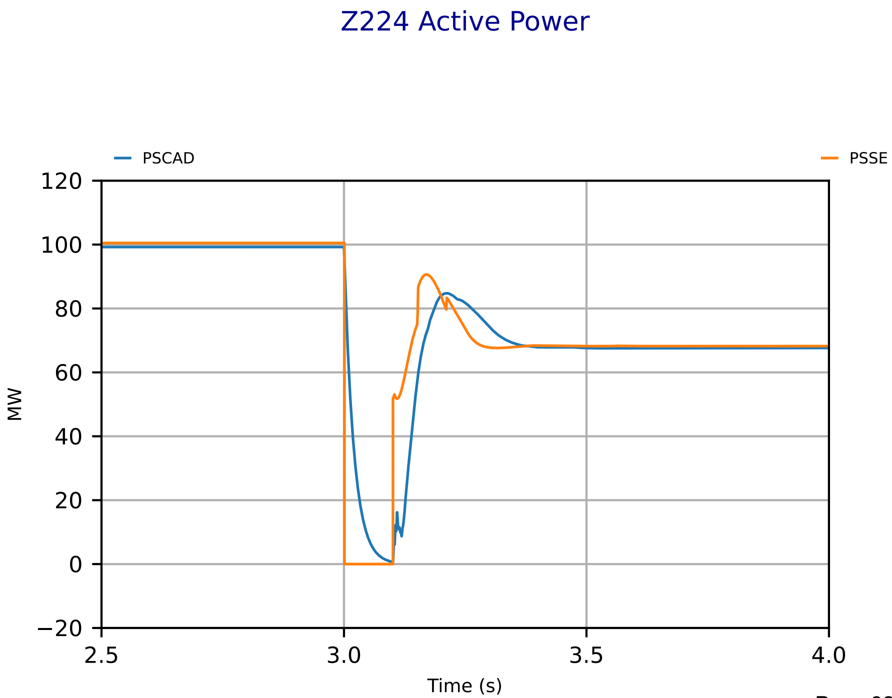
Z82 Reactive Power

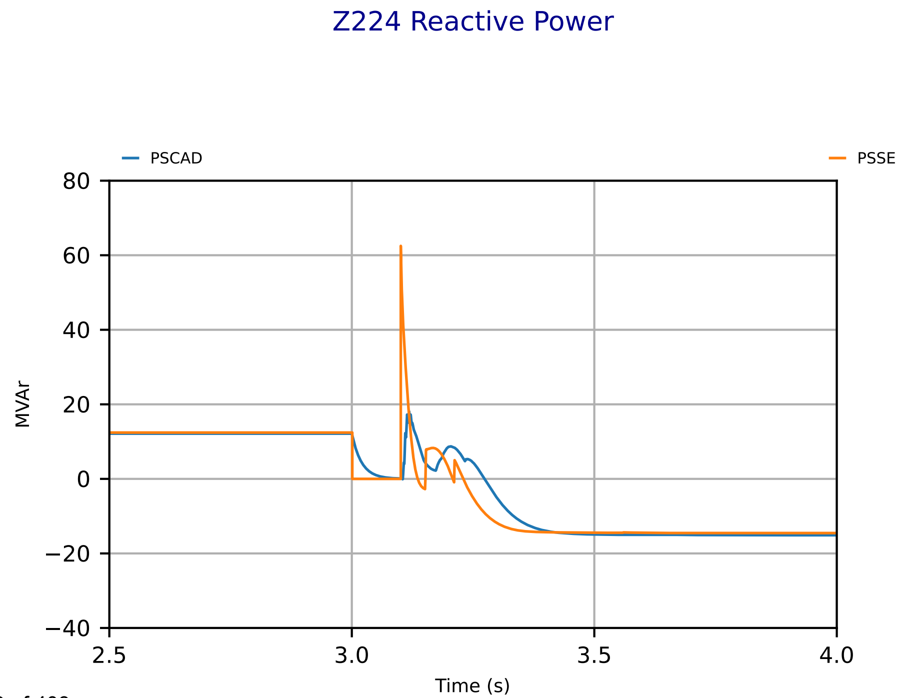


CMLD_SMIB_SCR_10_XR_3_T3_4









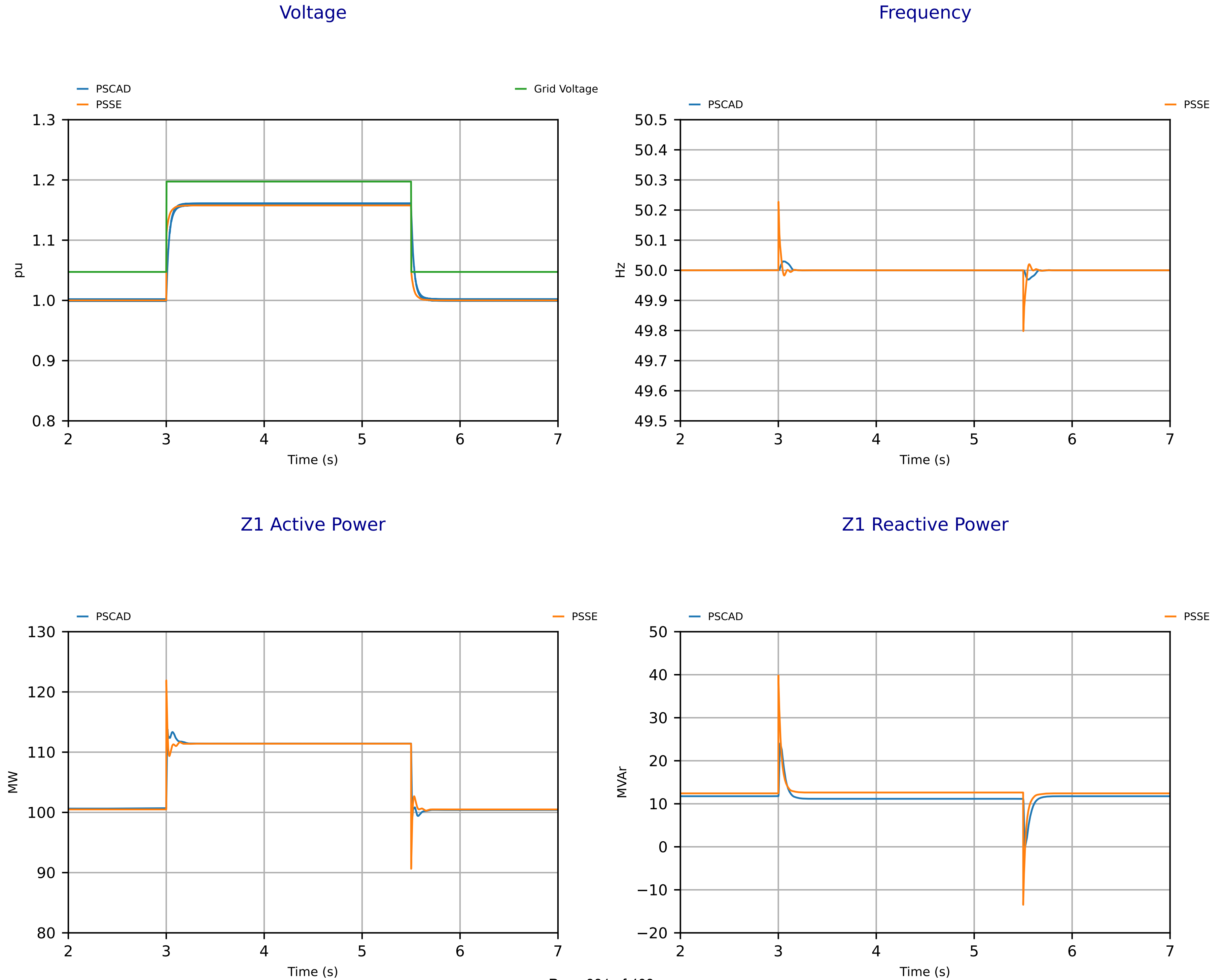
CMLD SMIB

SCR = 10, X/R = 3

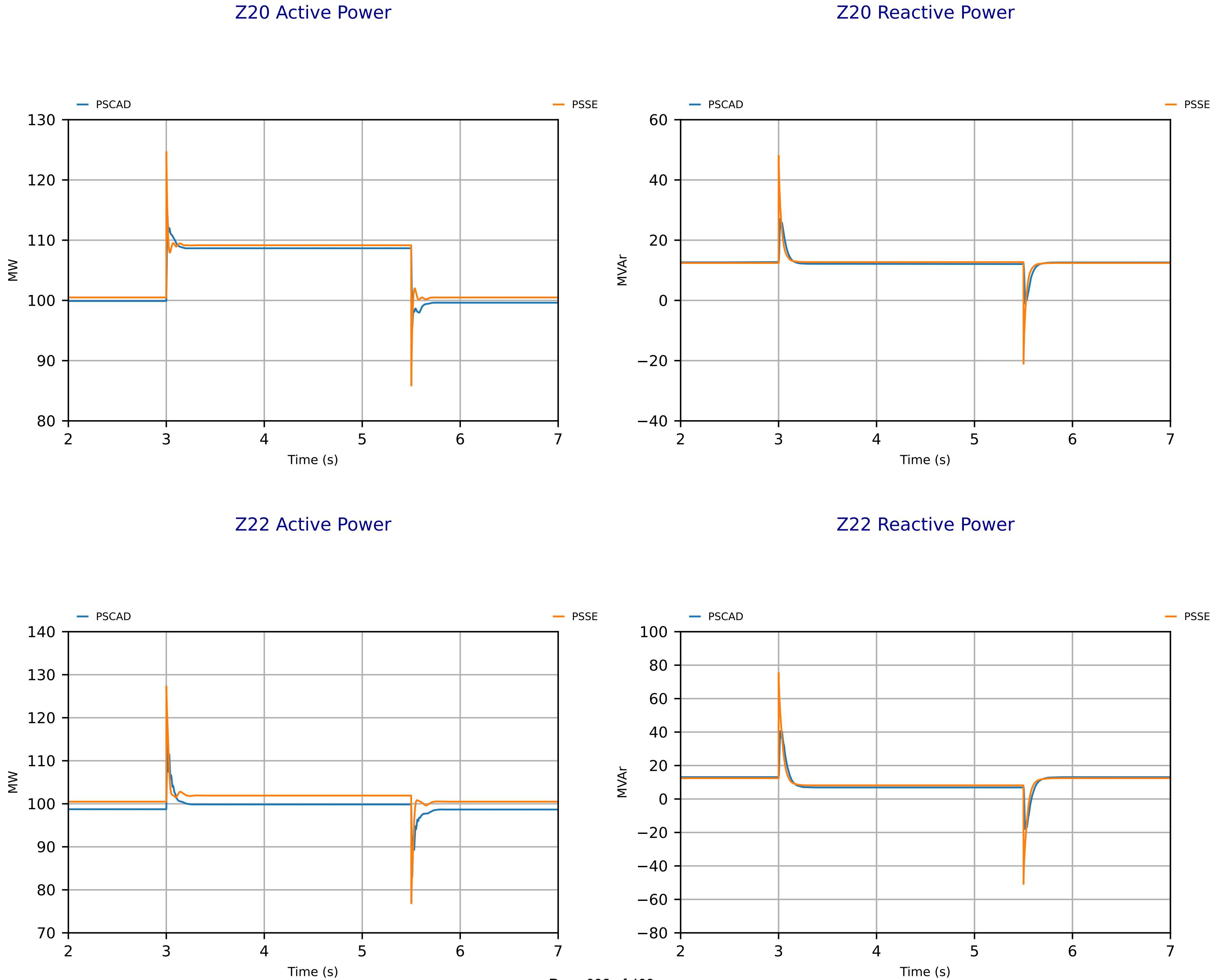
Test #4:

~115% Voltage disturbance for 2.5 s

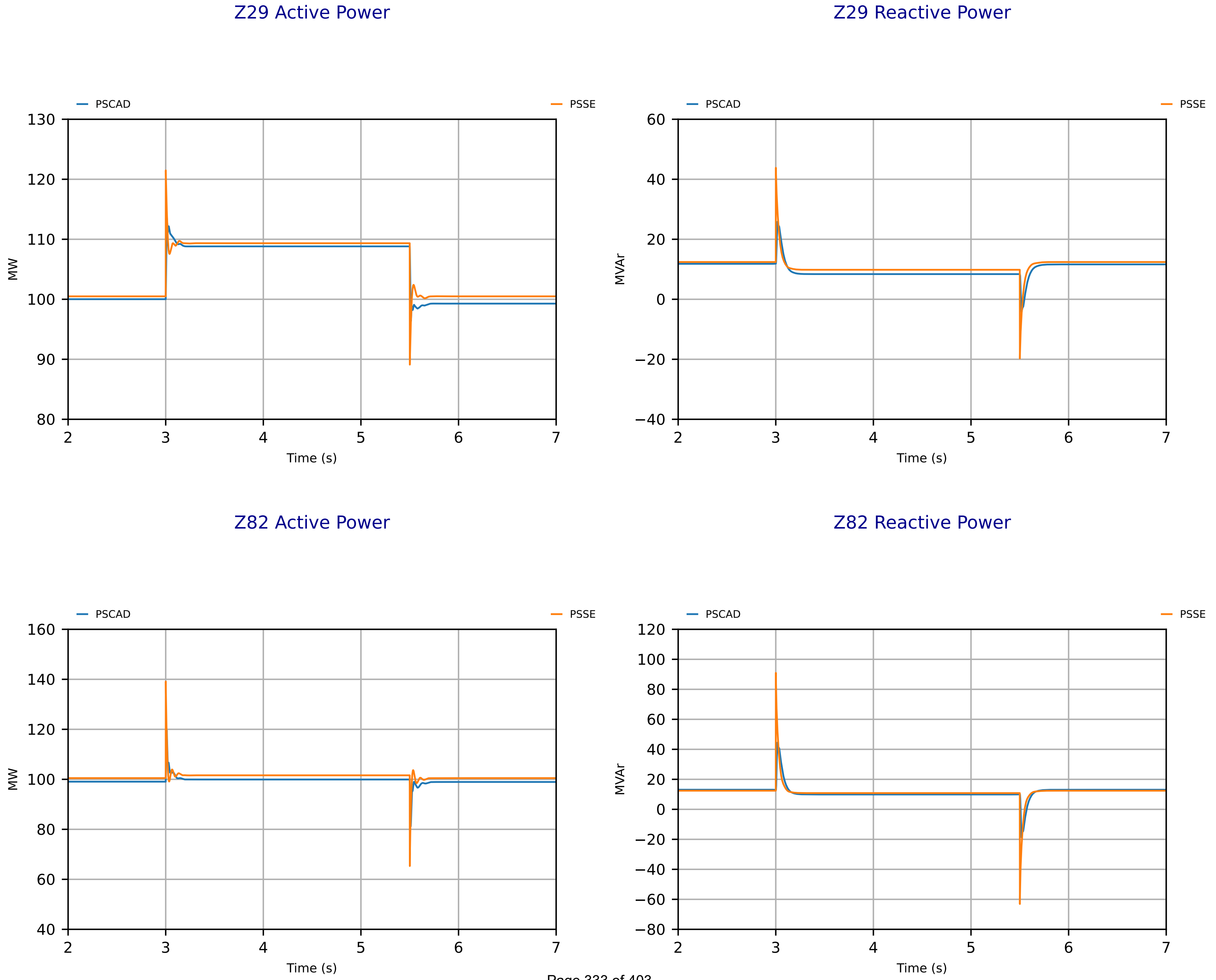
CMLD_SMIB_SCR_10_XR_3_T4_1



CMLD_SMIB_SCR_10_XR_3_T4_2

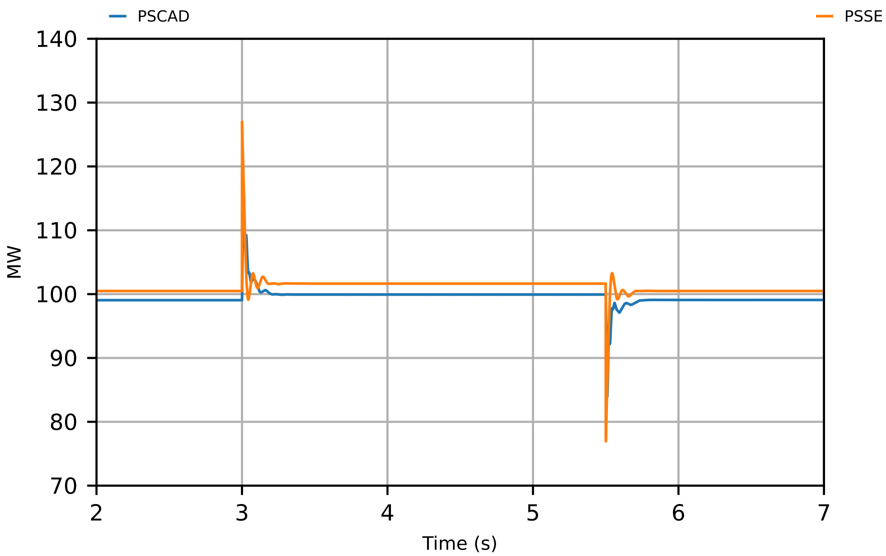


CMLD_SMIB_SCR_10_XR_3_T4_3

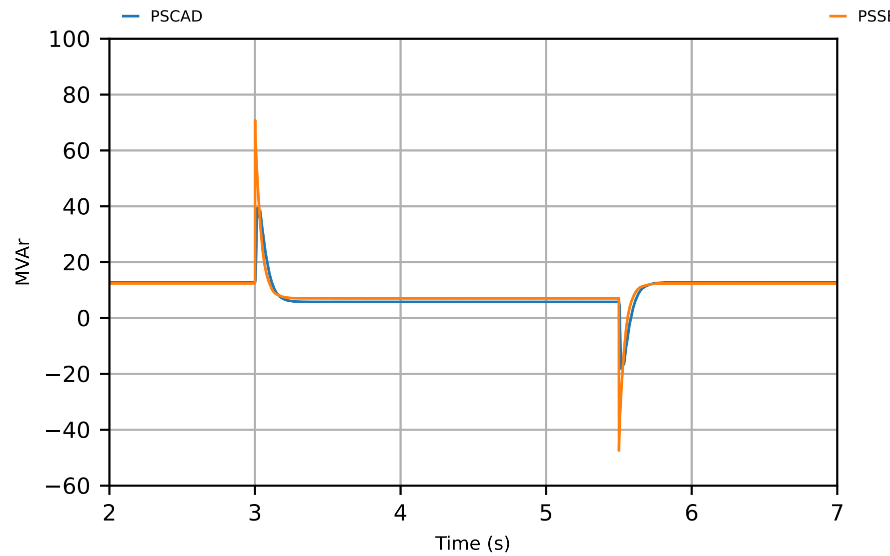


CMLD_SMIB_SCR_10_XR_3_T4_4

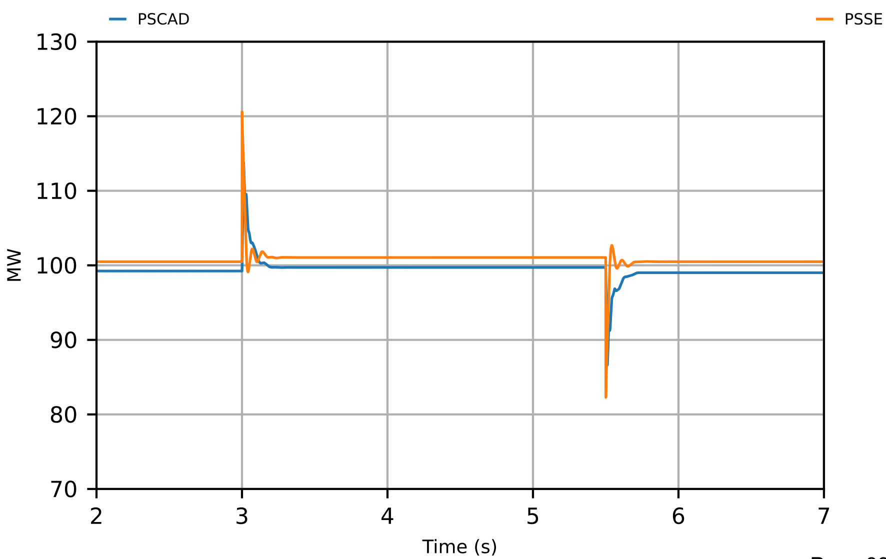
Z92 Active Power



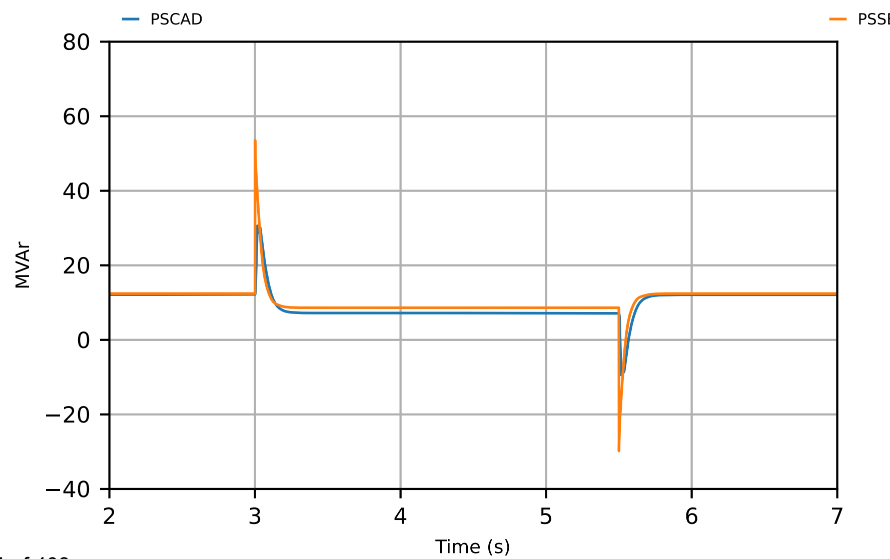
Z92 Reactive Power



Z224 Active Power



Z224 Reactive Power



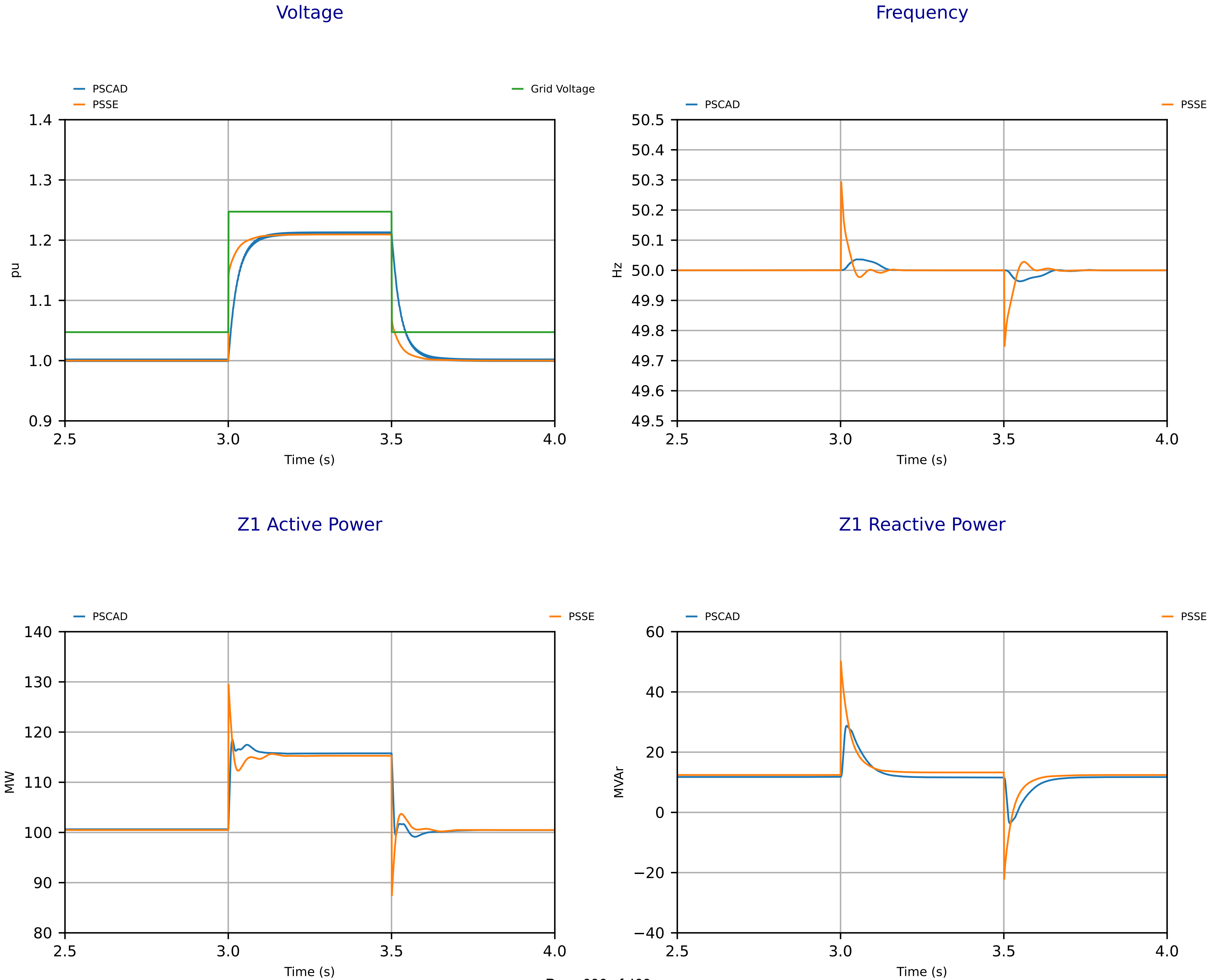
CMLD SMIB

SCR = 10, X/R = 3

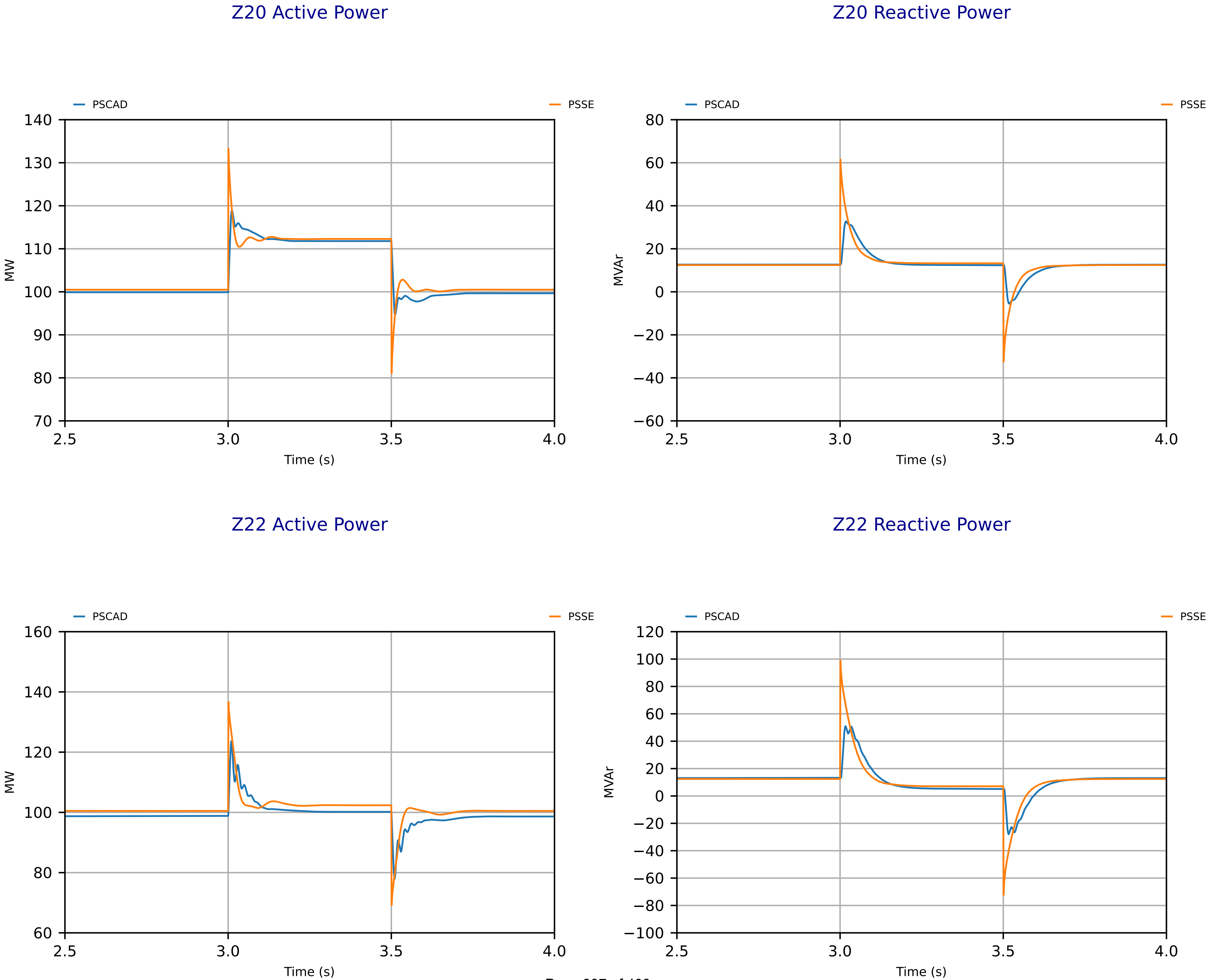
Test #5:

~120% Voltage disturbance for 500 ms

CMLD_SMIB_SCR_10_XR_3_T5_1

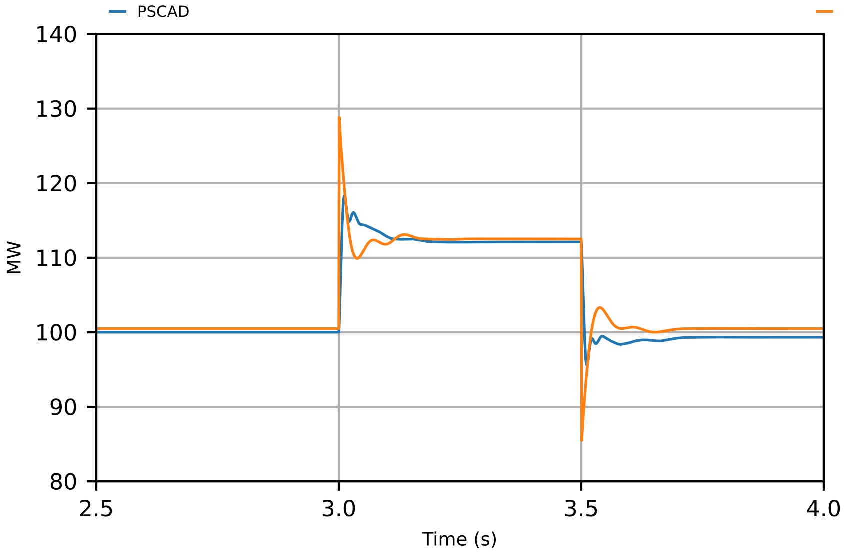


CMLD_SMIB_SCR_10_XR_3_T5_2

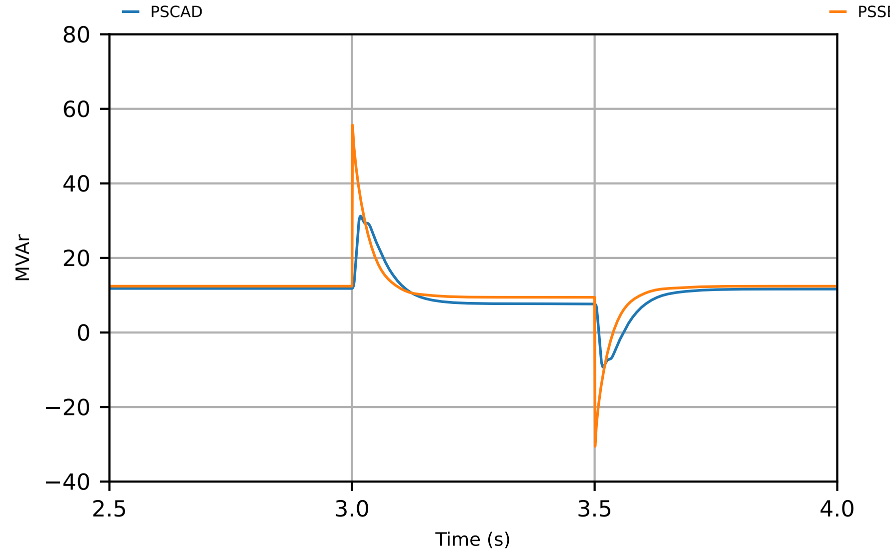


CMLD_SMIB_SCR_10_XR_3_T5_3

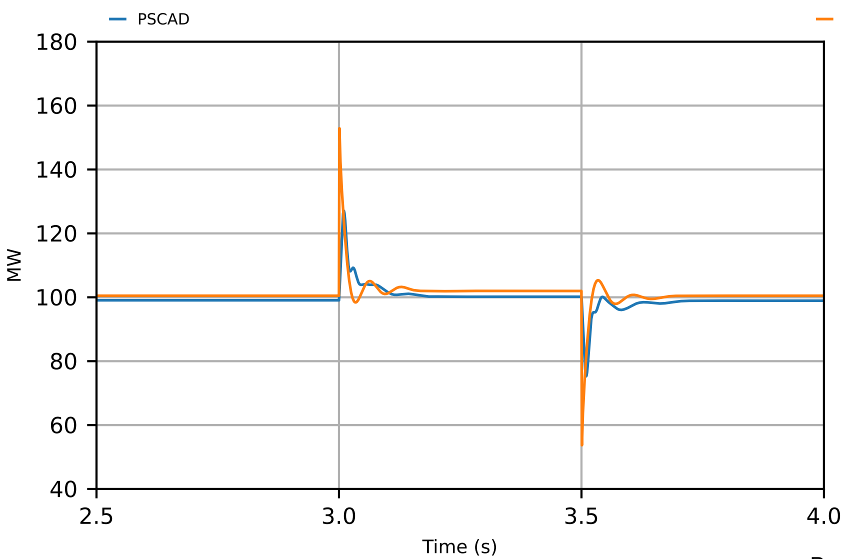
Z29 Active Power



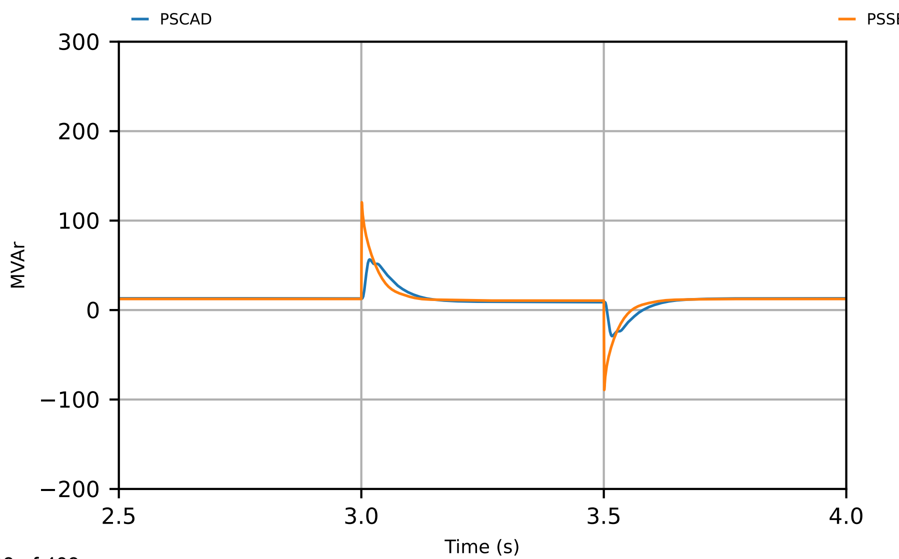
Z29 Reactive Power



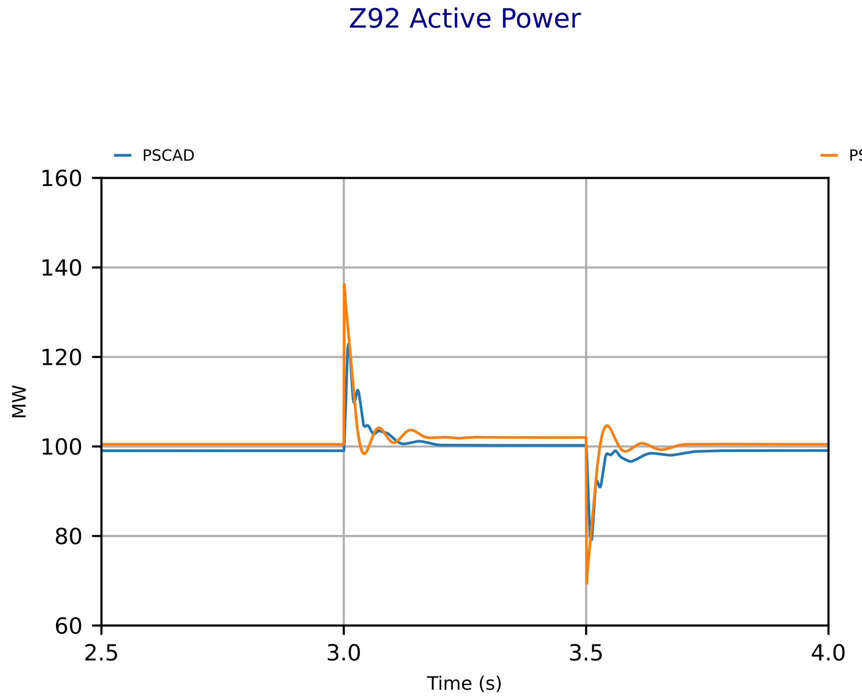
Z82 Active Power

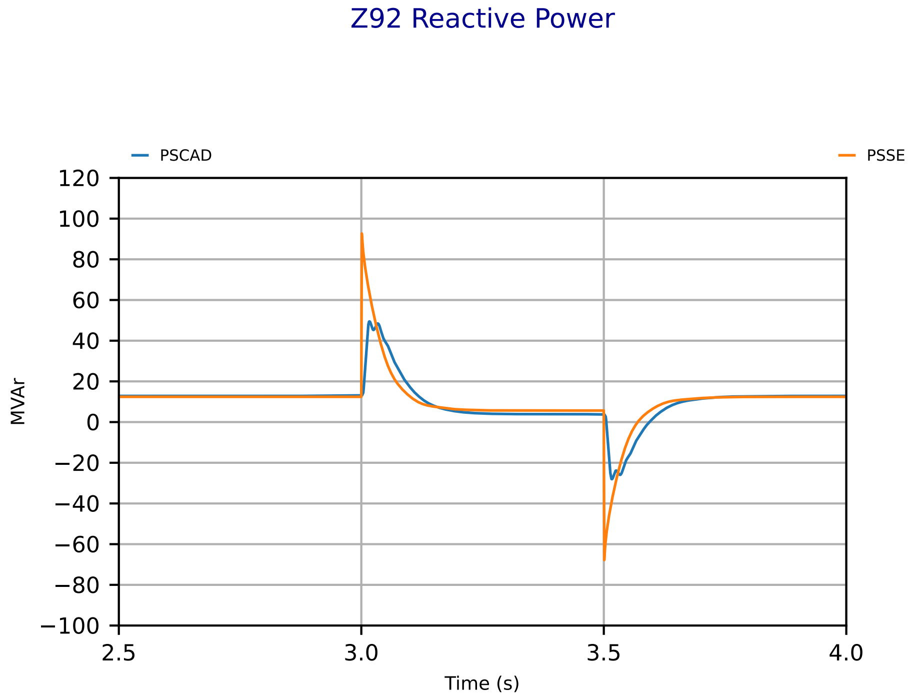


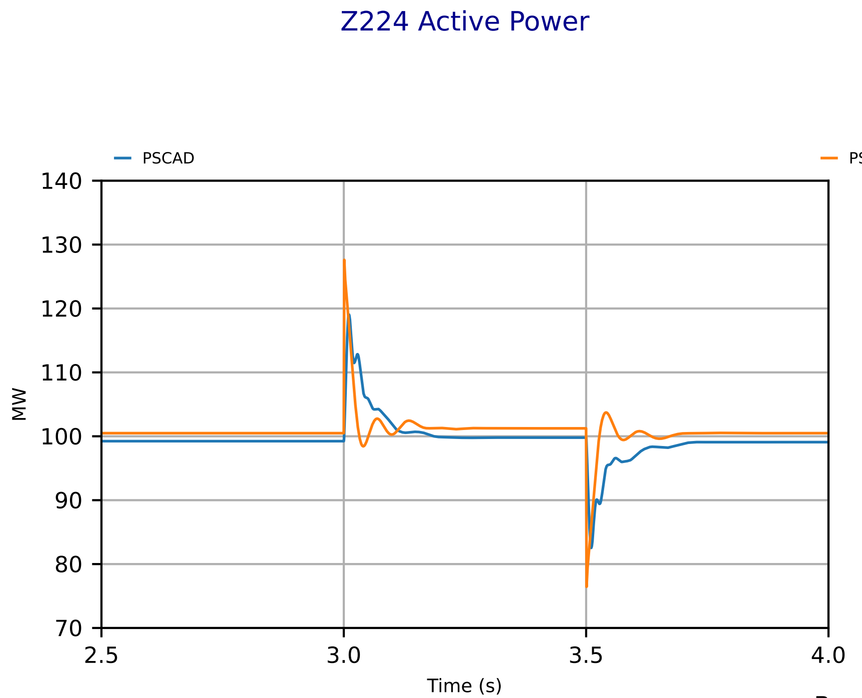
Z82 Reactive Power

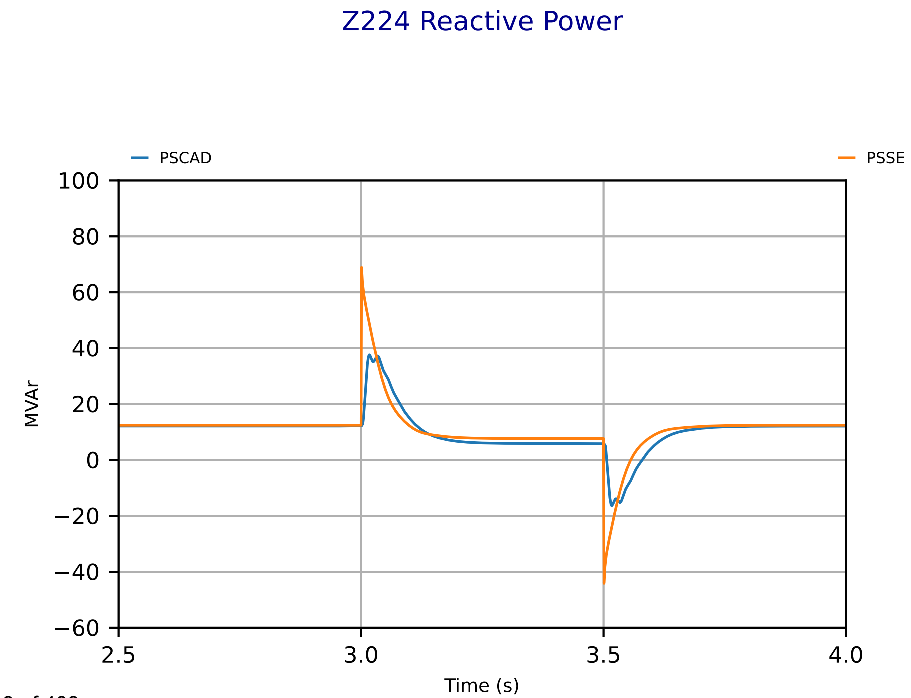


CMLD_SMIB_SCR_10_XR_3_T5_4









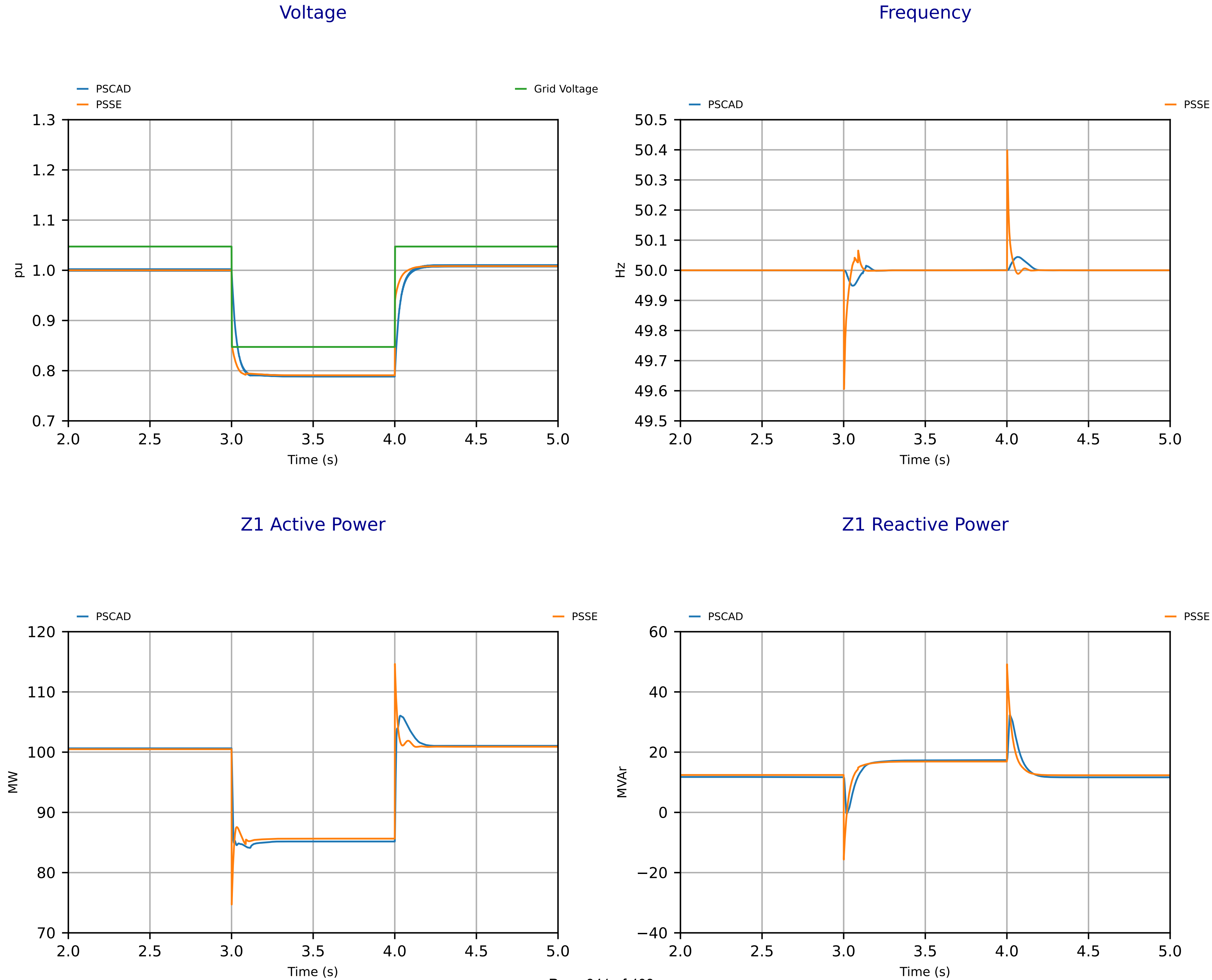
CMLD SMIB

SCR = 10, X/R = 3

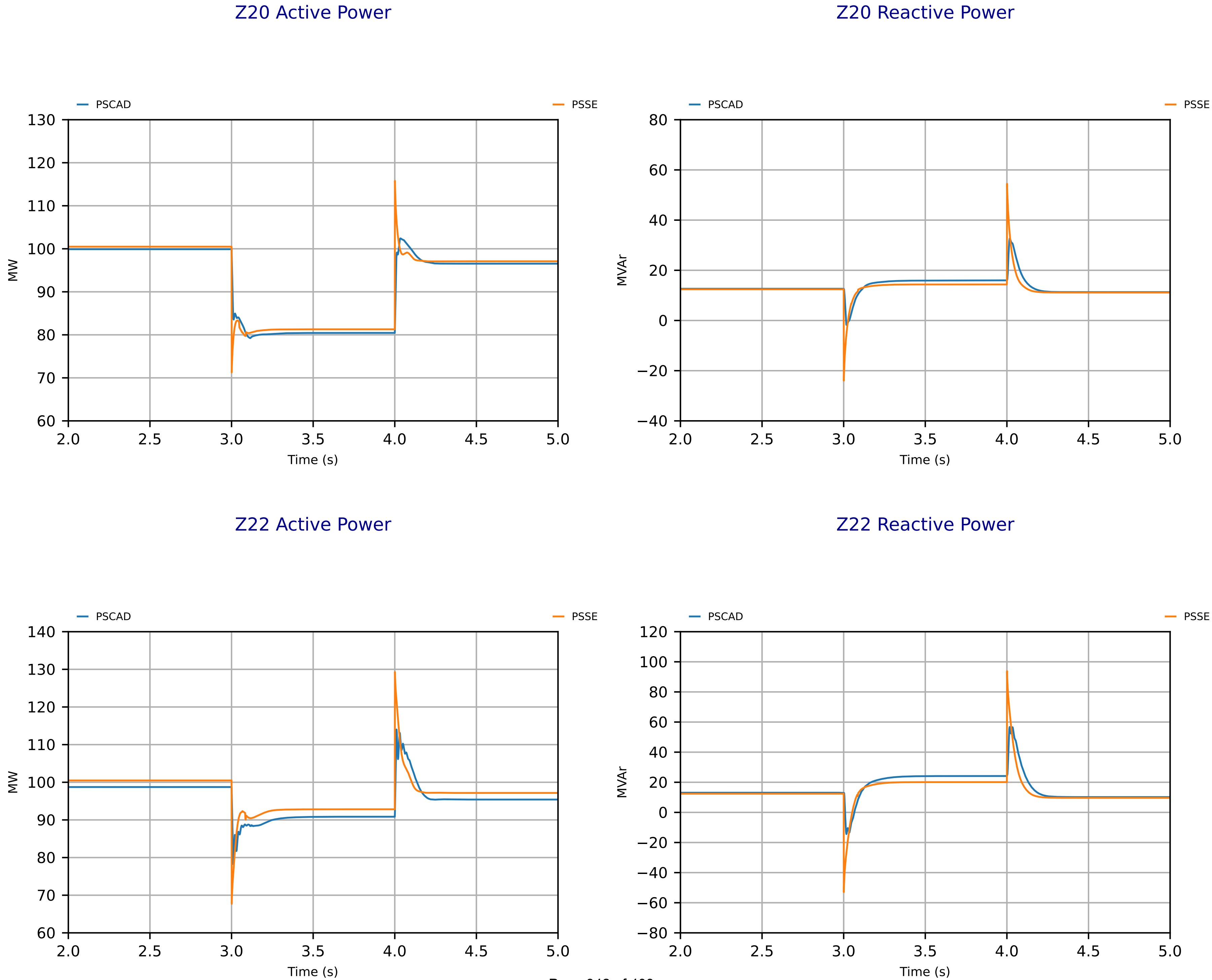
Test #6:

~80% Voltage disturbance for 1 sec

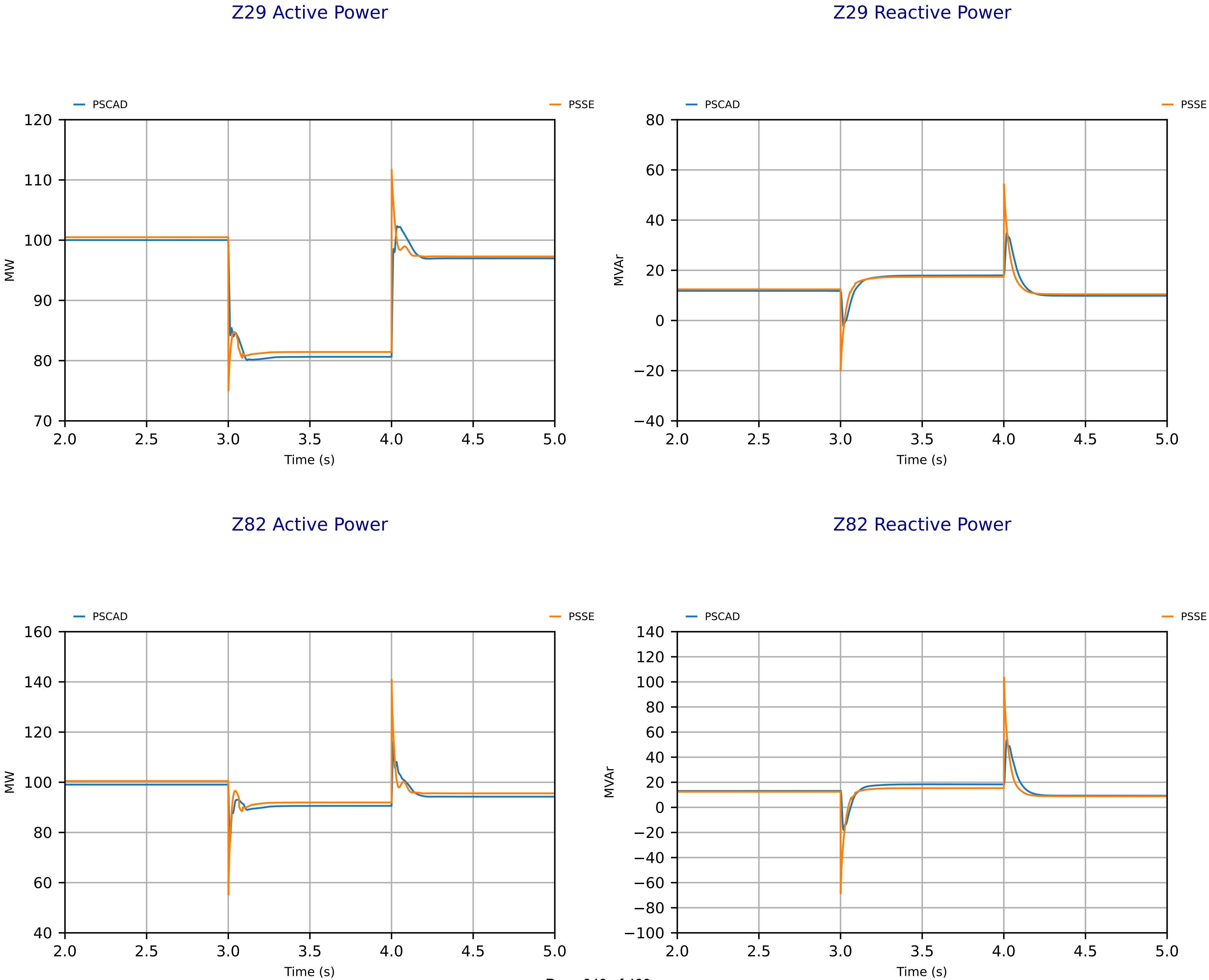
CMLD_SMIB_SCR_10_XR_3_T6_1



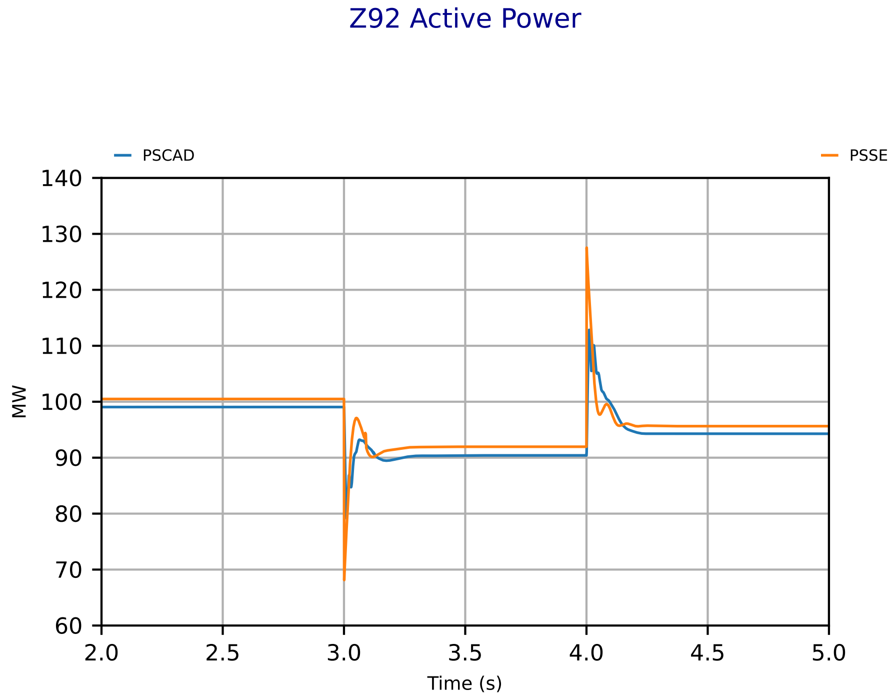
CMLD_SMIB_SCR_10_XR_3_T6_2

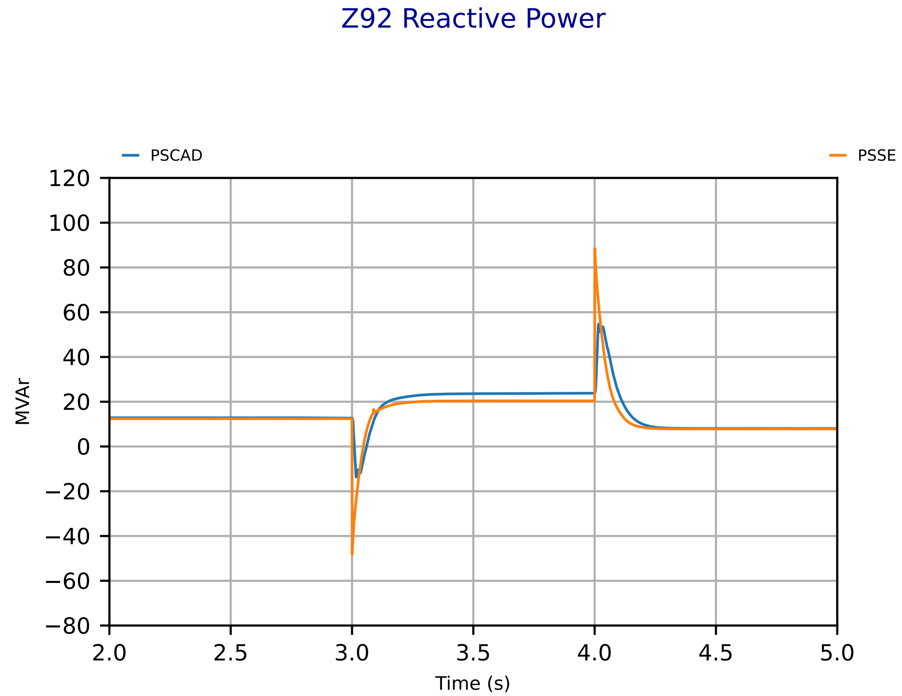


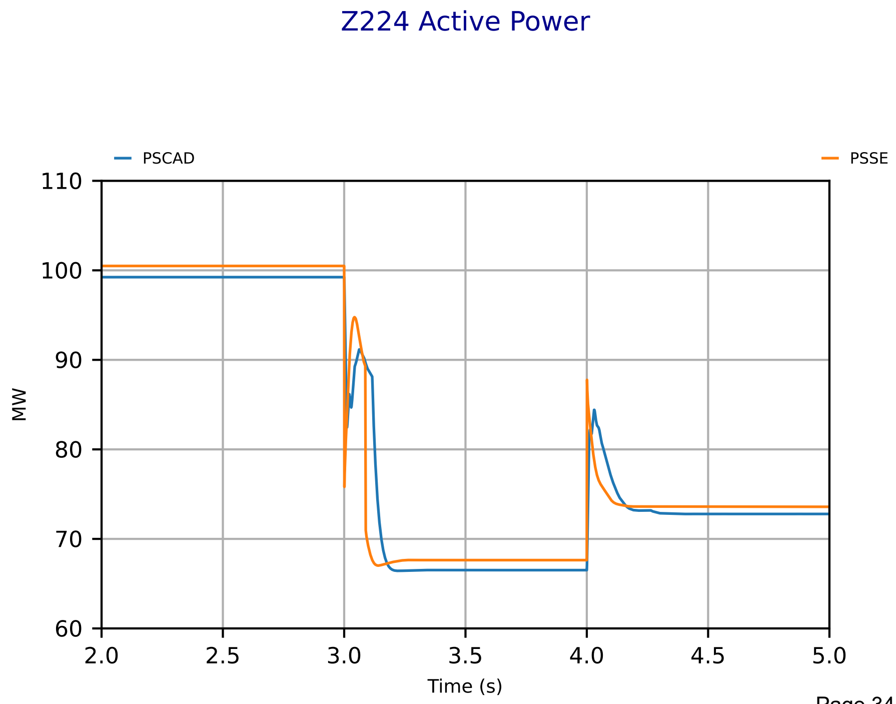
CMLD_SMIB_SCR_10_XR_3_T6_3

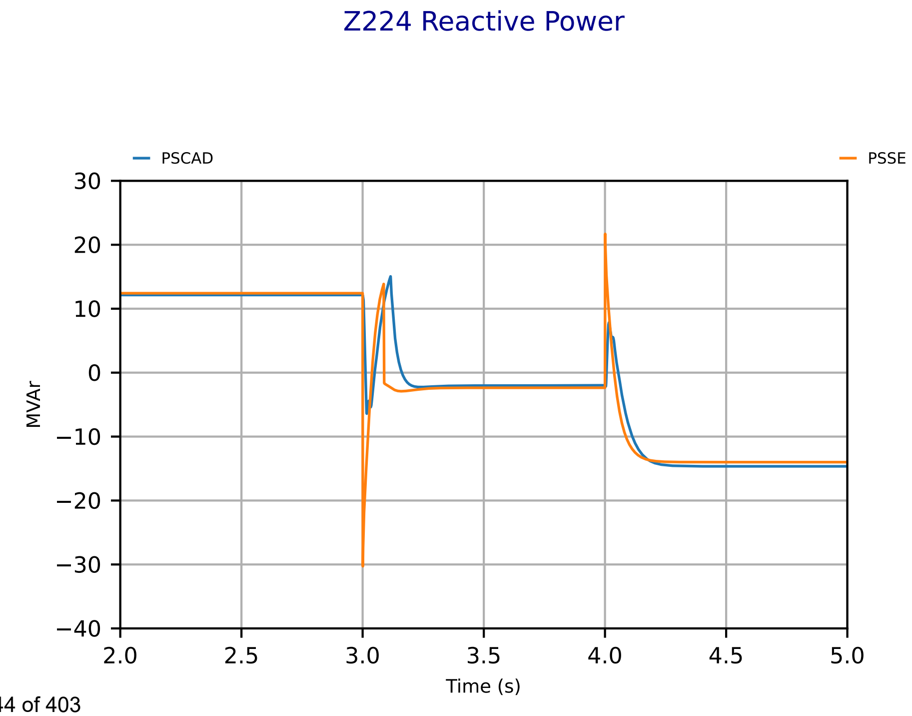


CMLD_SMIB_SCR_10_XR_3_T6_4









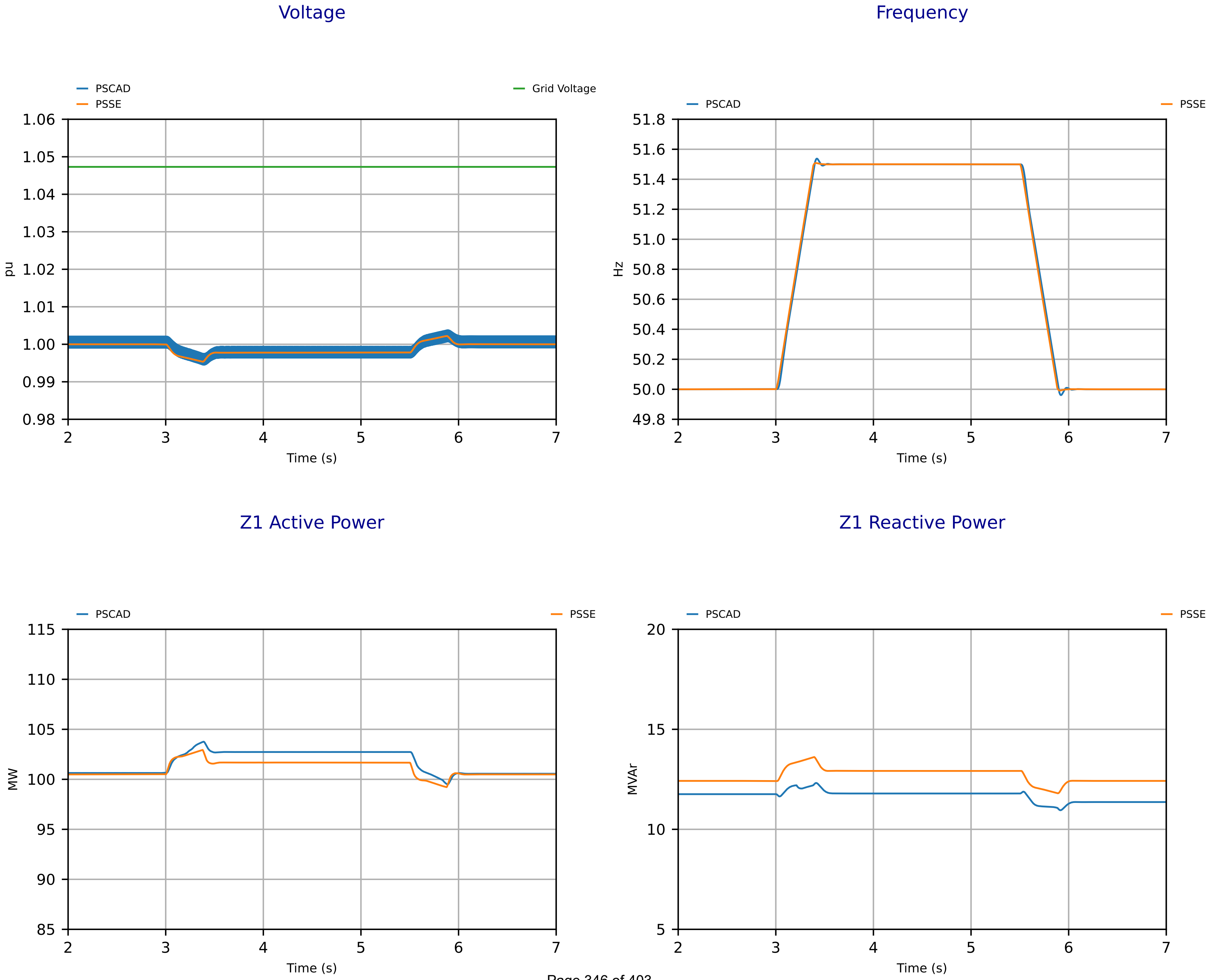
CMLD SMIB

SCR = 10, X/R = 3

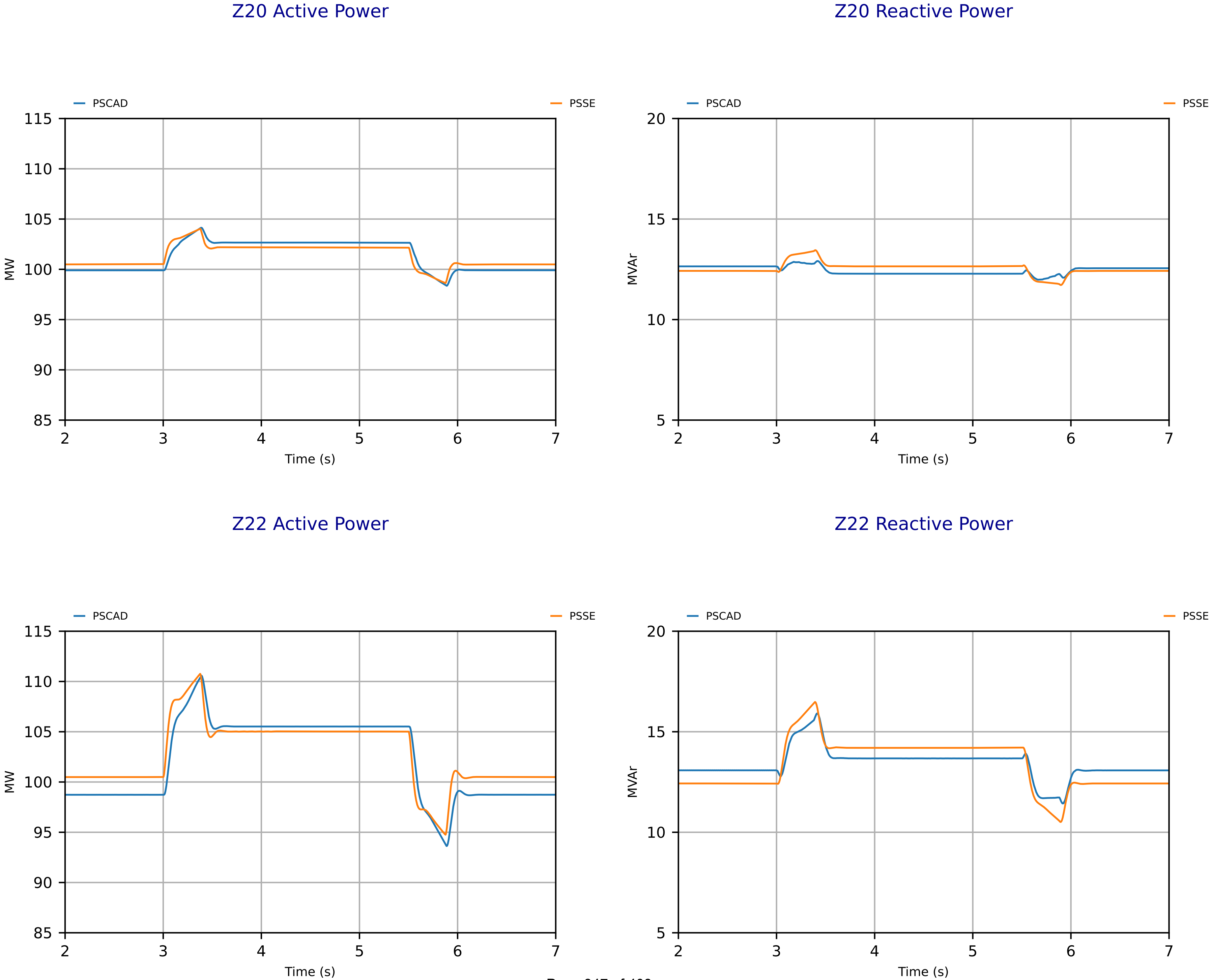
Test #7:

51.5 Hz frequency step for 2.5 sec (4 Hz/s)

CMLD_SMIB_SCR_10_XR_3_T7_1

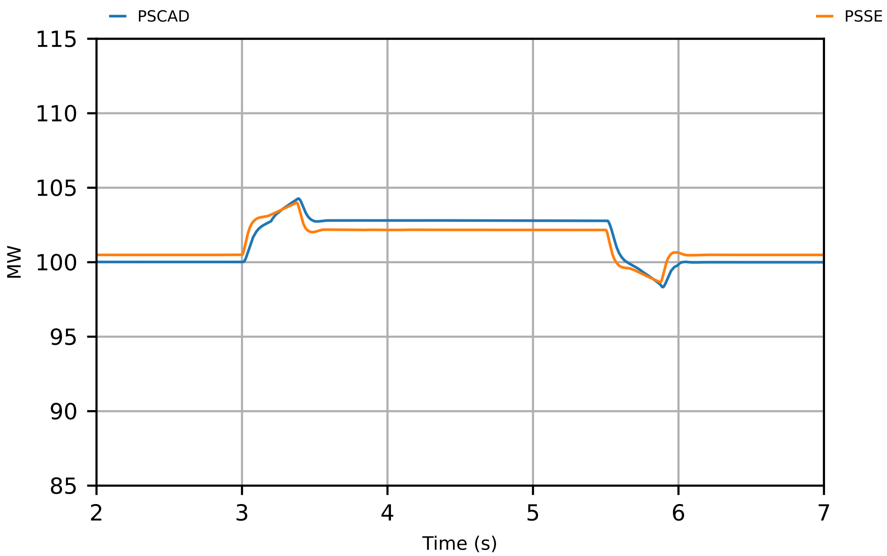


CMLD_SMIB_SCR_10_XR_3_T7_2

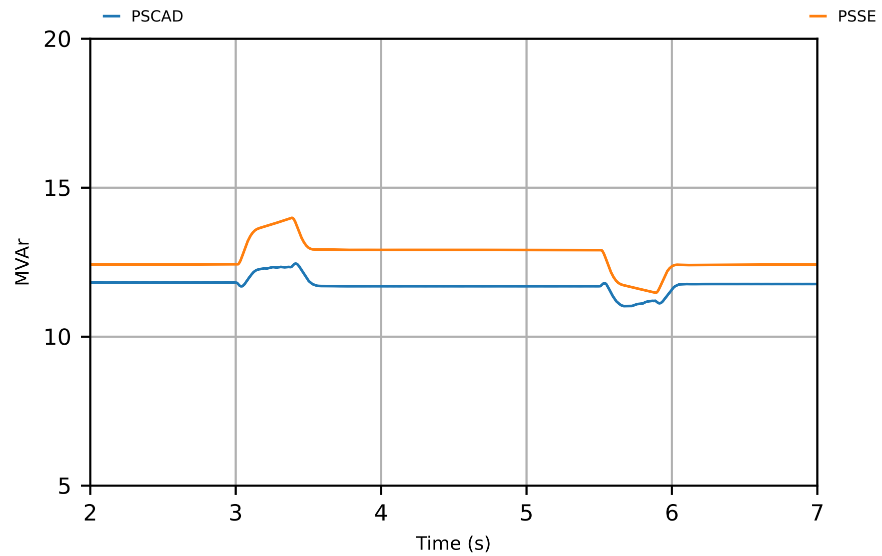


CMLD_SMIB_SCR_10_XR_3_T7_3

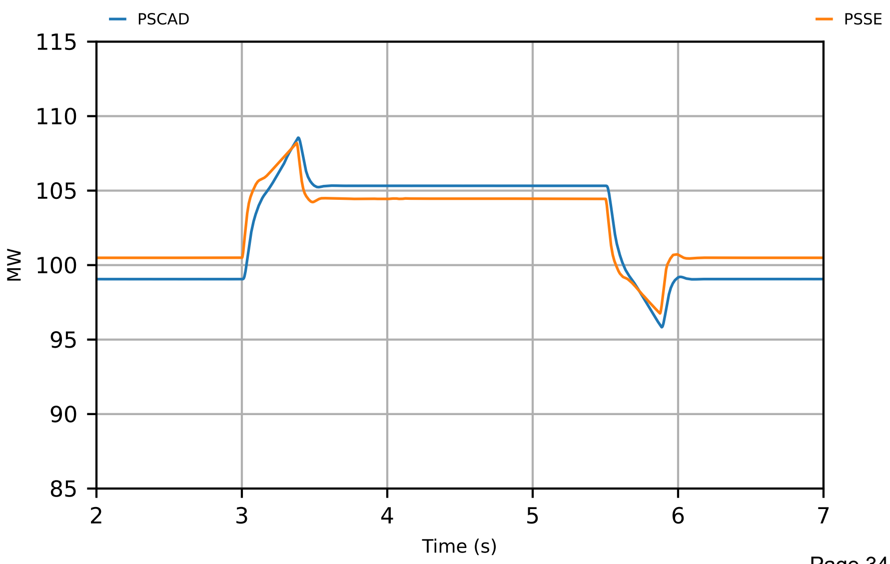
Z29 Active Power



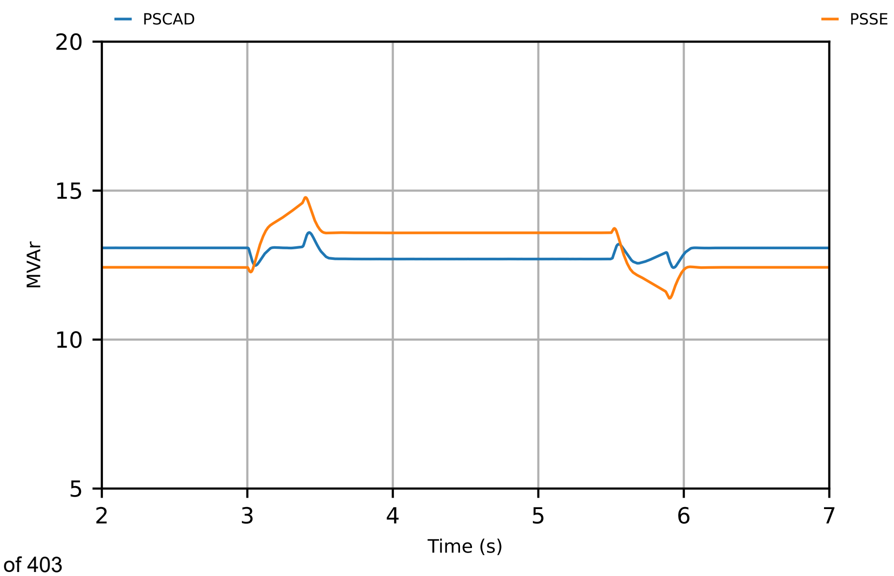
Z29 Reactive Power



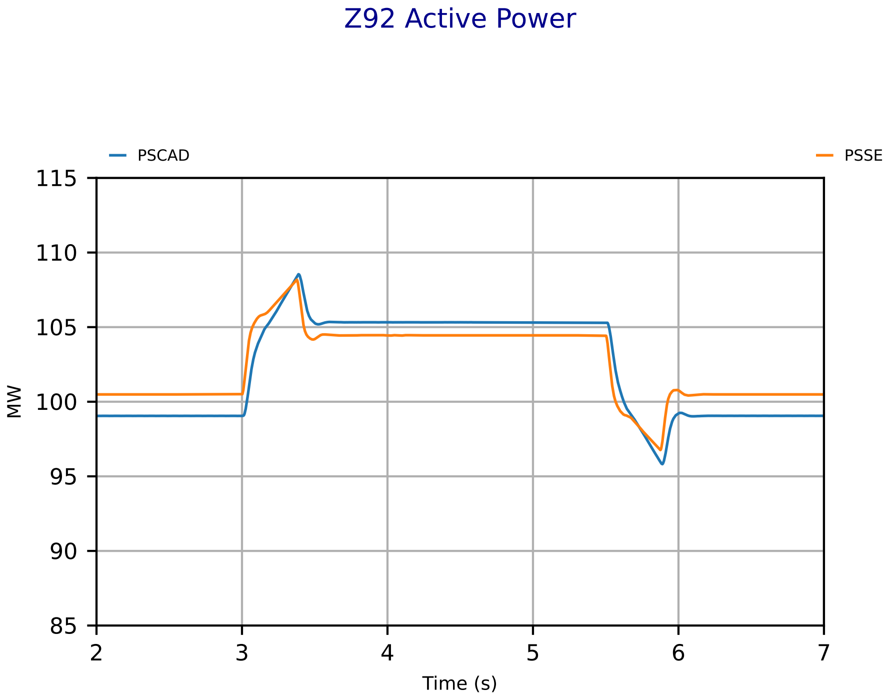
Z82 Active Power

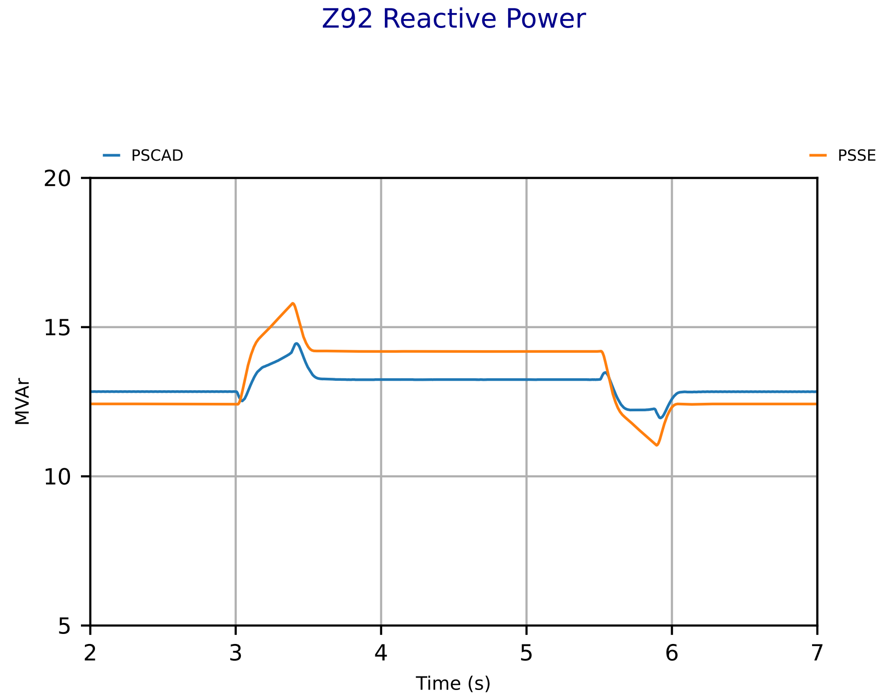


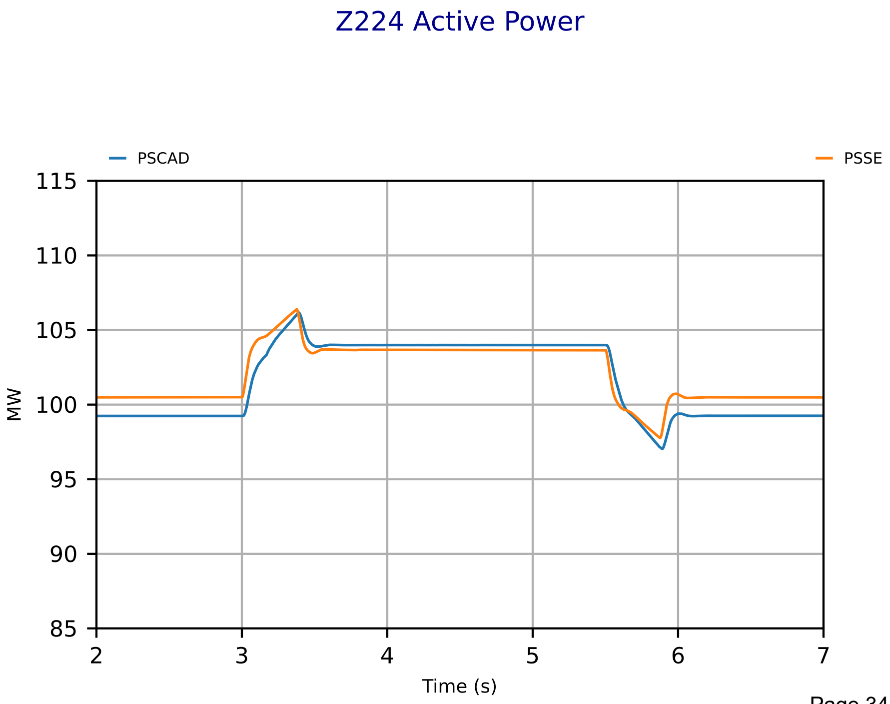
Z82 Reactive Power

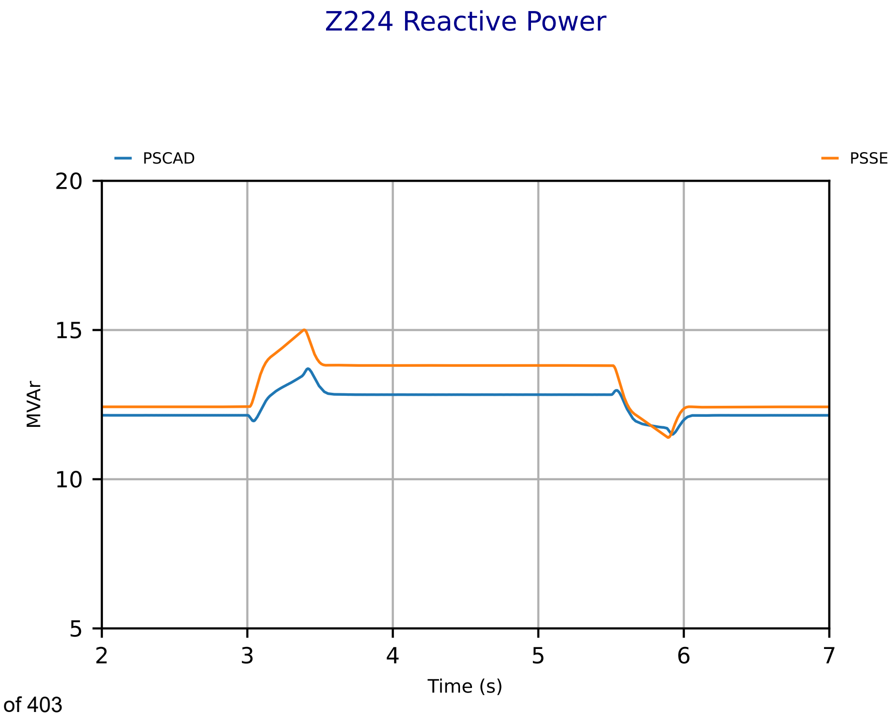


CMLD_SMIB_SCR_10_XR_3_T7_4









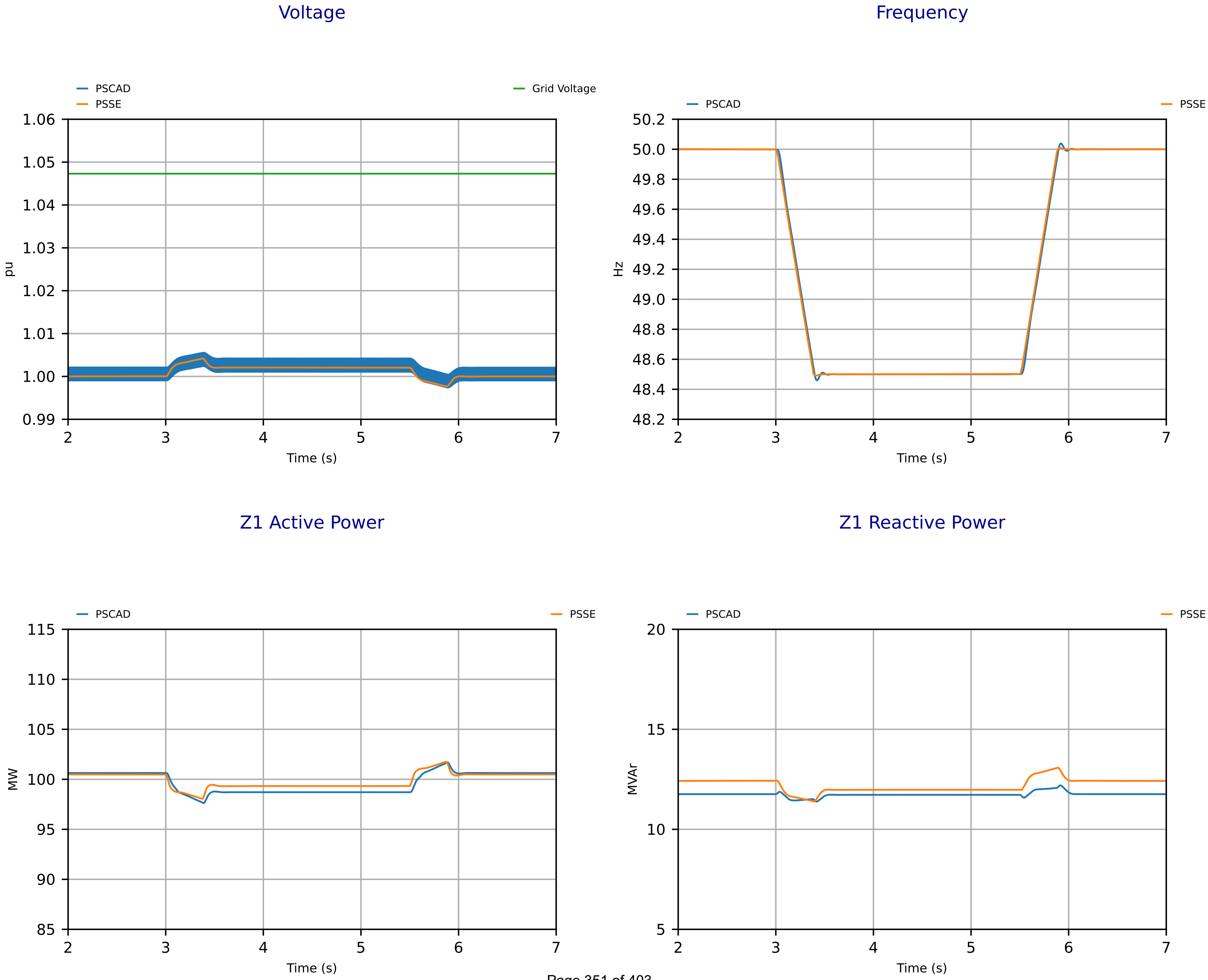
CMLD SMIB

SCR = 10, X/R = 3

Test #8:

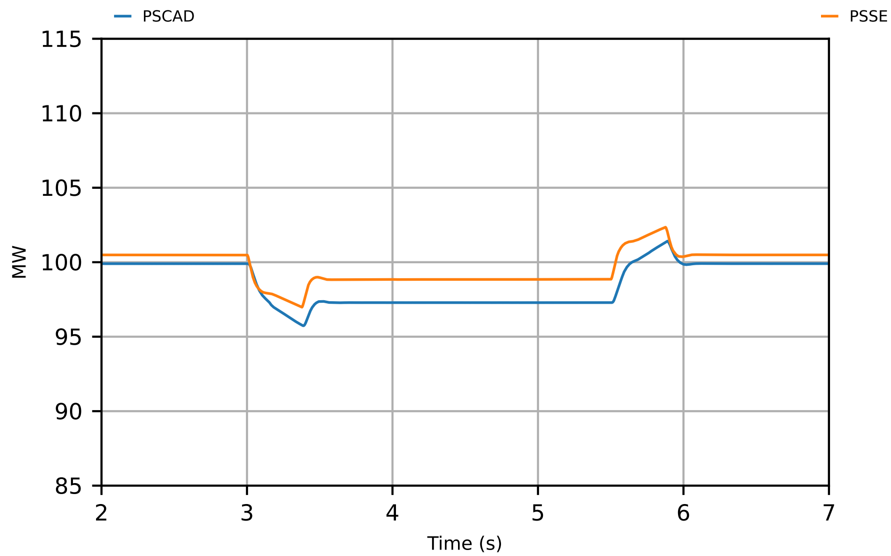
48.5 Hz frequency step for 2.5 sec (4 Hz/s)

CMLD_SMIB_SCR_10_XR_3_T8_1

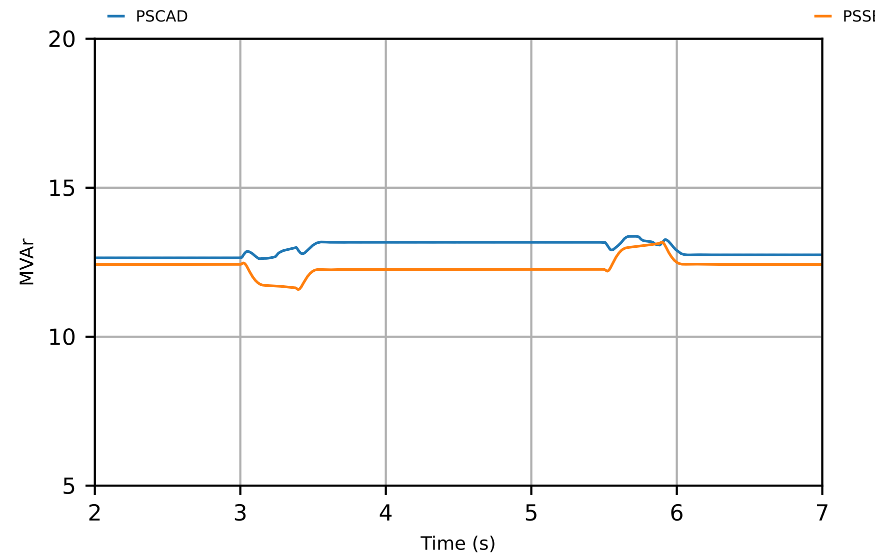


CMLD_SMIB_SCR_10_XR_3_T8_2

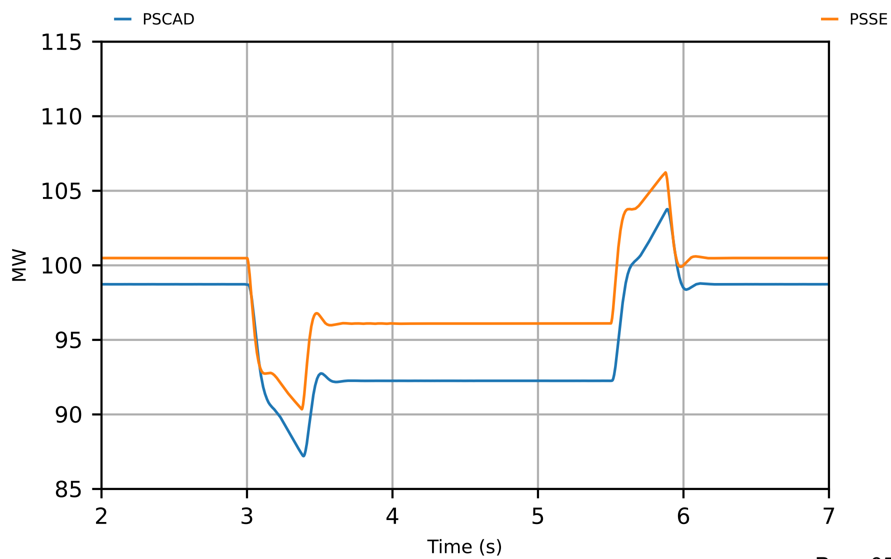
Z20 Active Power



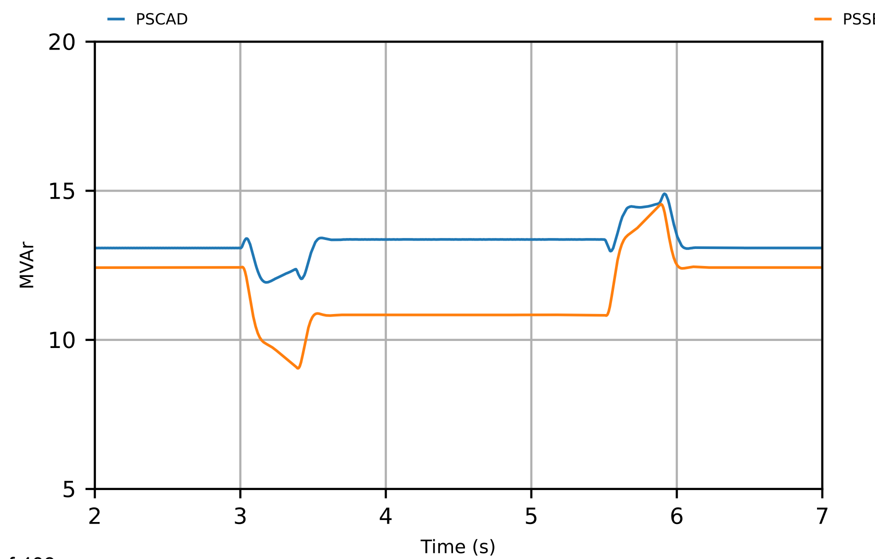
Z20 Reactive Power



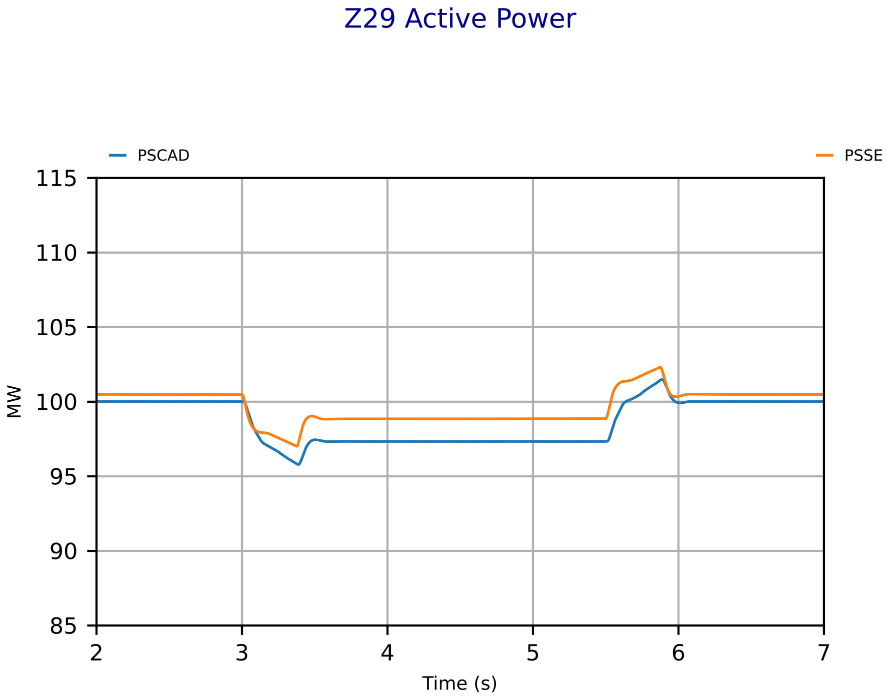
Z22 Active Power

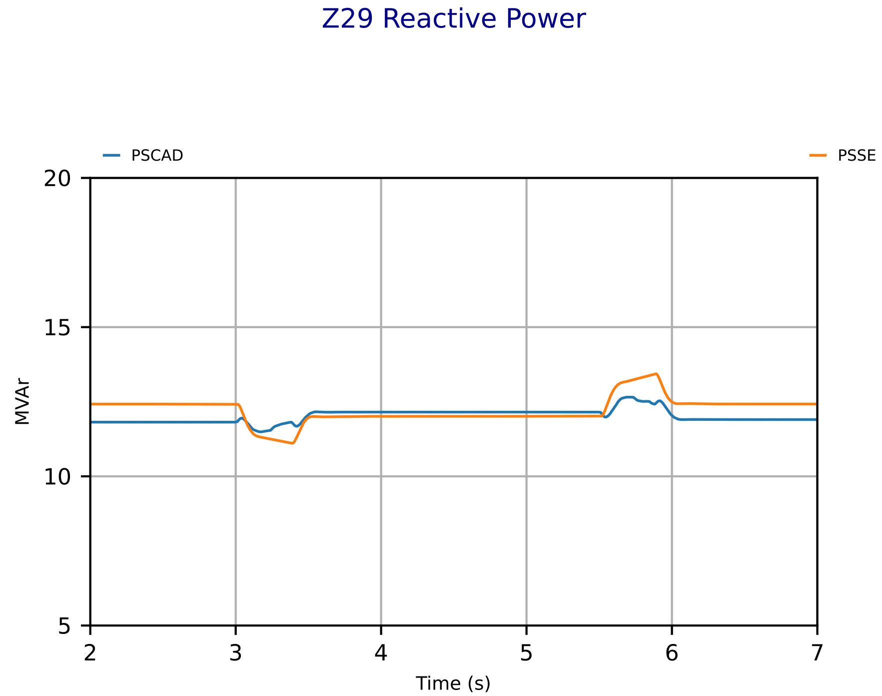


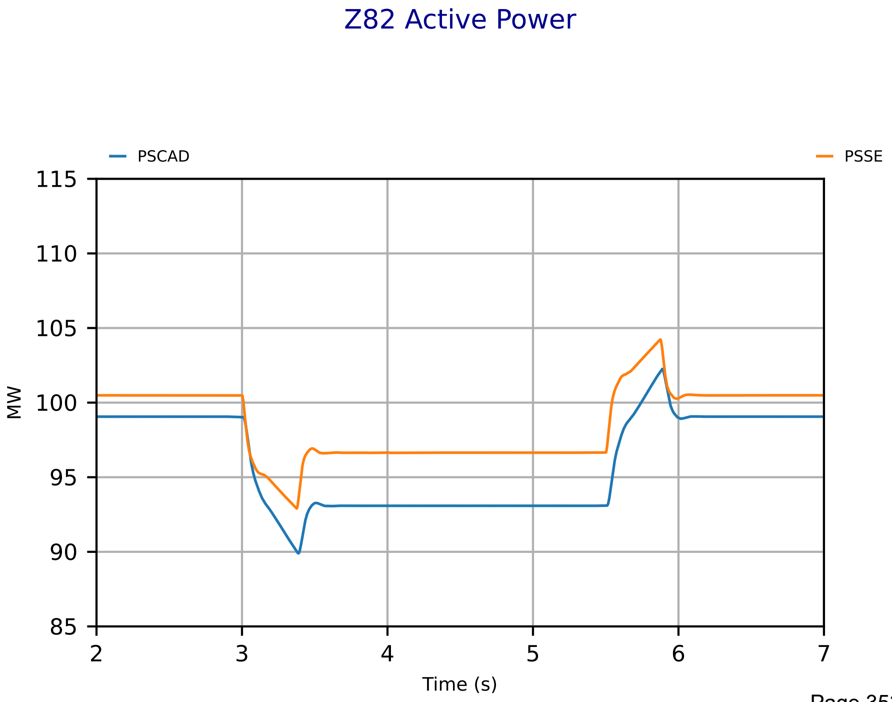
Z22 Reactive Power

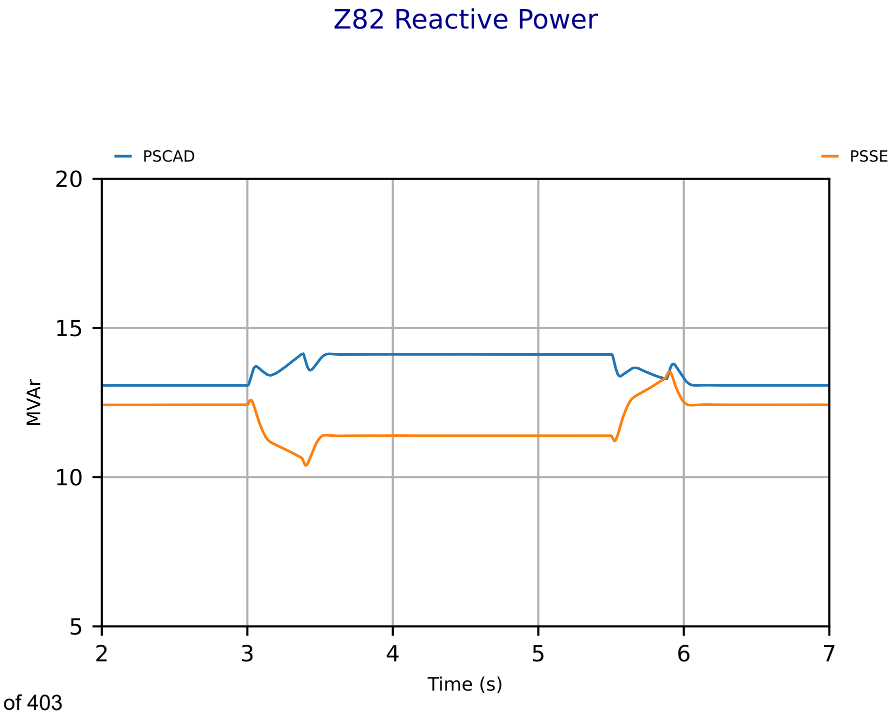


CMLD_SMIB_SCR_10_XR_3_T8_3

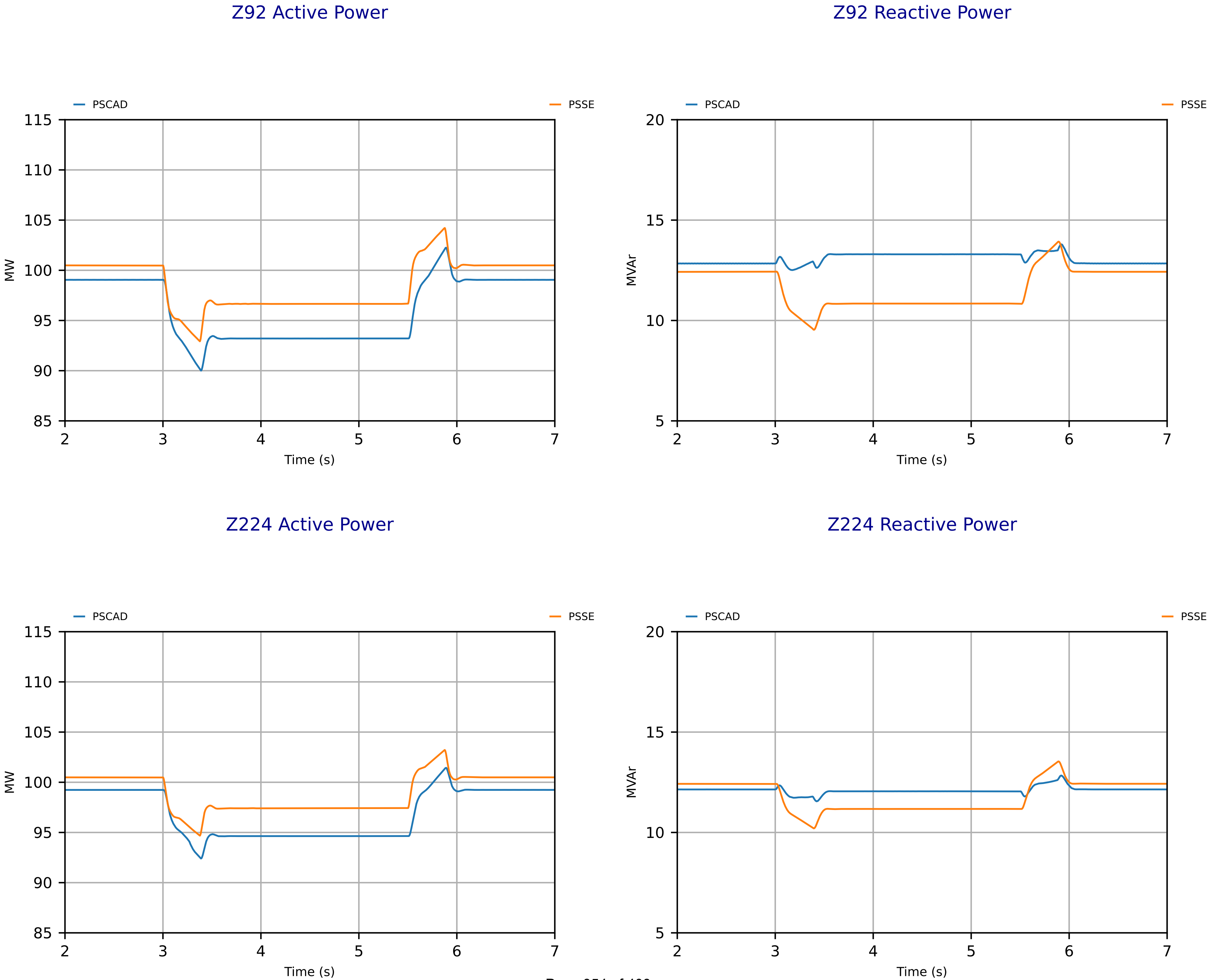








CMLD_SMIB_SCR_10_XR_3_T8_4



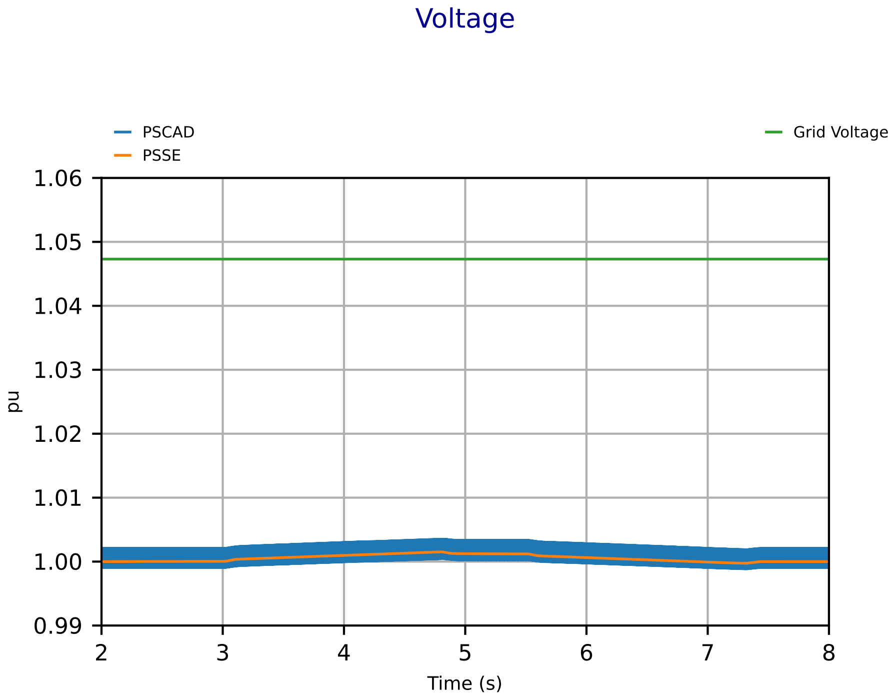
CMLD SMIB

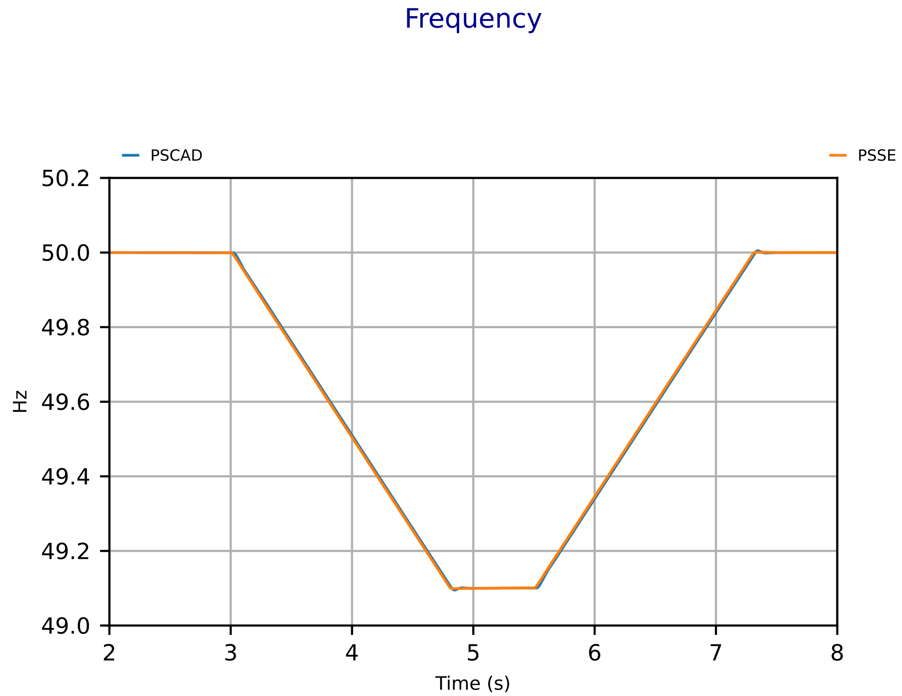
SCR = 10, X/R = 3

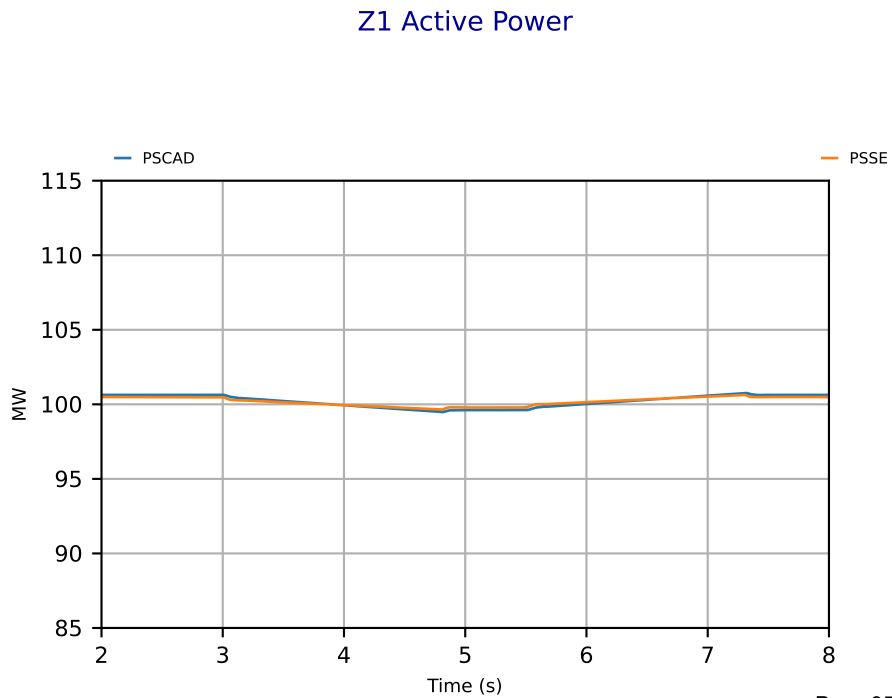
Test #9:

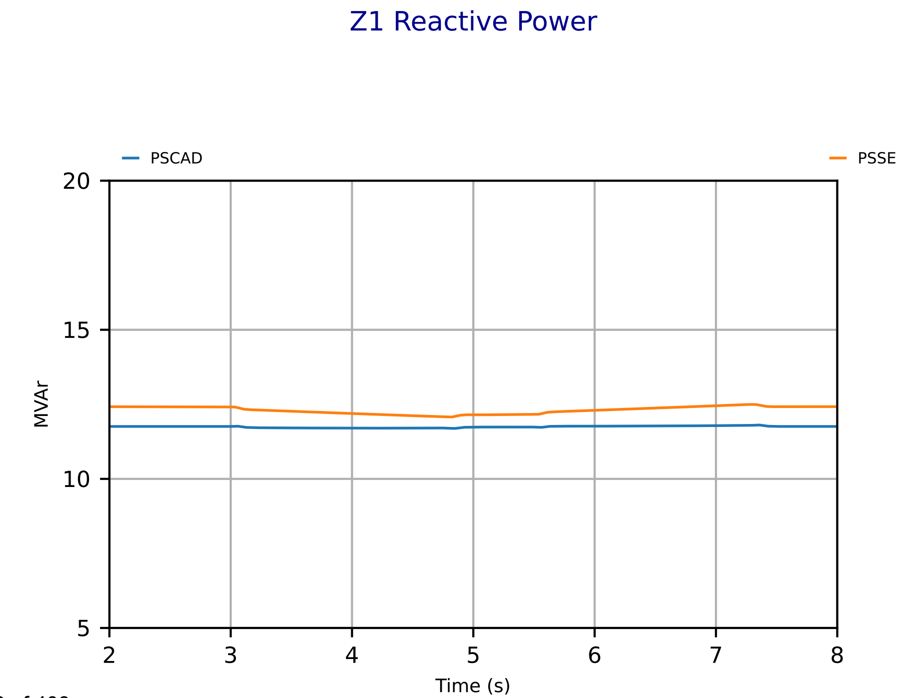
49.1 Hz slow frequency ramp (0.5 Hz/s)

CMLD_SMIB_SCR_10_XR_3_T9_1



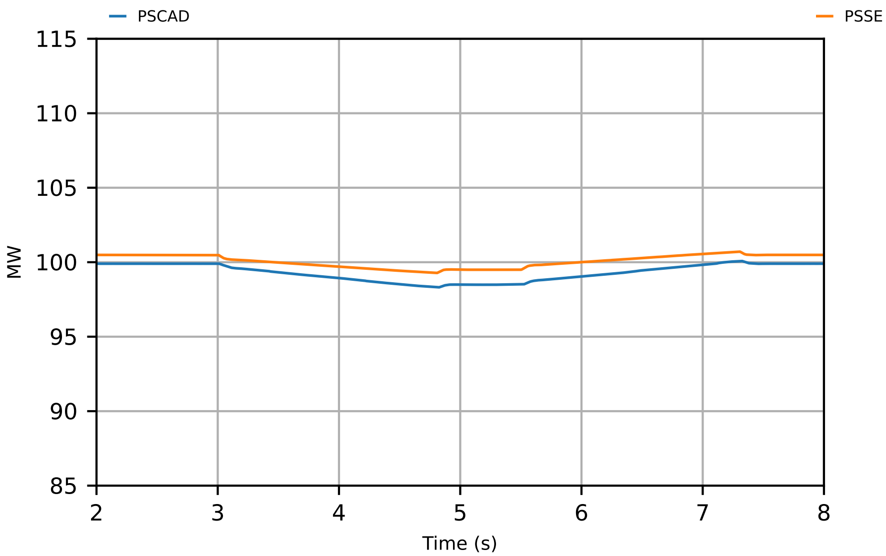




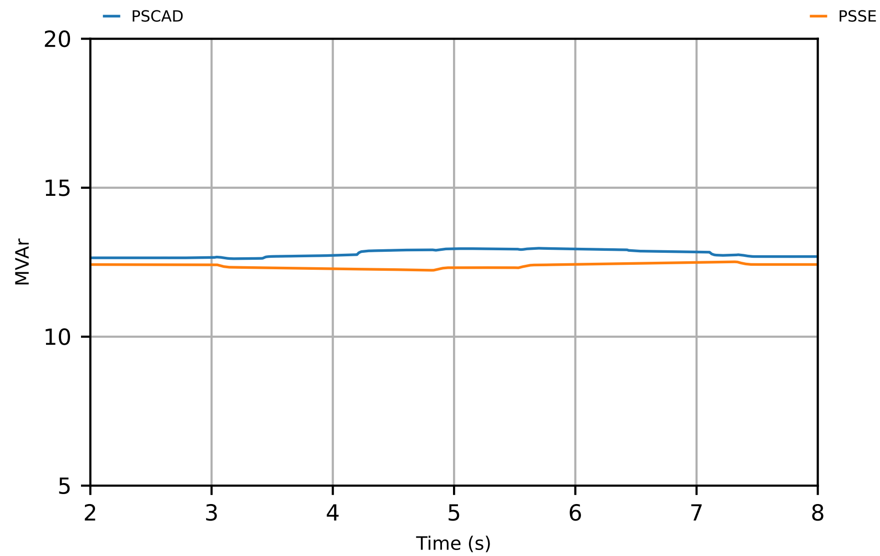


CMLD_SMIB_SCR_10_XR_3_T9_2

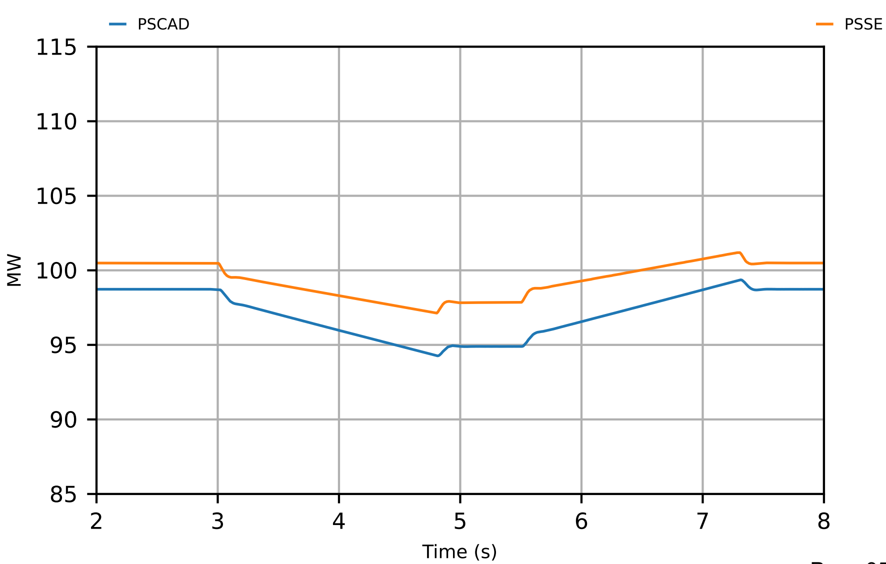
Z20 Active Power



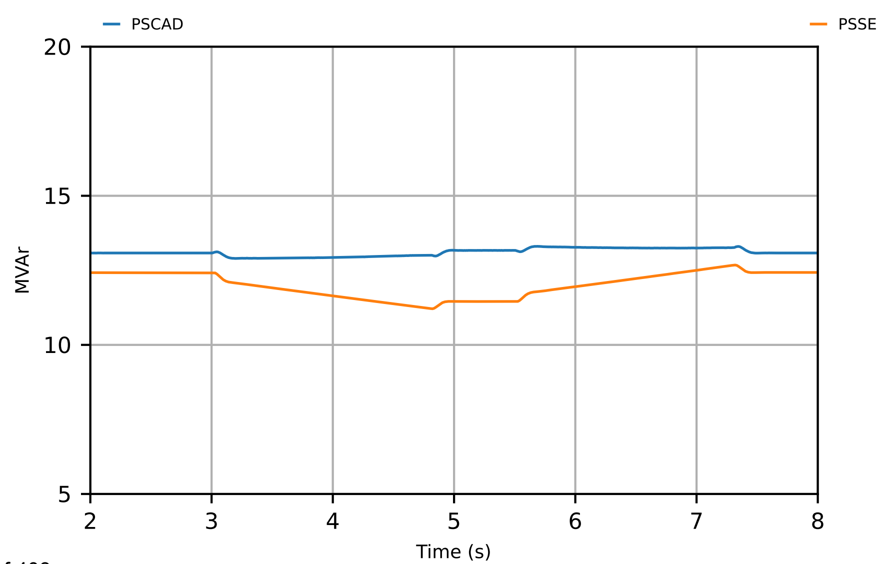
Z20 Reactive Power



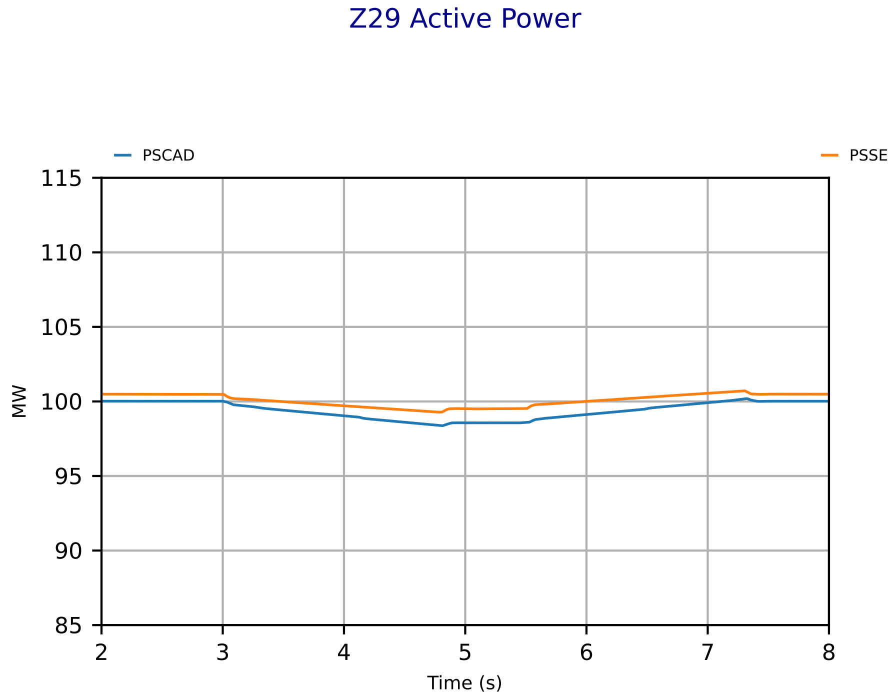
Z22 Active Power

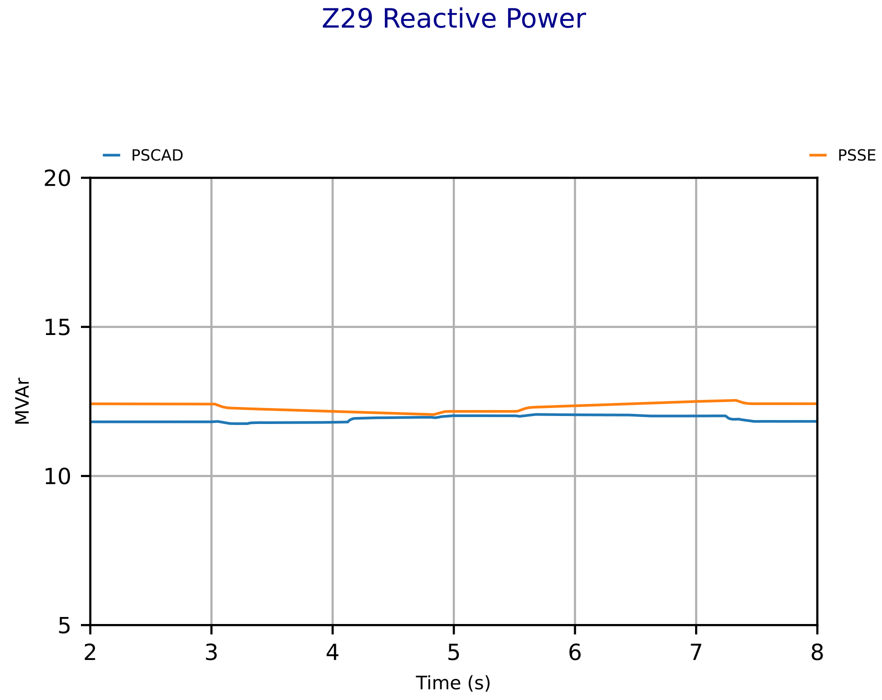


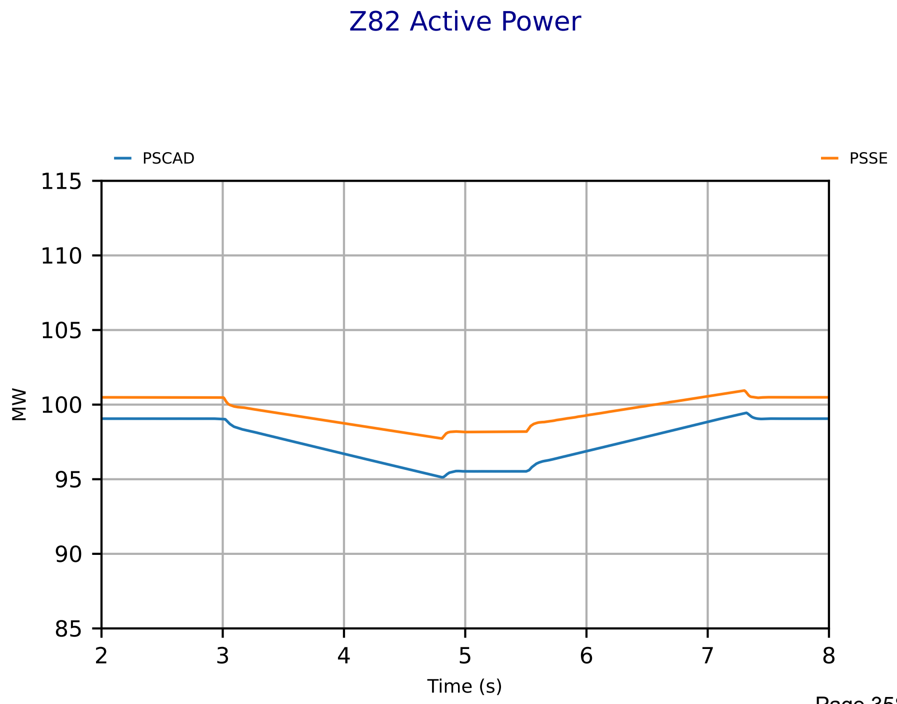
Z22 Reactive Power

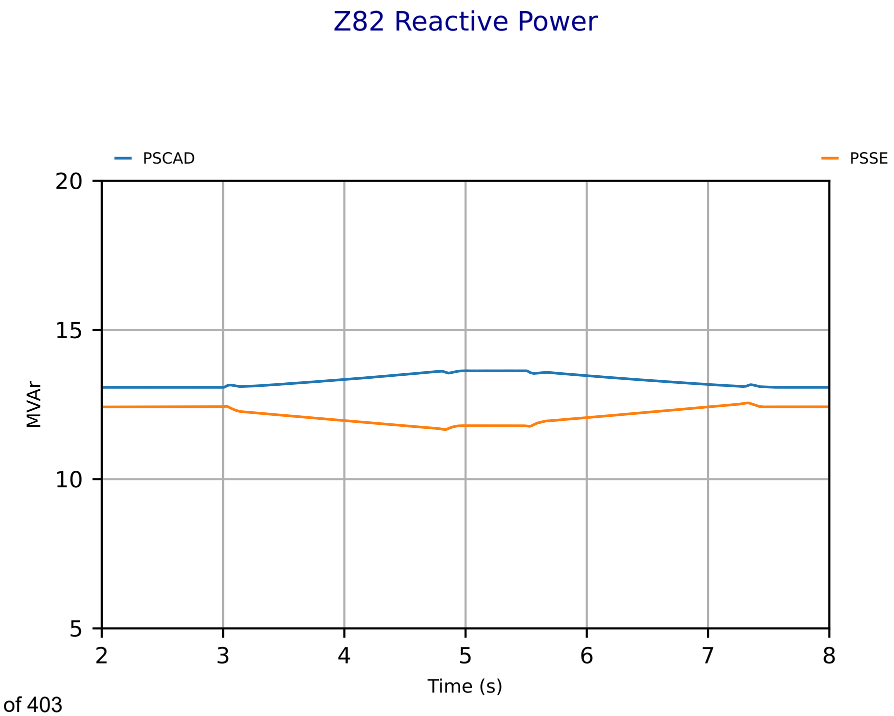


CMLD_SMIB_SCR_10_XR_3_T9_3

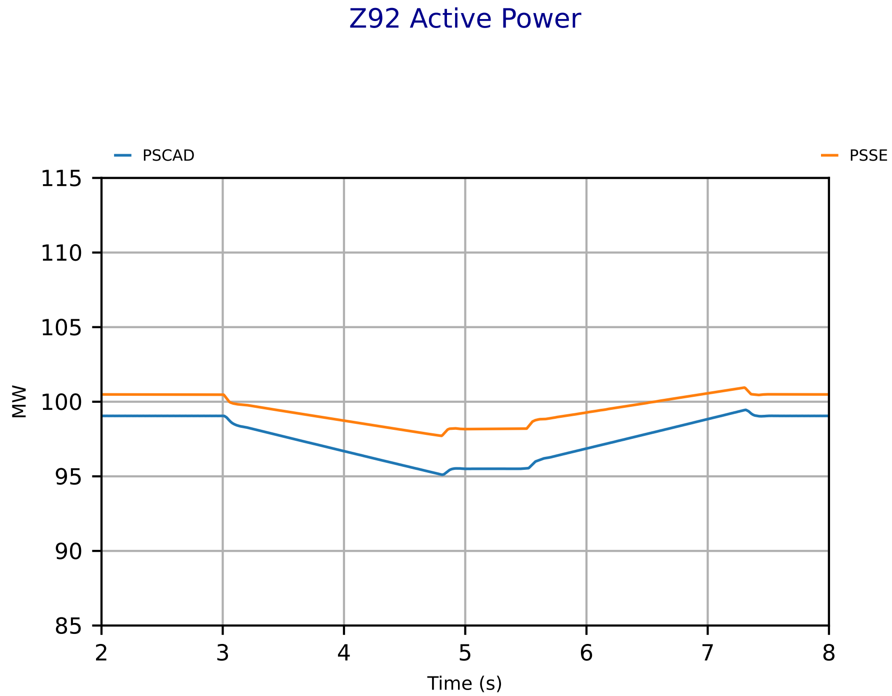


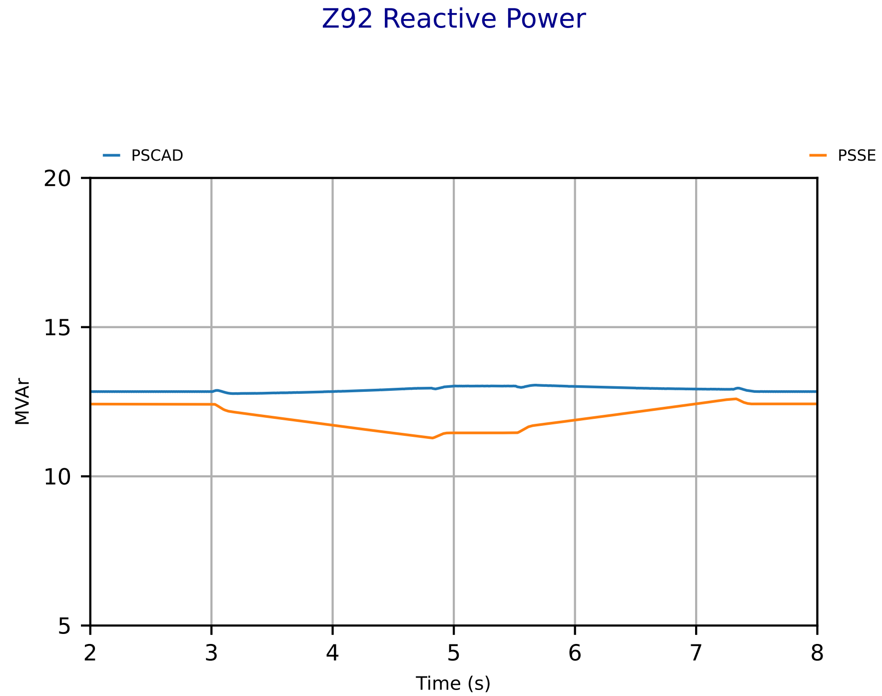


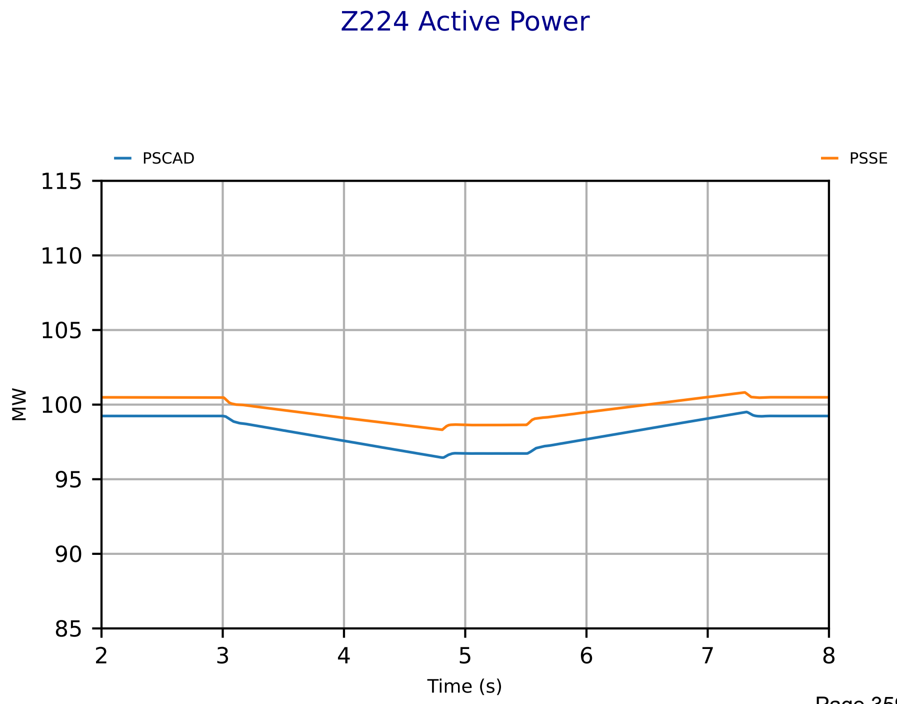


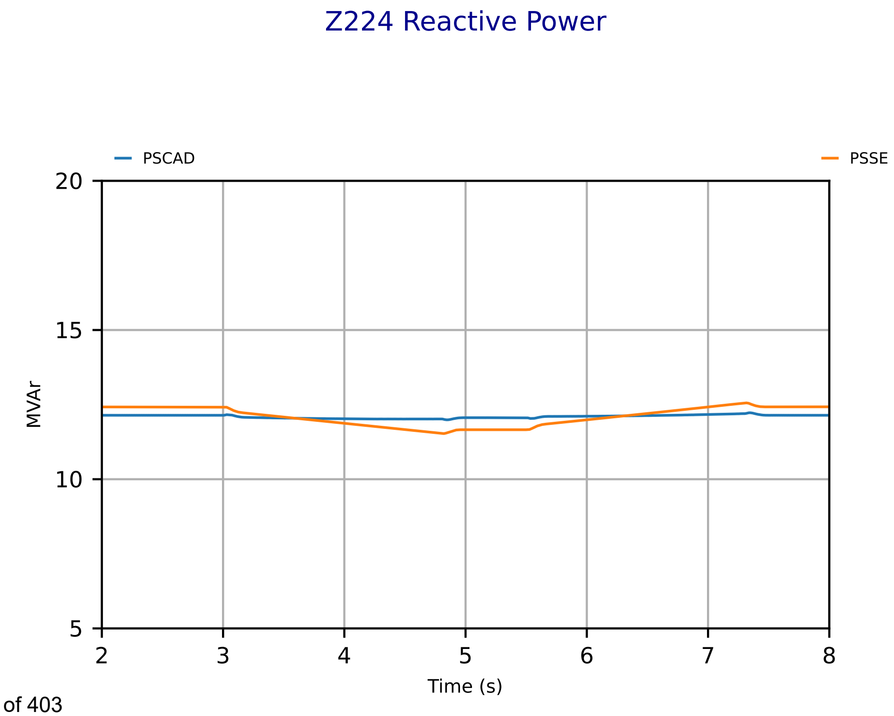


CMLD_SMIB_SCR_10_XR_3_T9_4









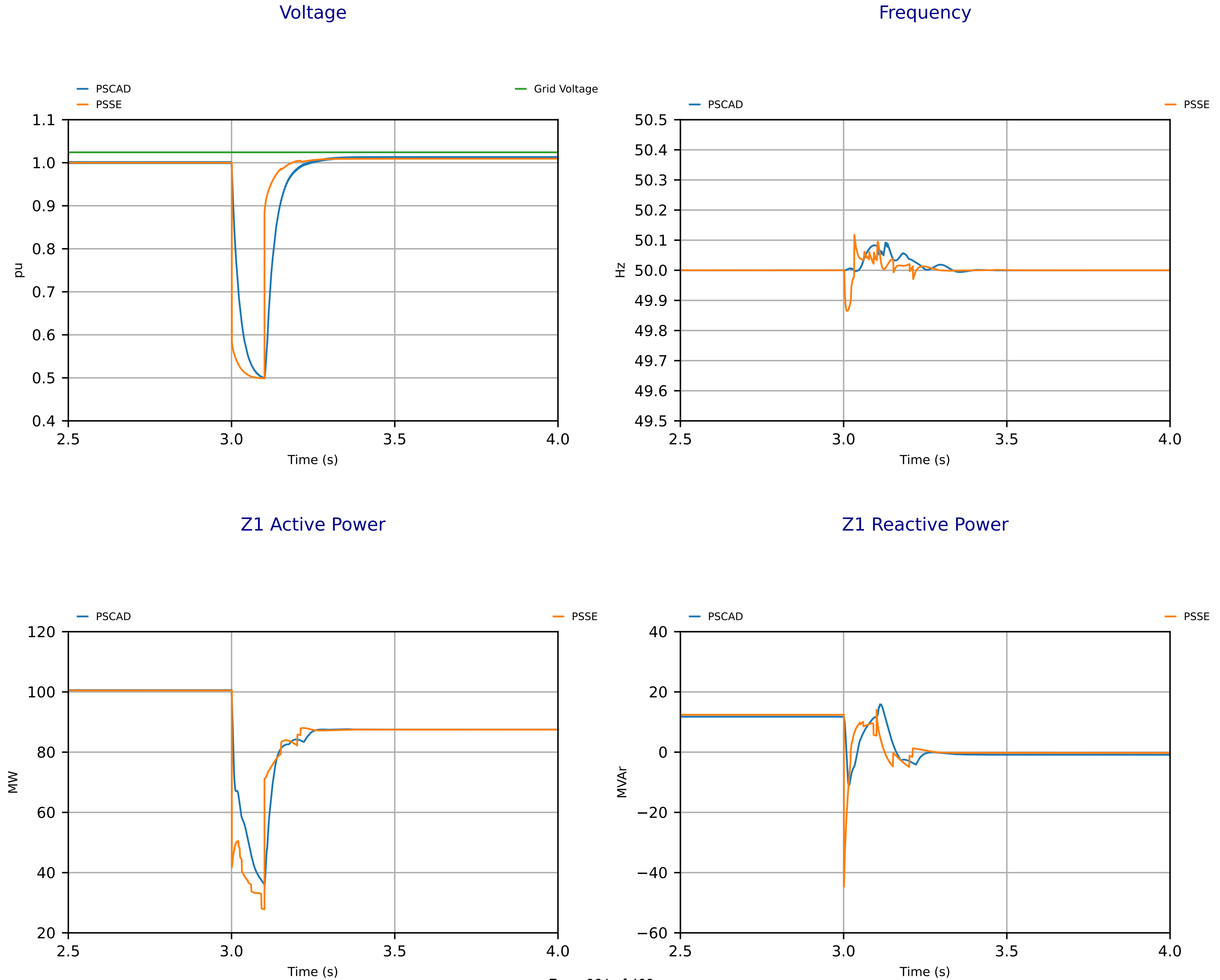
CMLD SMIB

SCR = 10, X/R = 14

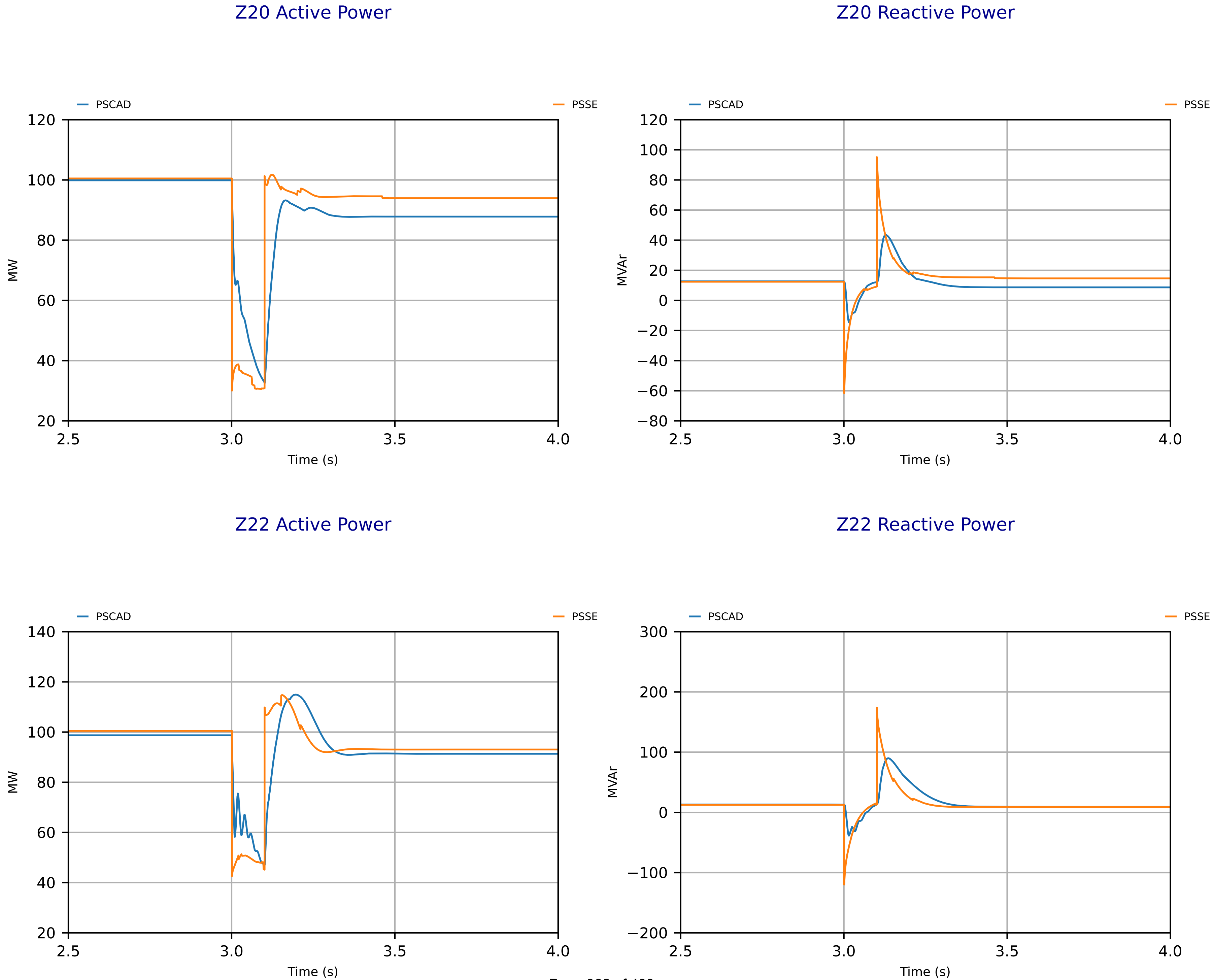
Test #2:

LLG fault for 100 ms

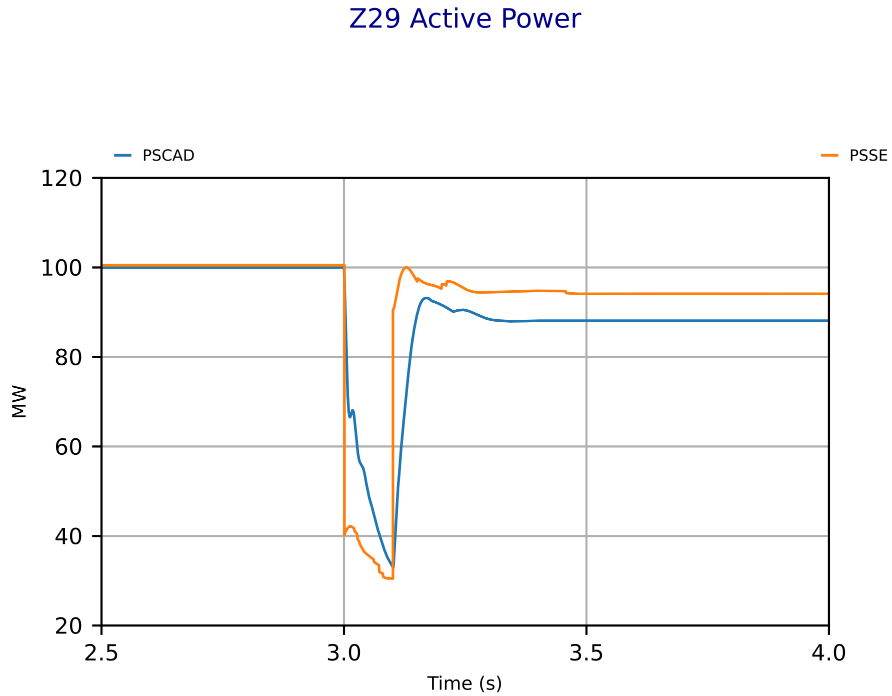
CMLD_SMIB_SCR_10_XR_14_T2_1

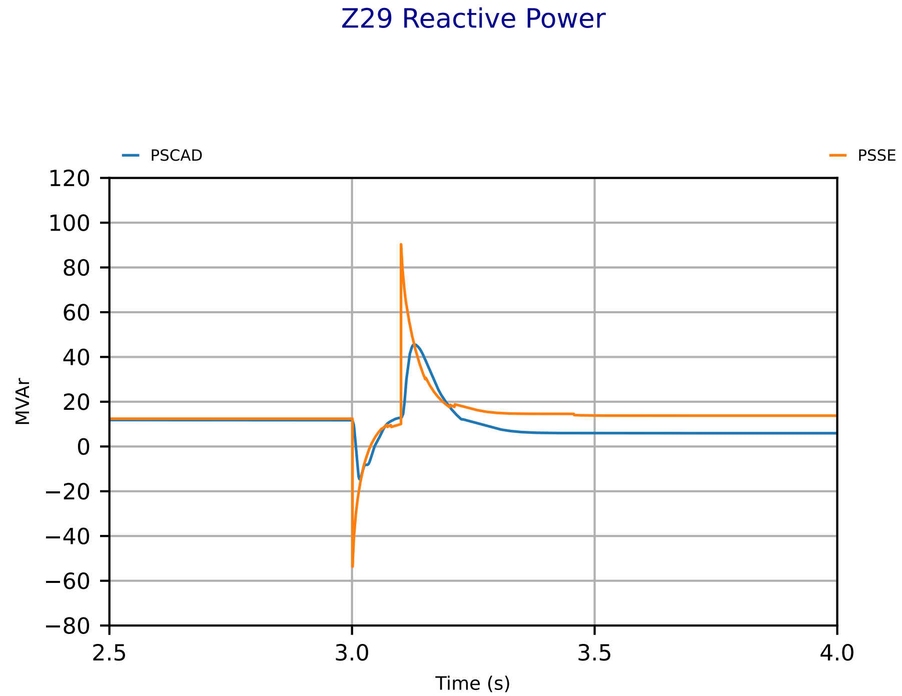


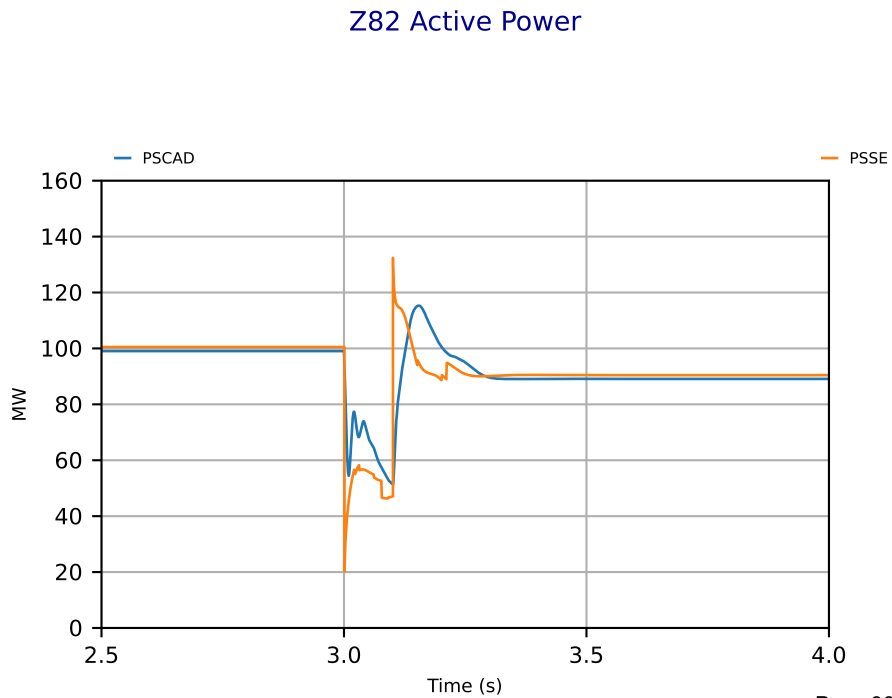
CMLD_SMIB_SCR_10_XR_14_T2_2

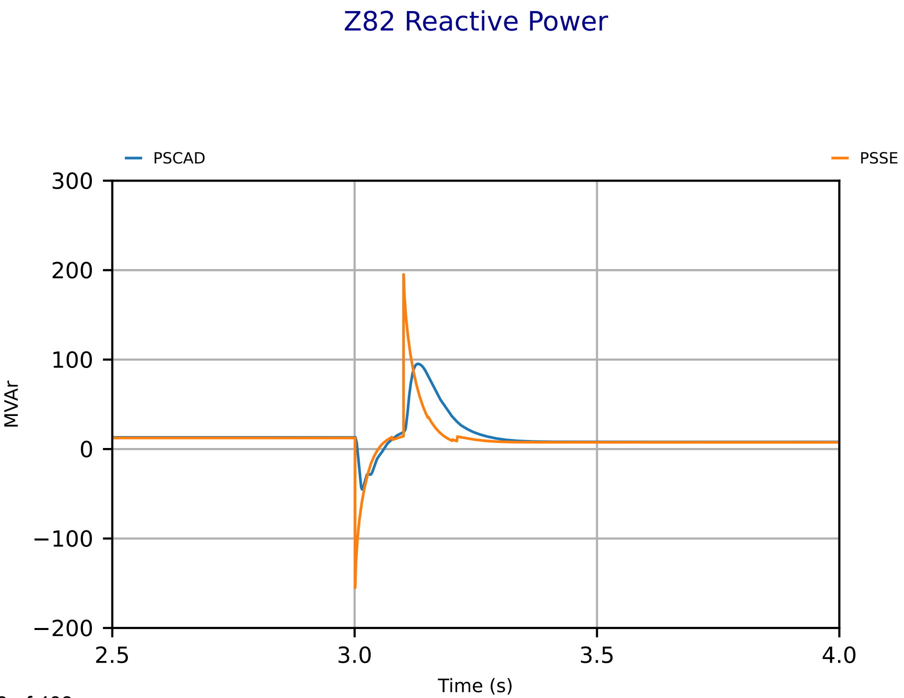


CMLD_SMIB_SCR_10_XR_14_T2_3

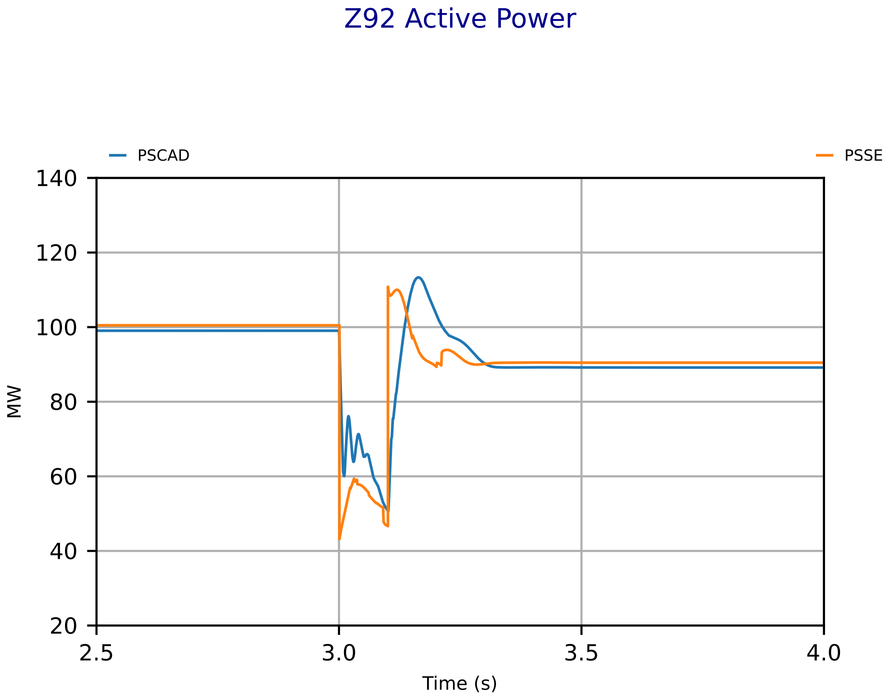


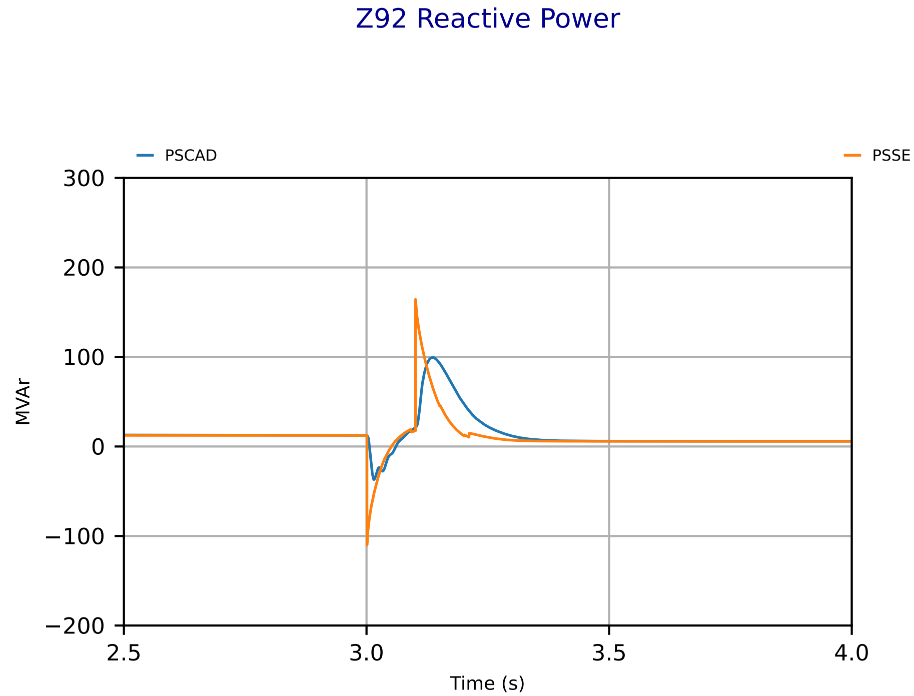


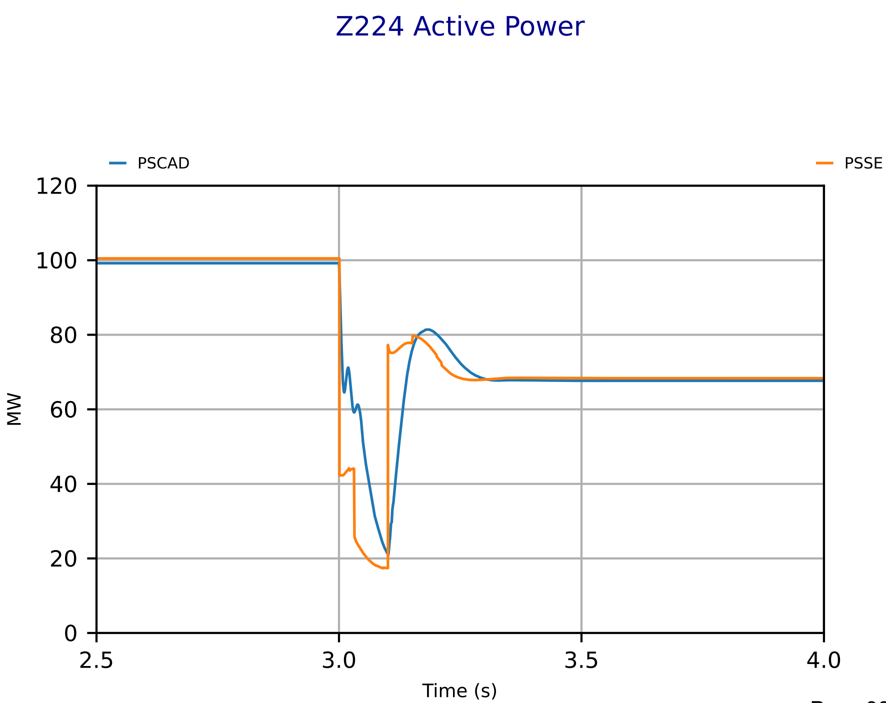


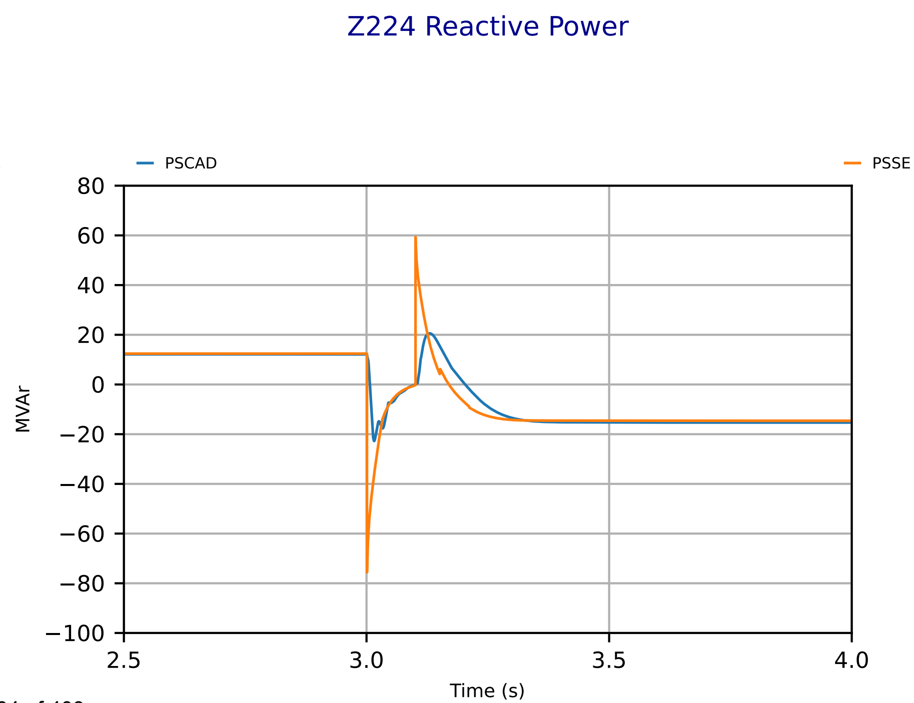


CMLD_SMIB_SCR_10_XR_14_T2_4







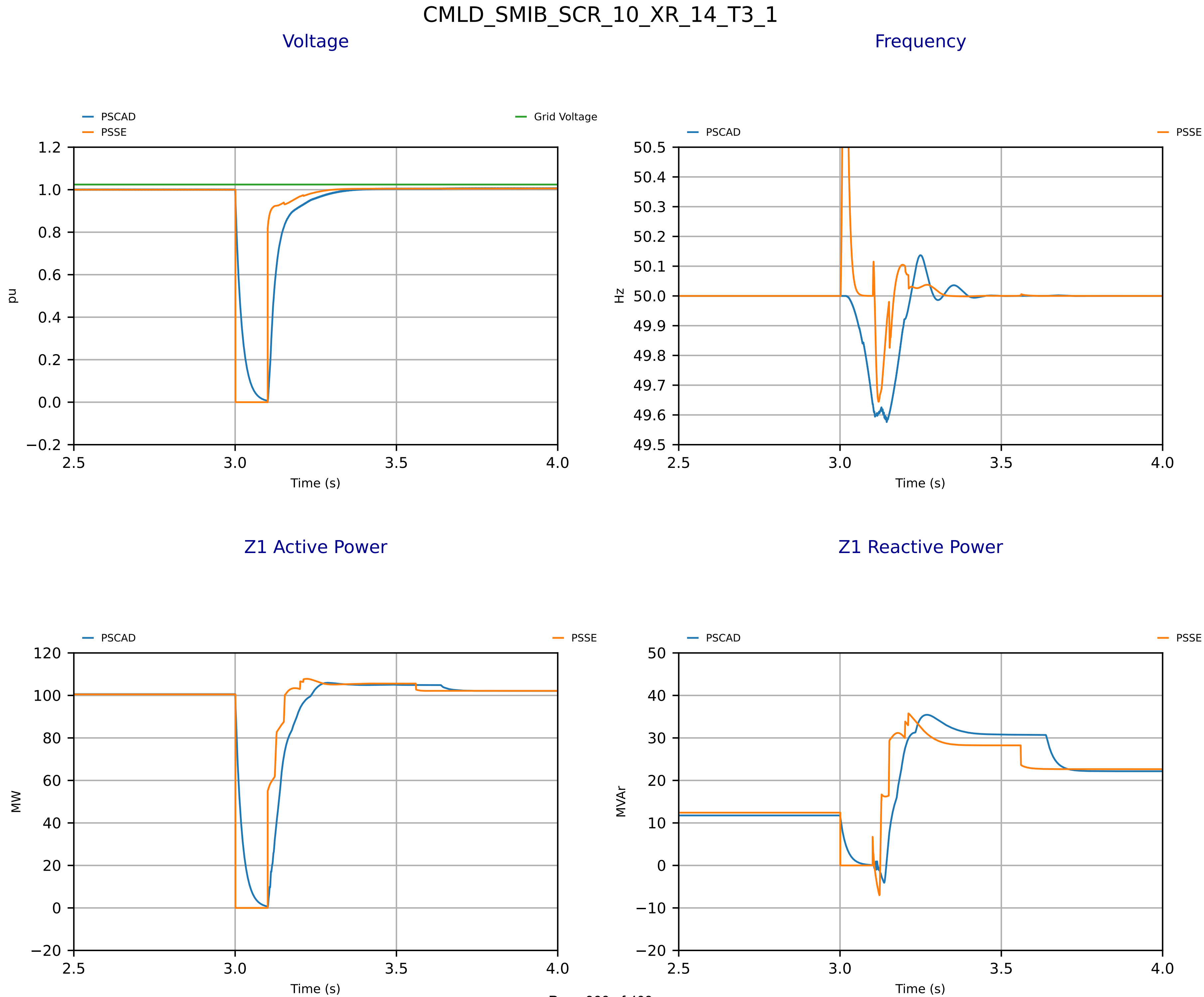


CMLD SMIB

SCR = 10, X/R = 14

Test #3:

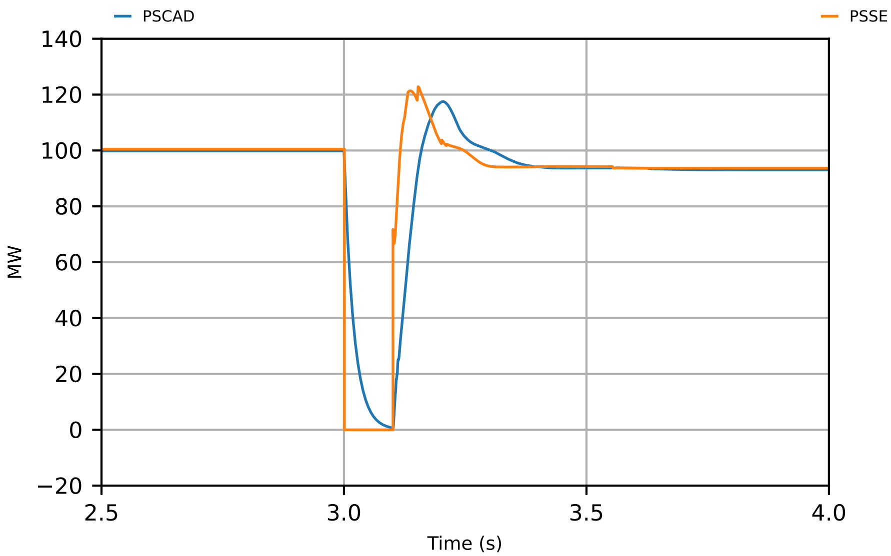
3PH-G fault for 100 ms



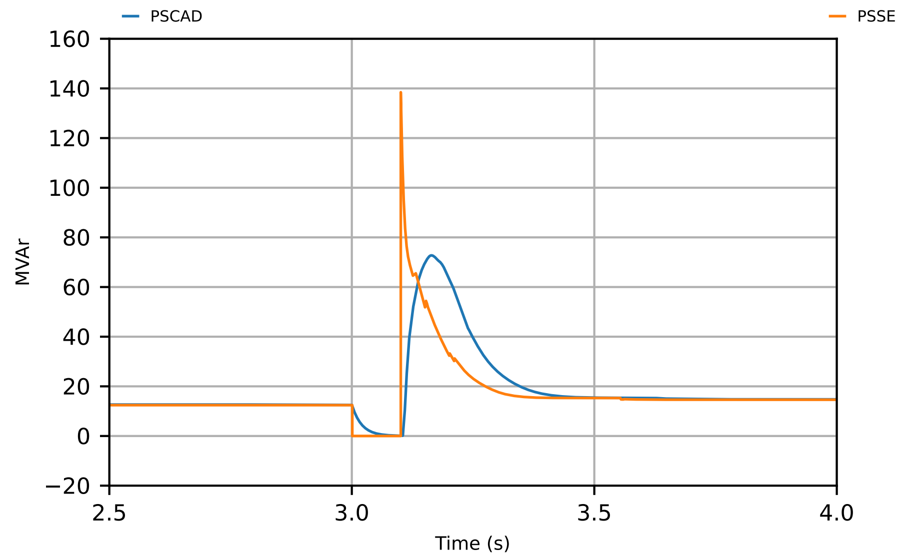
CMLD_SMIB_SCR_10_XR_14_T3_1
Voltage
PSCAD
PSSE
Grid Voltage
pu
Time (s)
Frequency
Hz
Z1 Active Power
MW
Z1 Reactive Power
MVAr

CMLD_SMIB_SCR_10_XR_14_T3_2

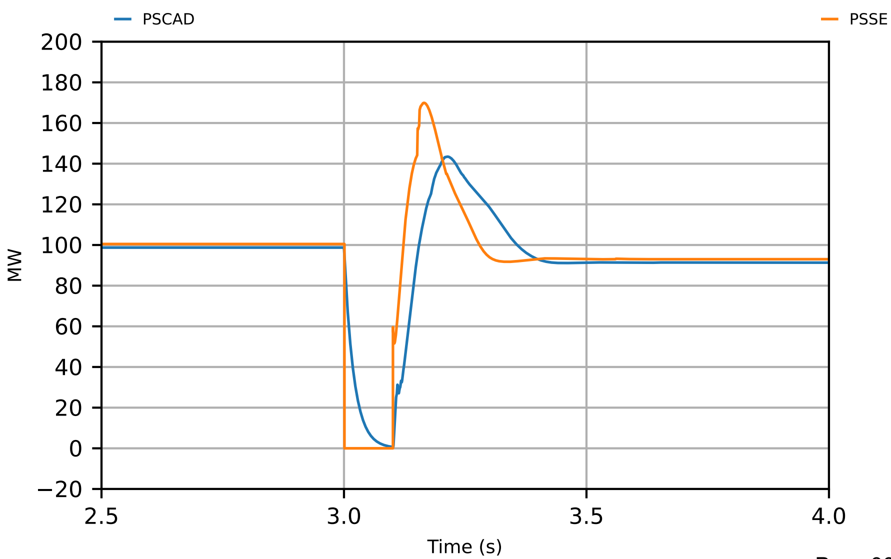
Z20 Active Power



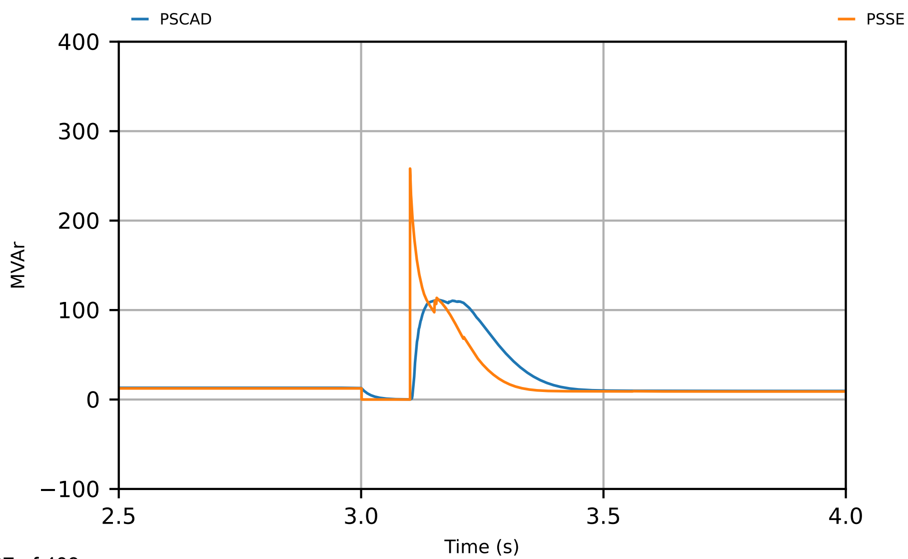
Z20 Reactive Power



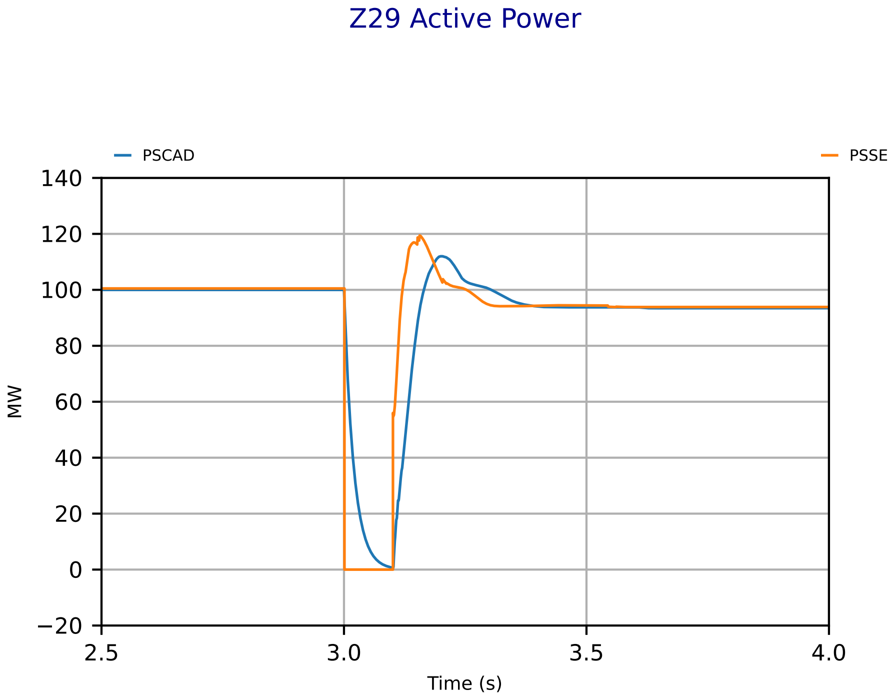
Z22 Active Power

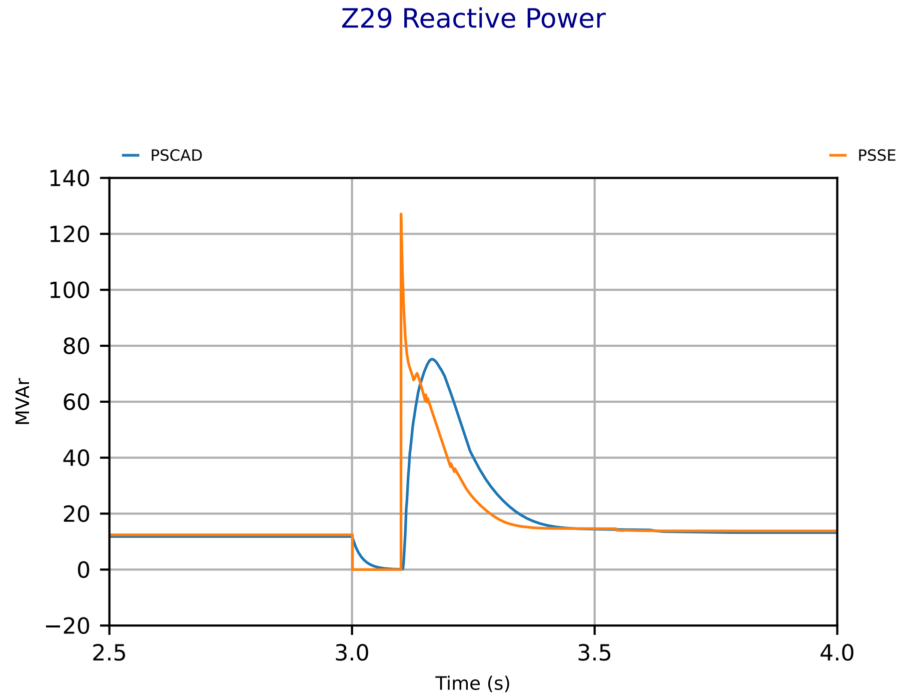


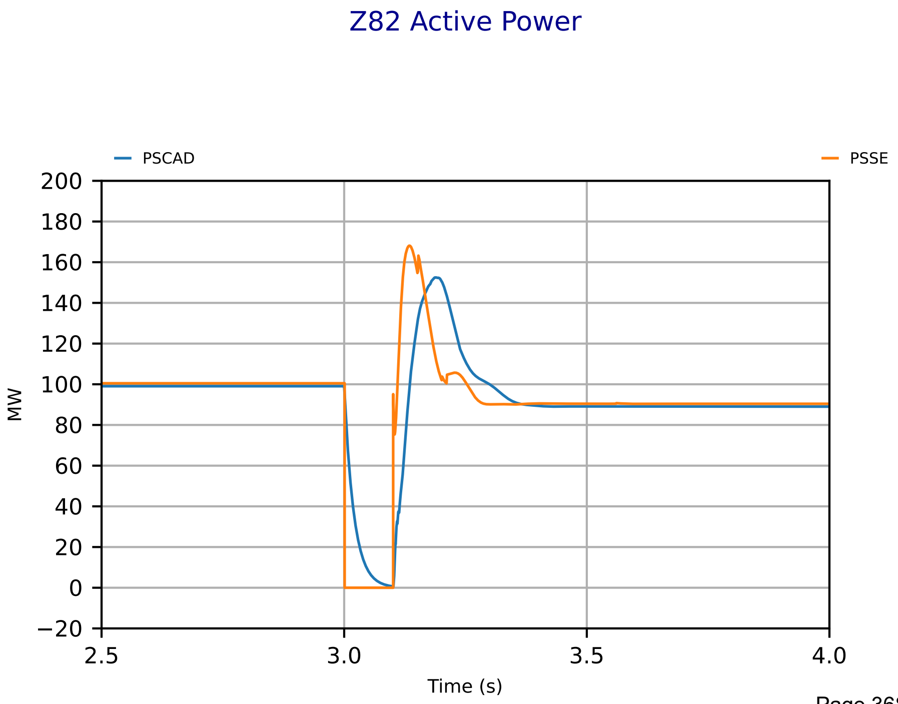
Z22 Reactive Power

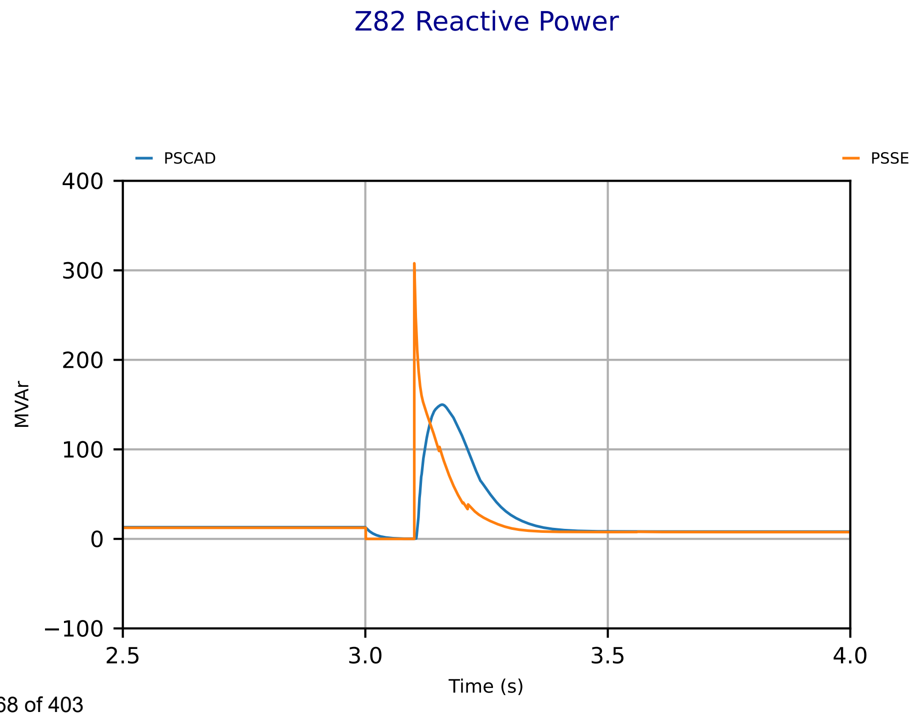


CMLD_SMIB_SCR_10_XR_14_T3_3



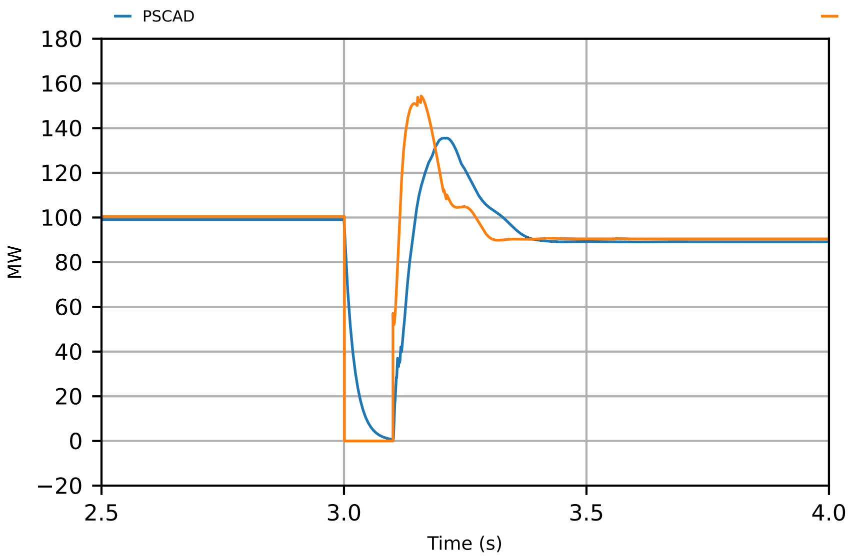




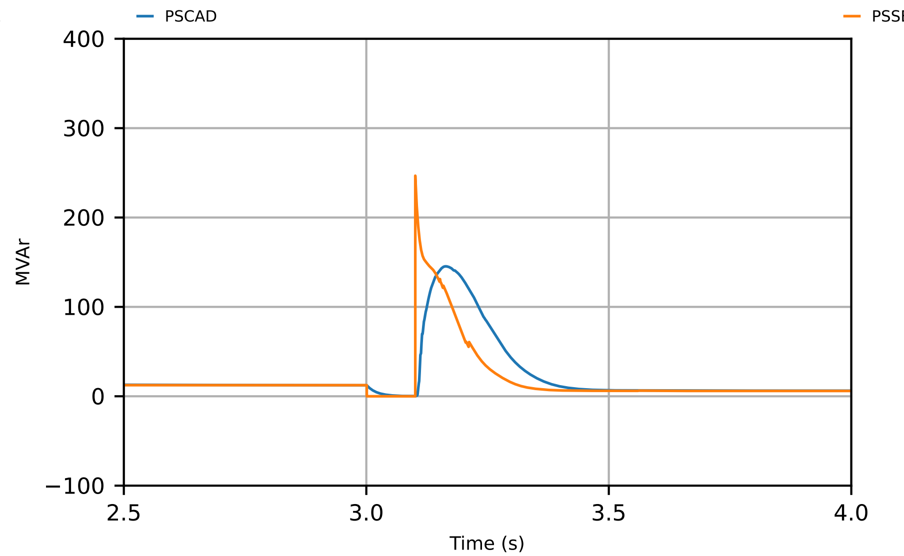


CMLD_SMIB_SCR_10_XR_14_T3_4

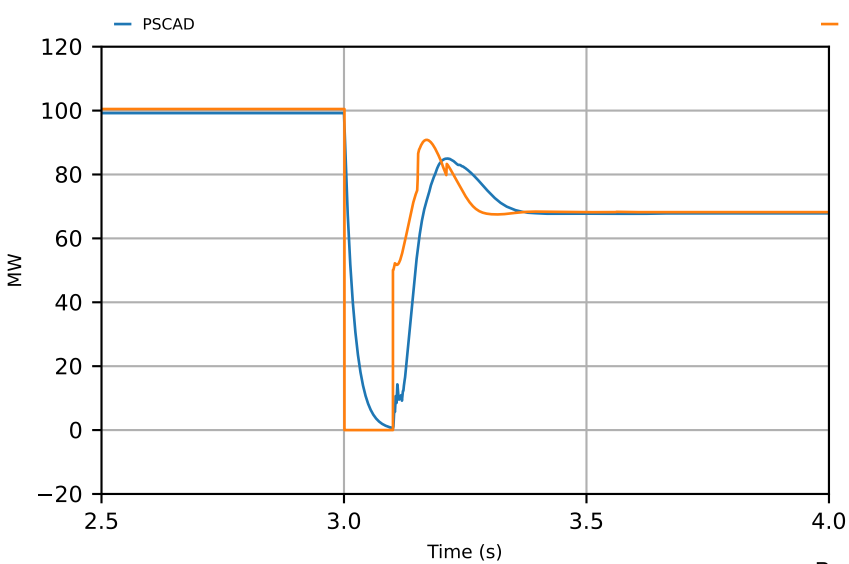
Z92 Active Power



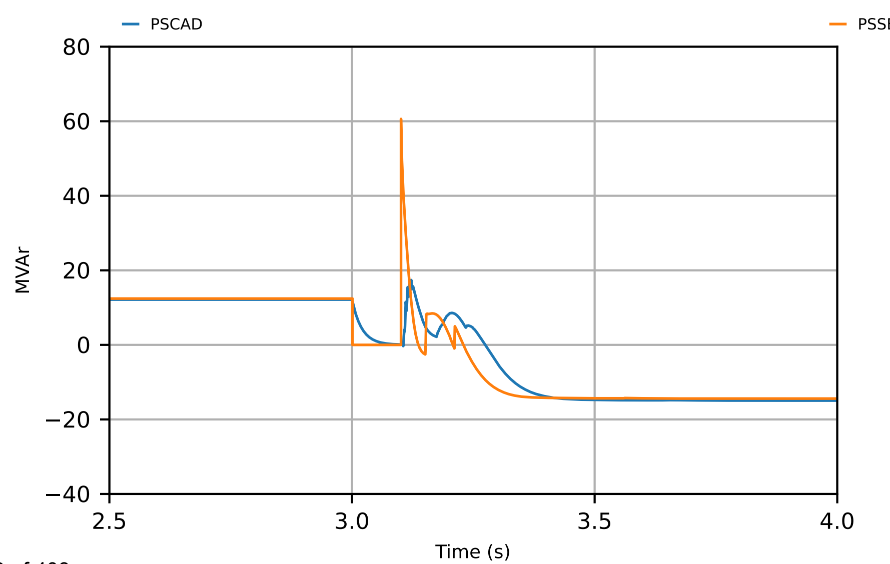
Z92 Reactive Power



Z224 Active Power



Z224 Reactive Power



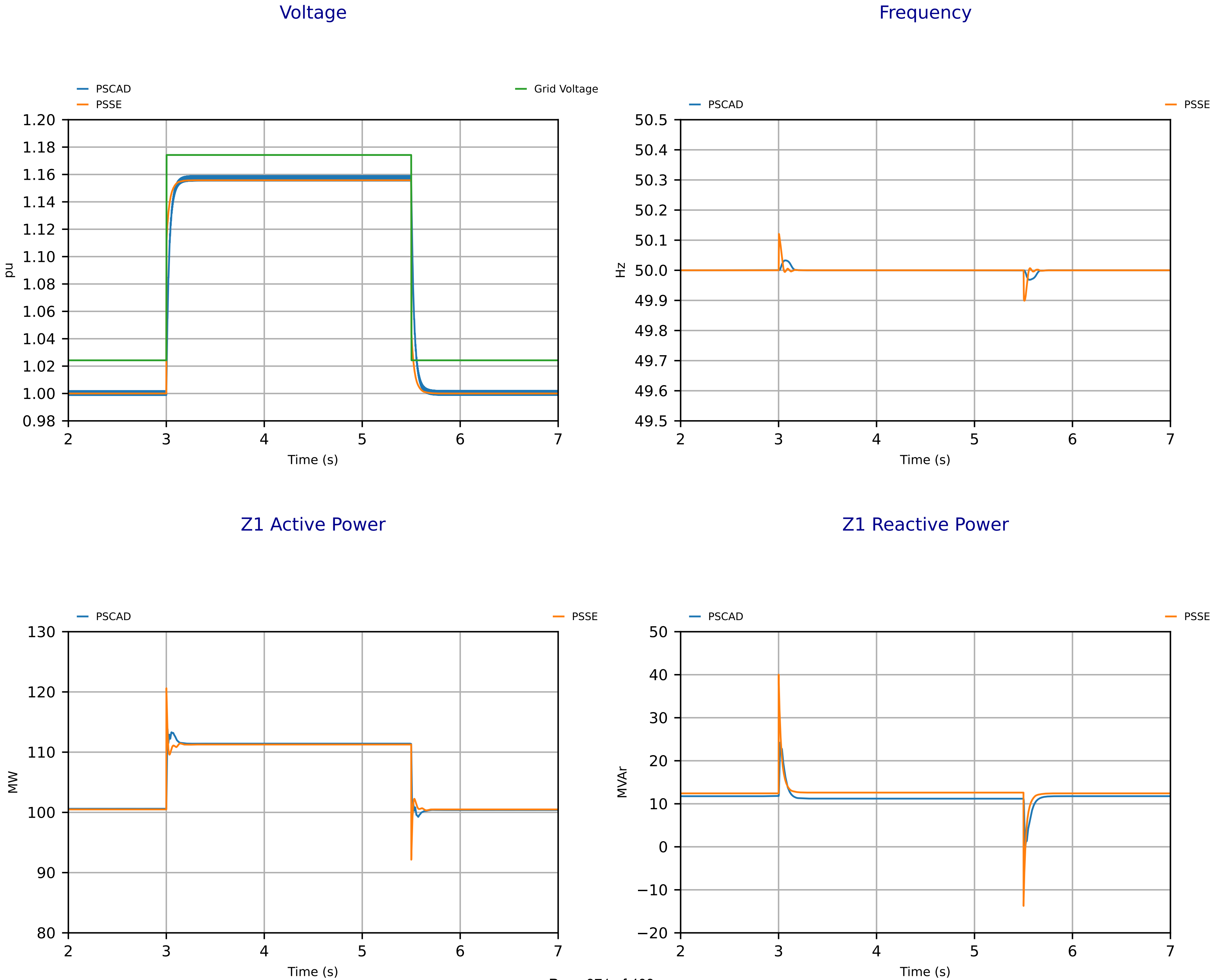
CMLD SMIB

SCR = 10, X/R = 14

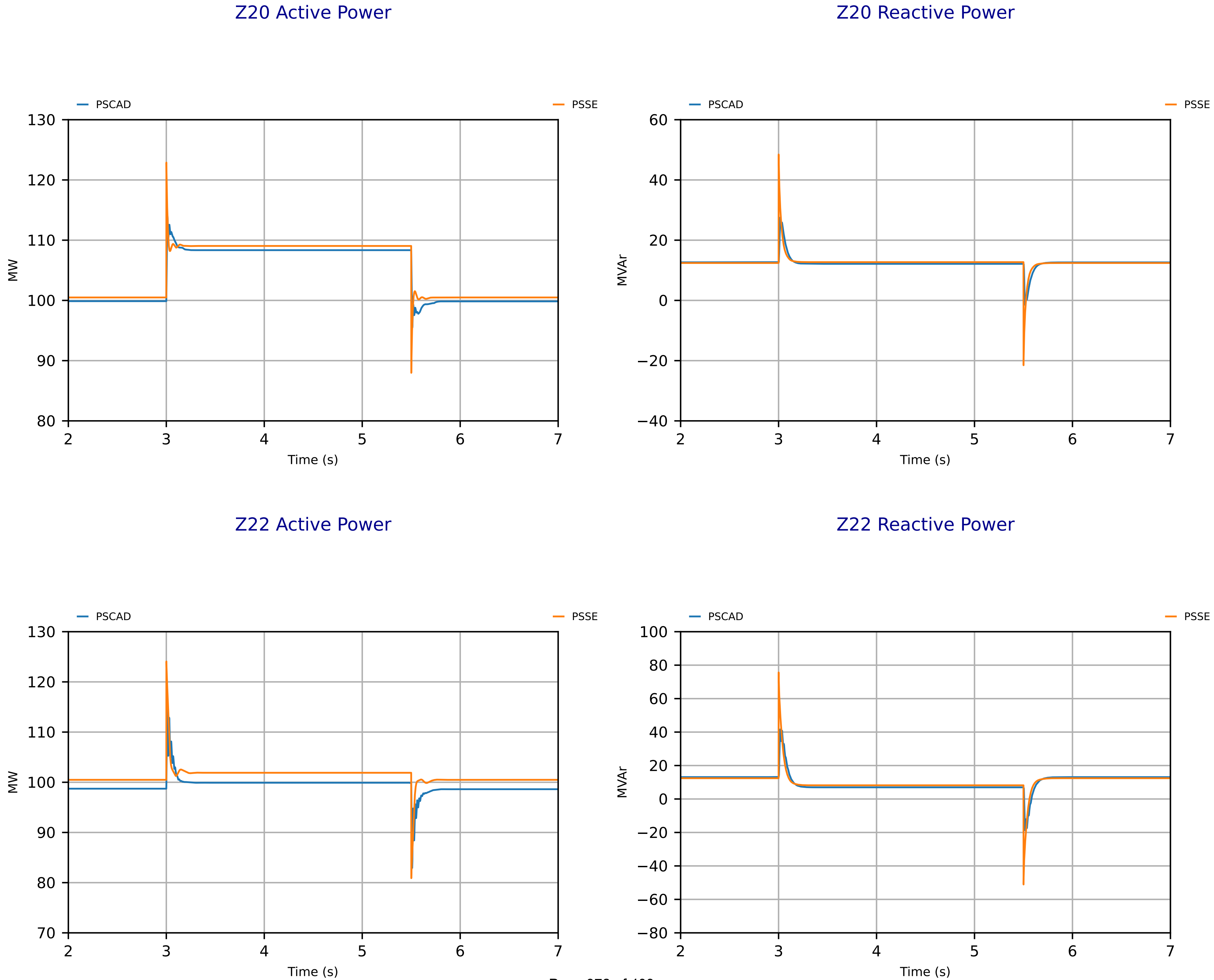
Test #4:

~115% Voltage disturbance for 2.5 s

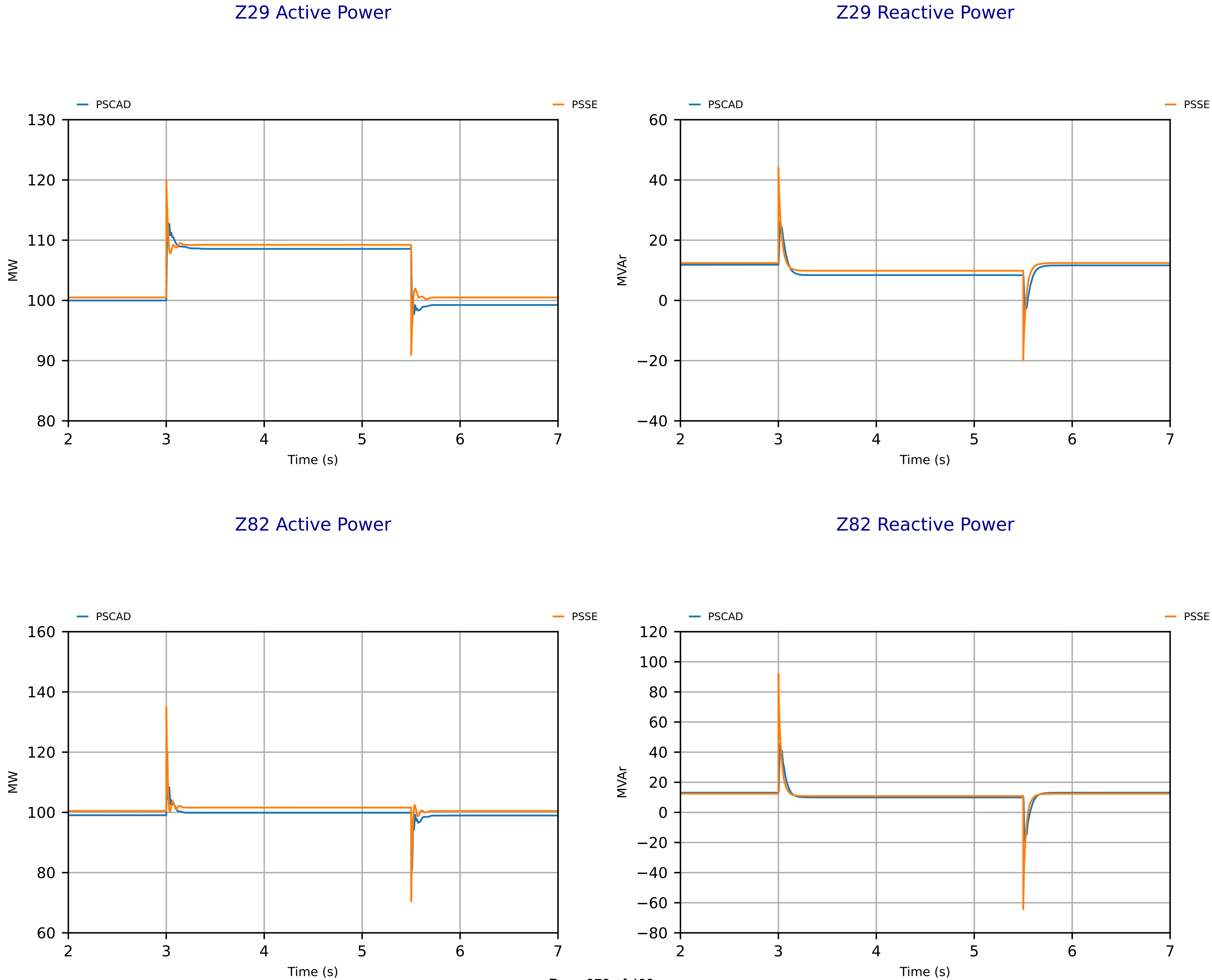
CMLD_SMIB_SCR_10_XR_14_T4_1



CMLD_SMIB_SCR_10_XR_14_T4_2

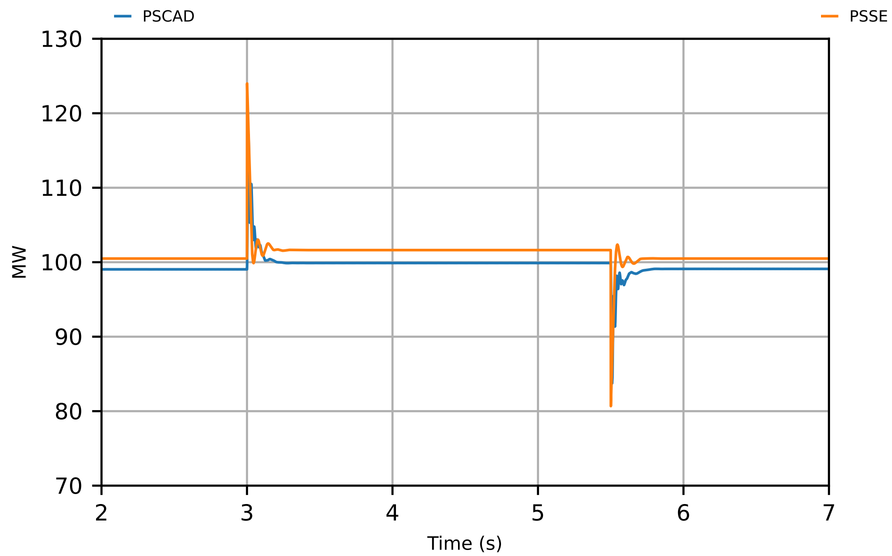


CMLD_SMIB_SCR_10_XR_14_T4_3

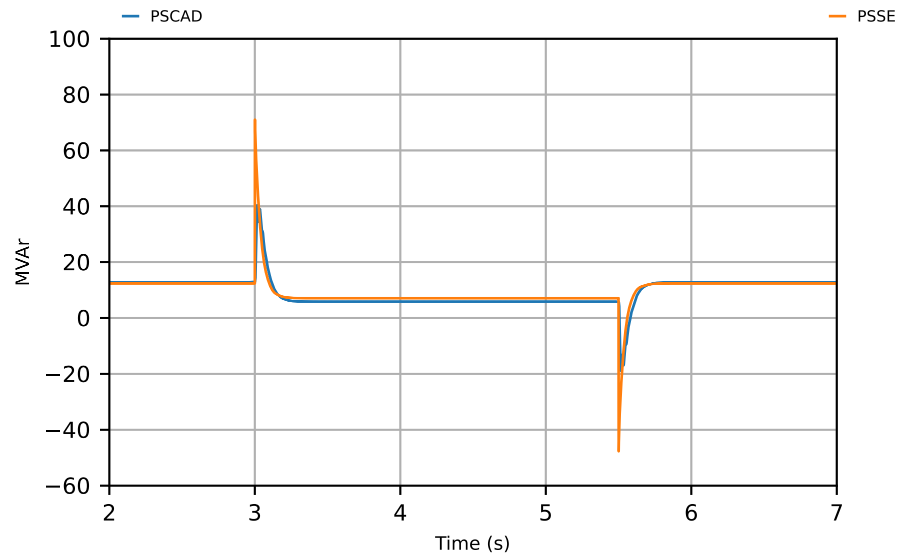


CMLD_SMIB_SCR_10_XR_14_T4_4

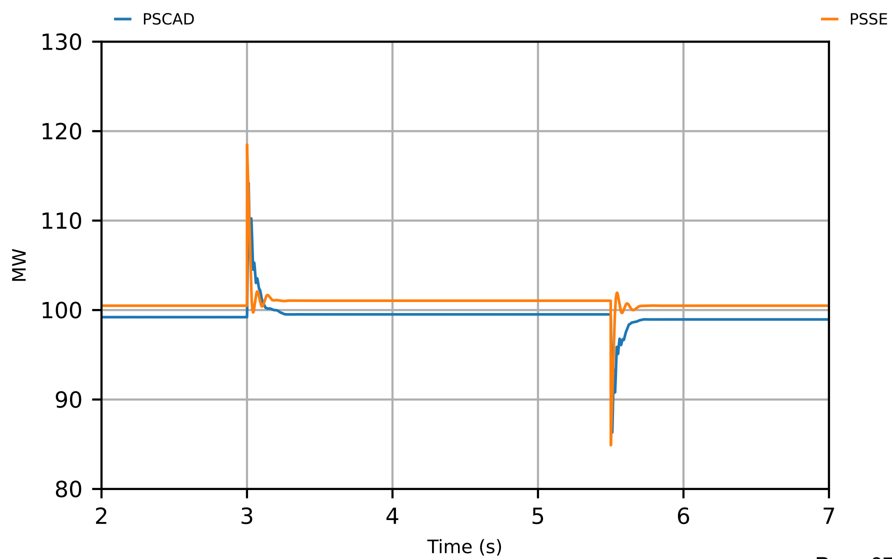
Z92 Active Power



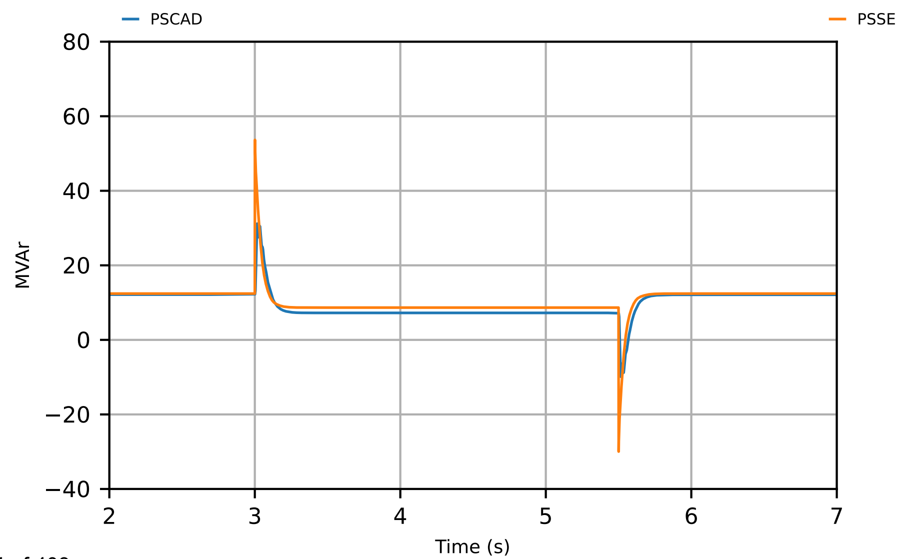
Z92 Reactive Power



Z224 Active Power



Z224 Reactive Power



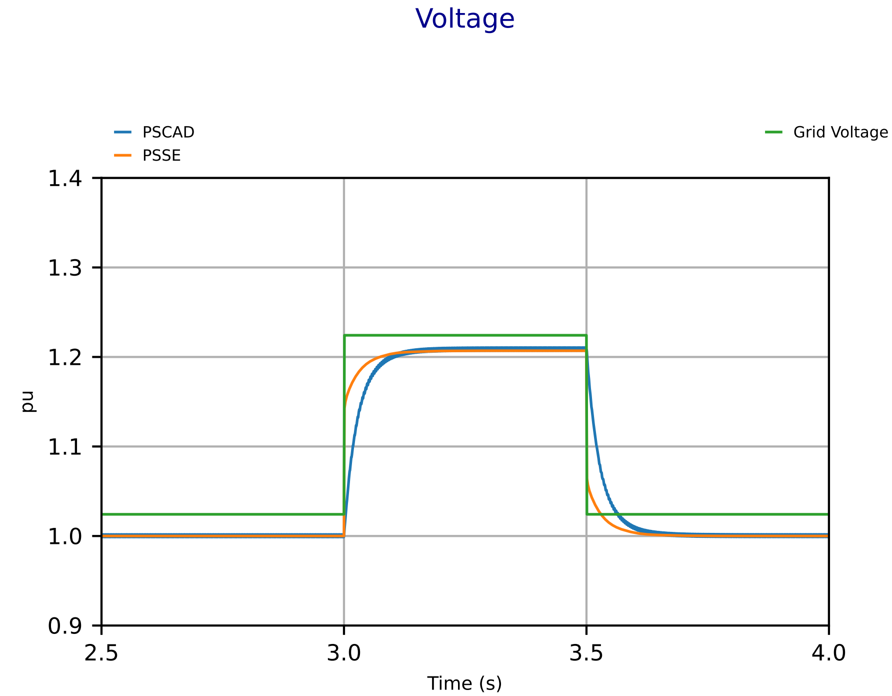
CMLD SMIB

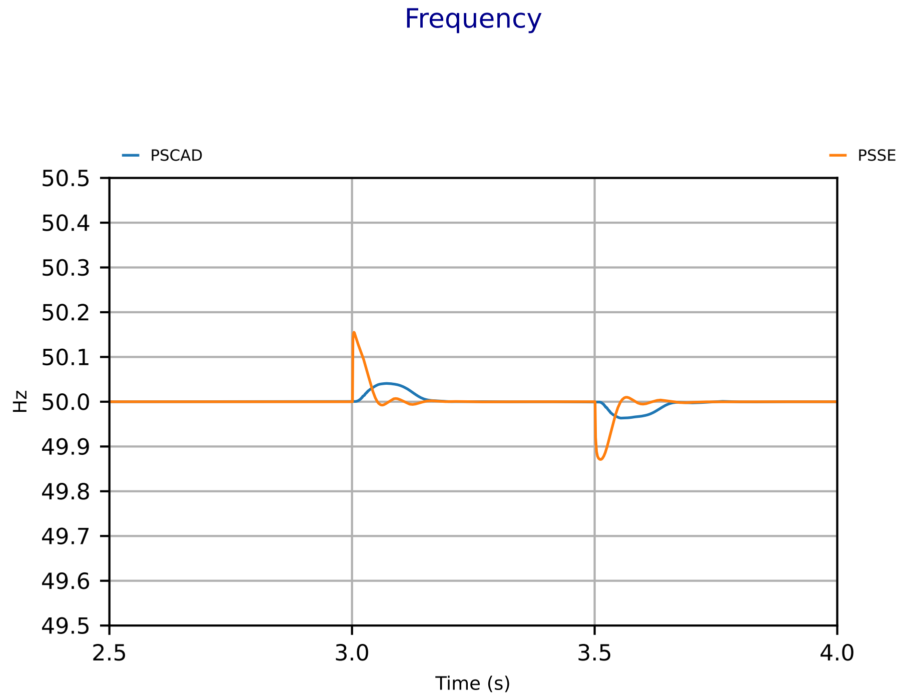
SCR = 10, X/R = 14

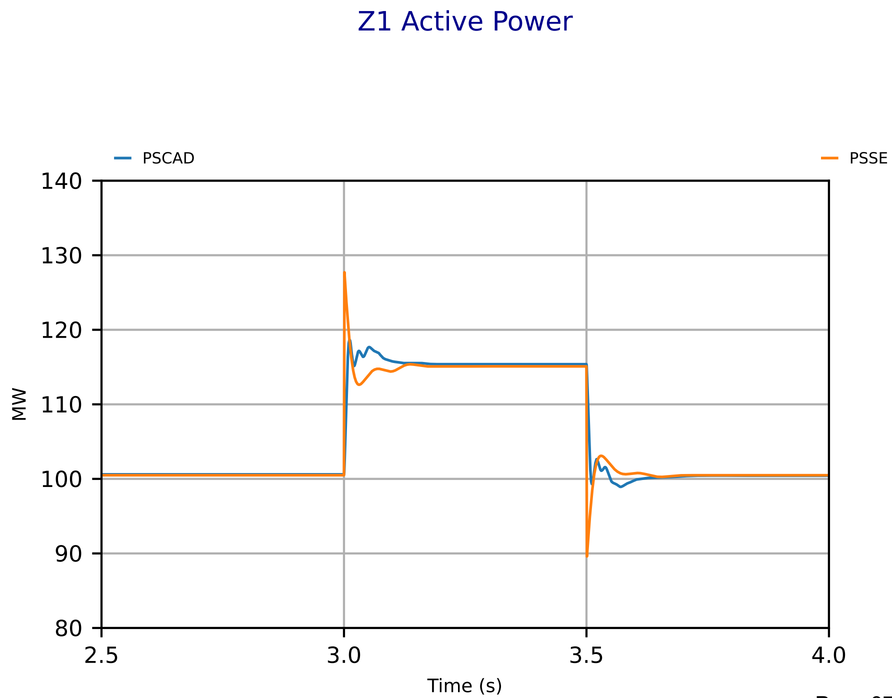
Test #5:

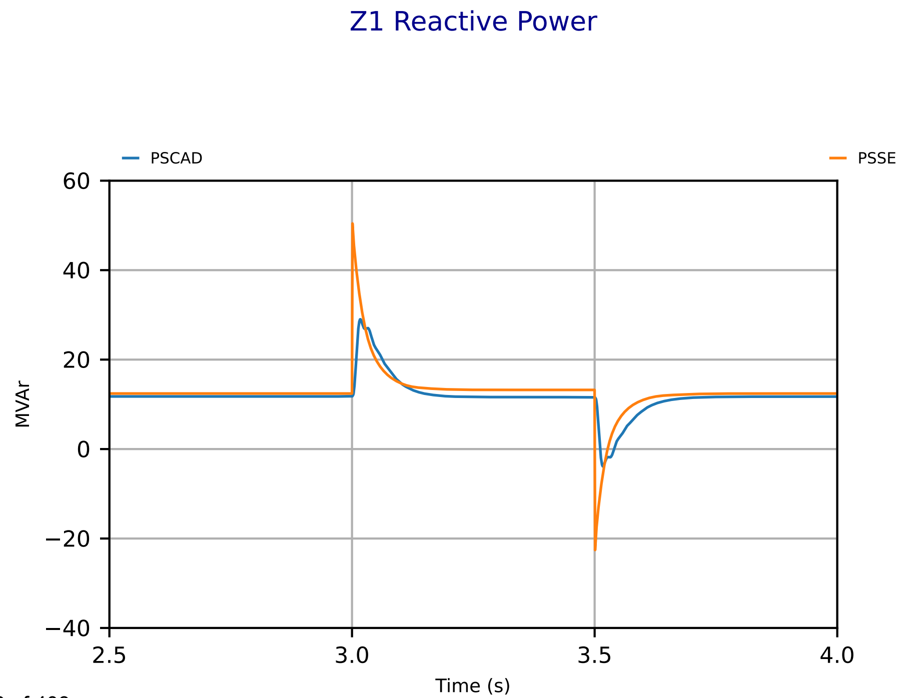
~120% Voltage disturbance for 500 ms

CMLD_SMIB_SCR_10_XR_14_T5_1

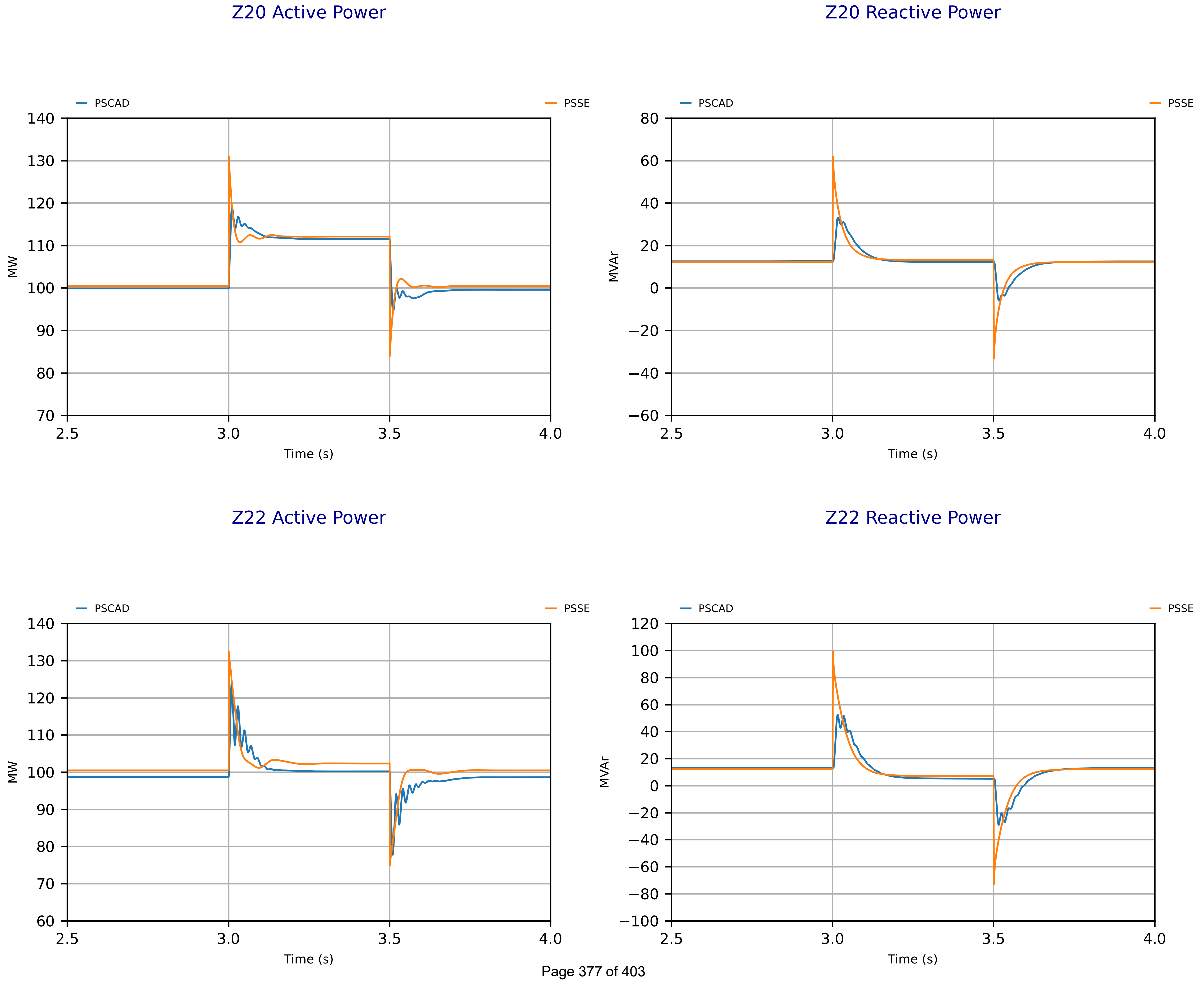




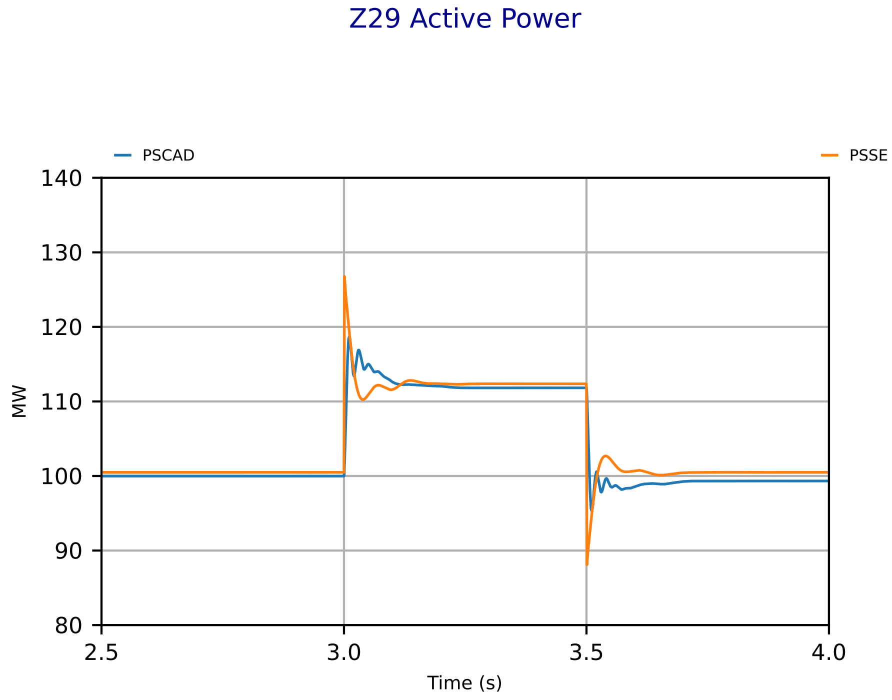


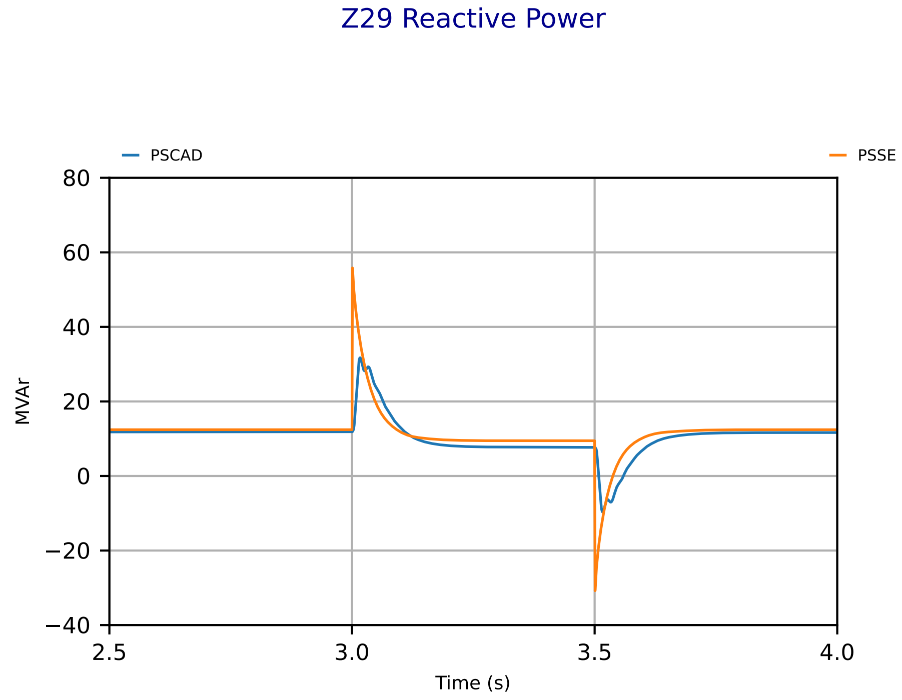


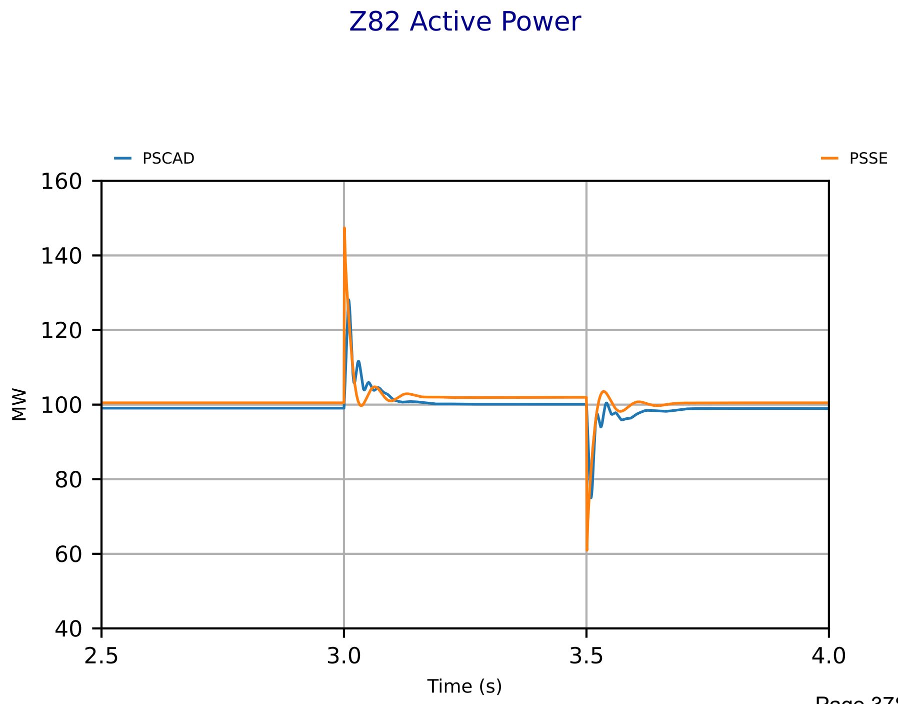
CMLD_SMIB_SCR_10_XR_14_T5_2

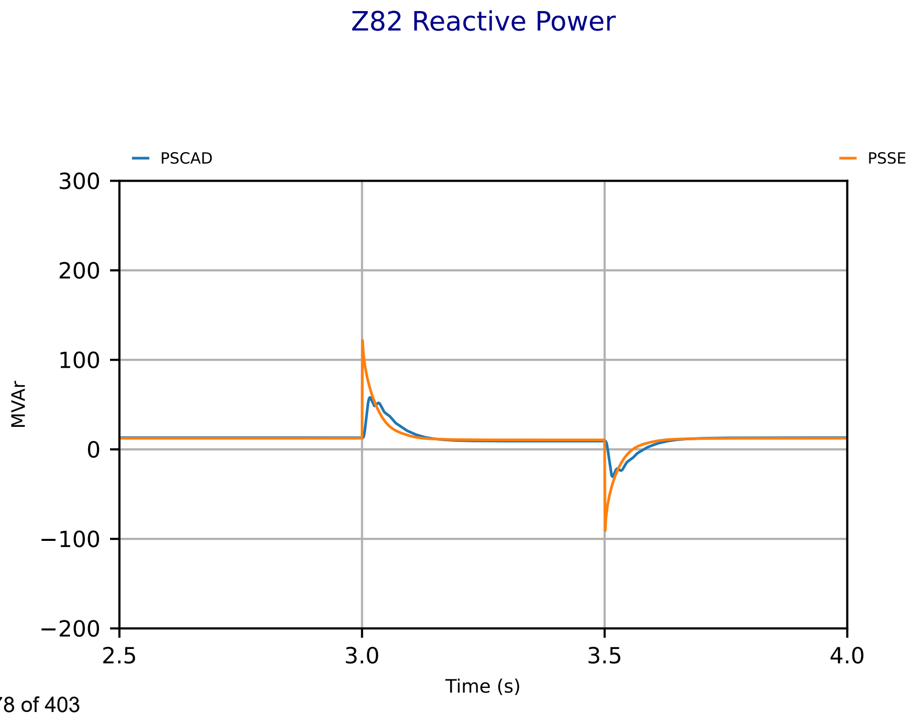


CMLD_SMIB_SCR_10_XR_14_T5_3

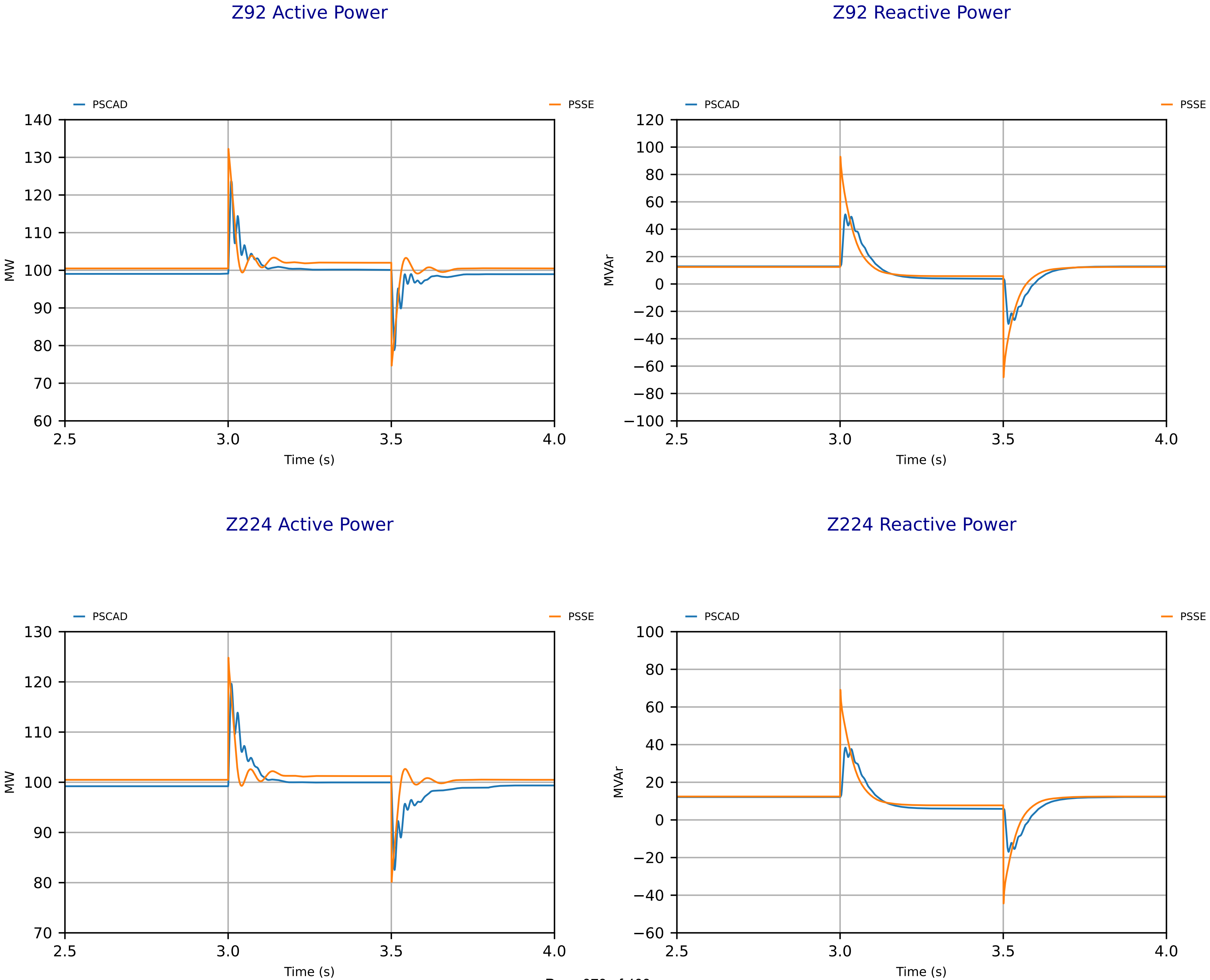








CMLD_SMIB_SCR_10_XR_14_T5_4



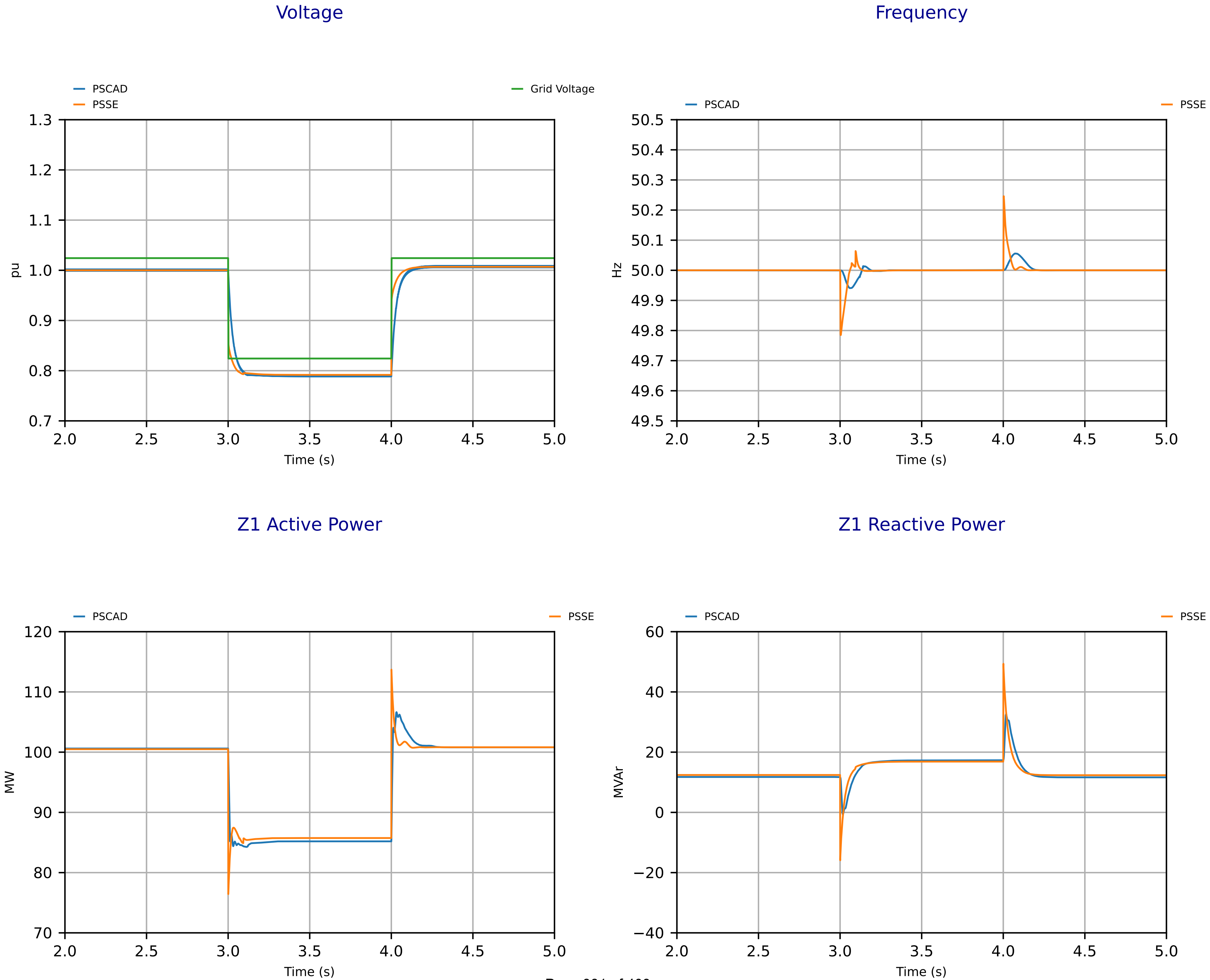
CMLD SMIB

SCR = 10, X/R = 14

Test #6:

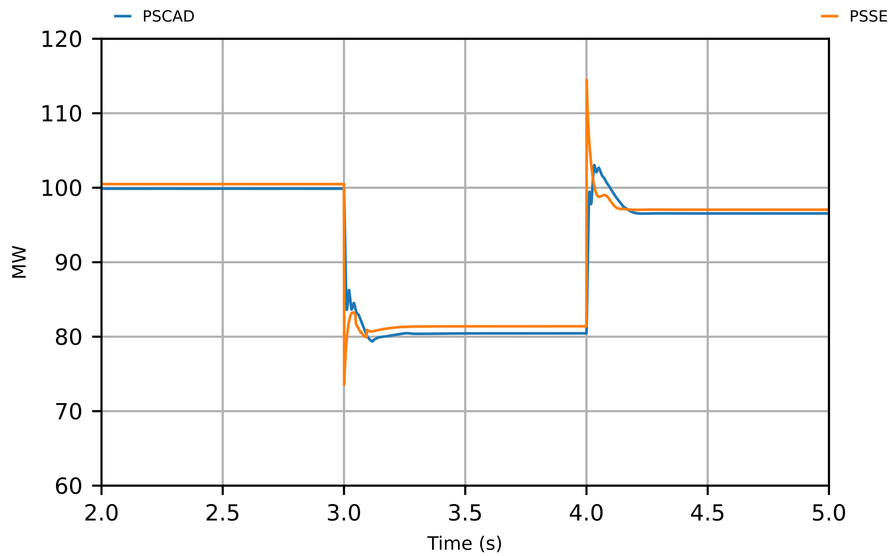
~80% Voltage disturbance for 1 sec

CMLD_SMIB_SCR_10_XR_14_T6_1

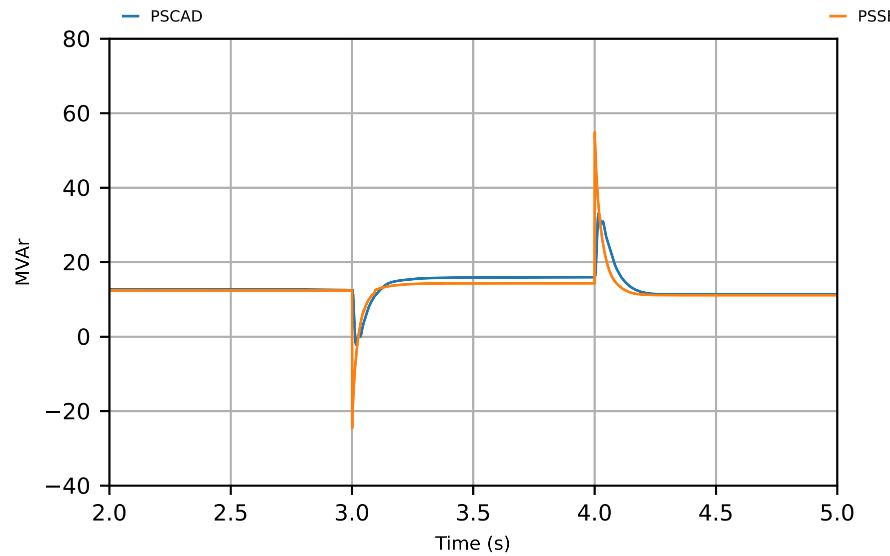


CMLD_SMIB_SCR_10_XR_14_T6_2

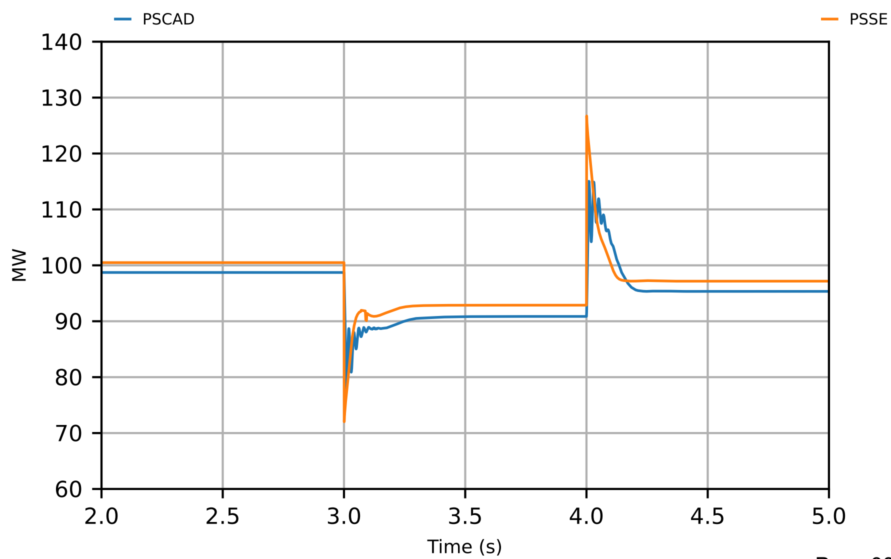
Z20 Active Power



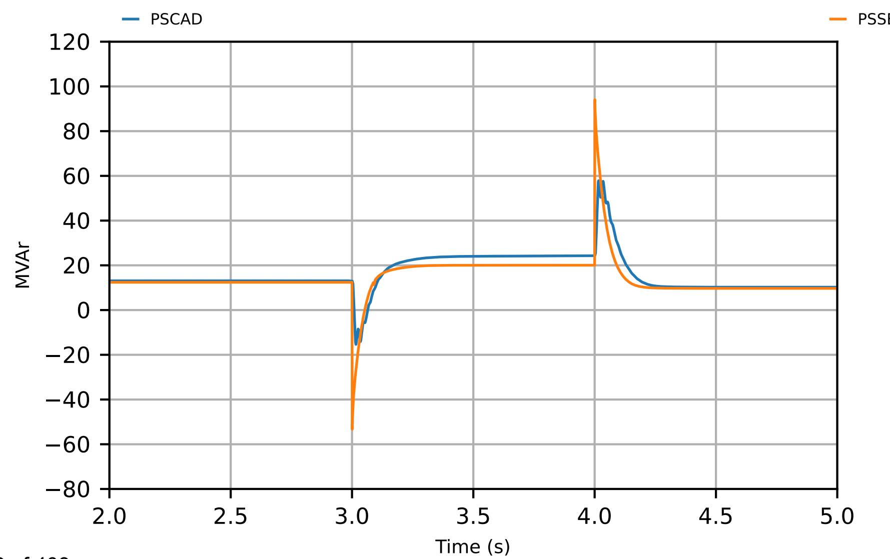
Z20 Reactive Power

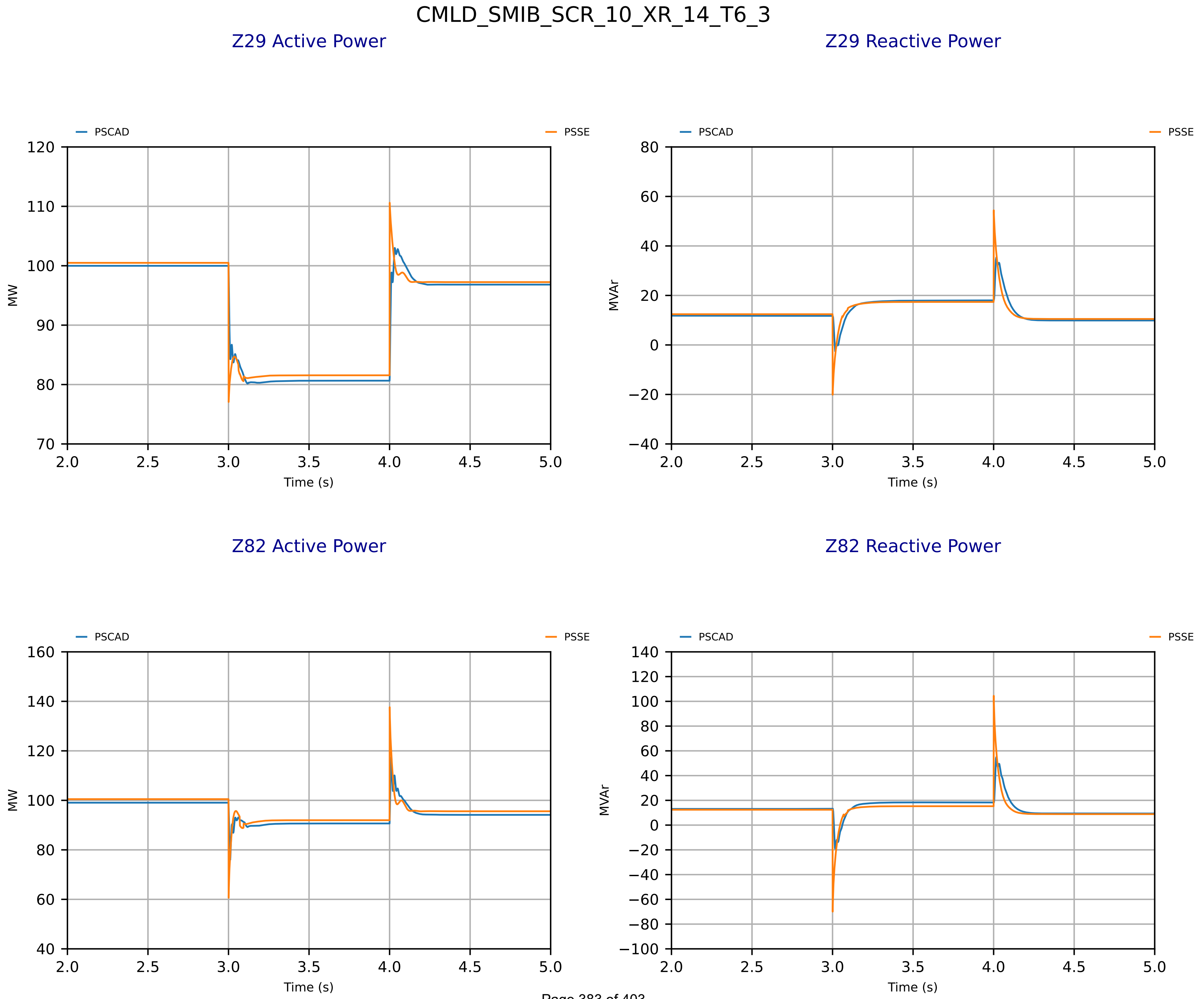


Z22 Active Power

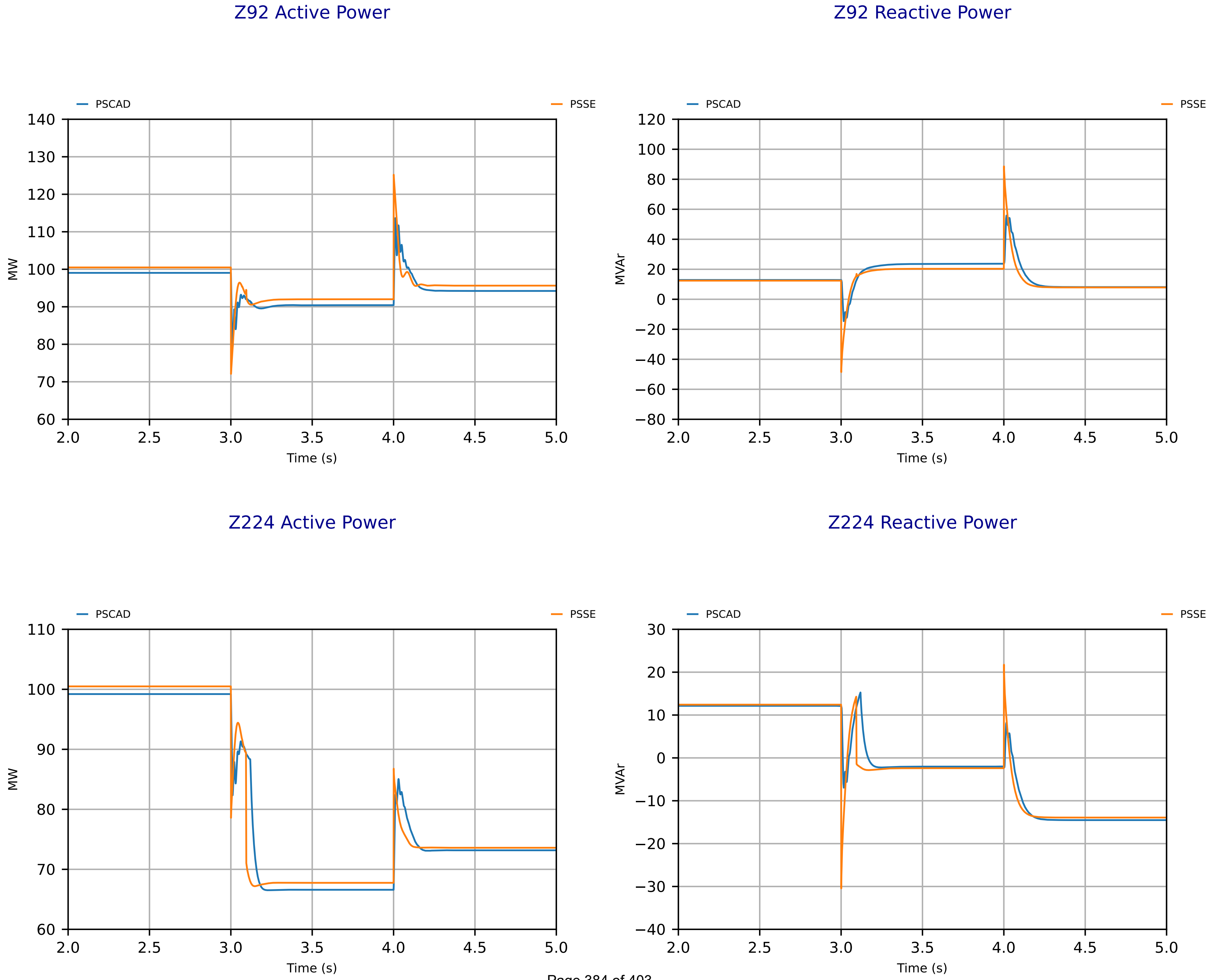


Z22 Reactive Power




CMLD_SMIB_SCR_10_XR_14_T6_3
Z29 Active Power
Z29 Reactive Power
Z82 Active Power
Z82 Reactive Power
PSCAD
PSSE
MW
MVAr
Time (s)

CMLD_SMIB_SCR_10_XR_14_T6_4



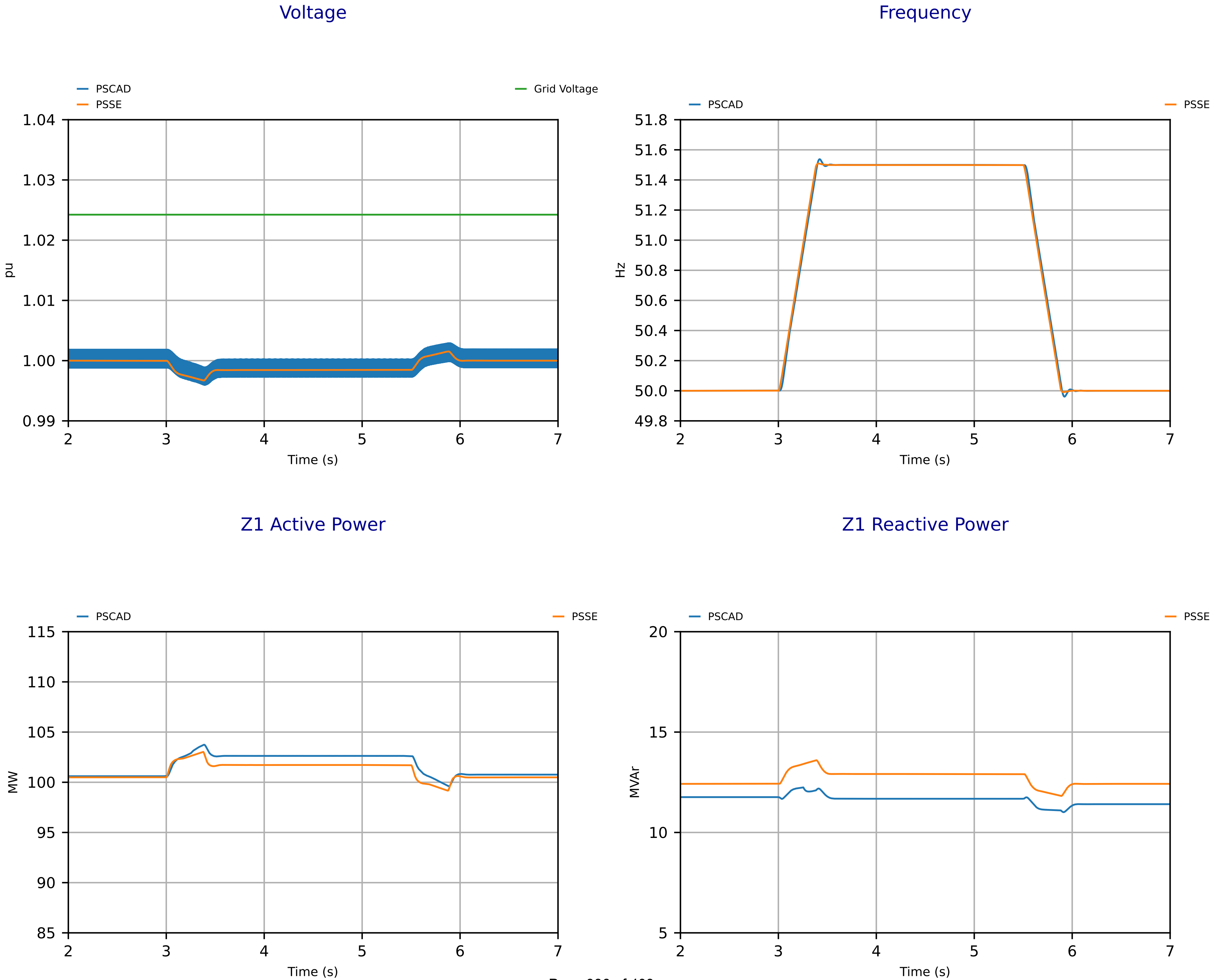
CMLD SMIB

SCR = 10, X/R = 14

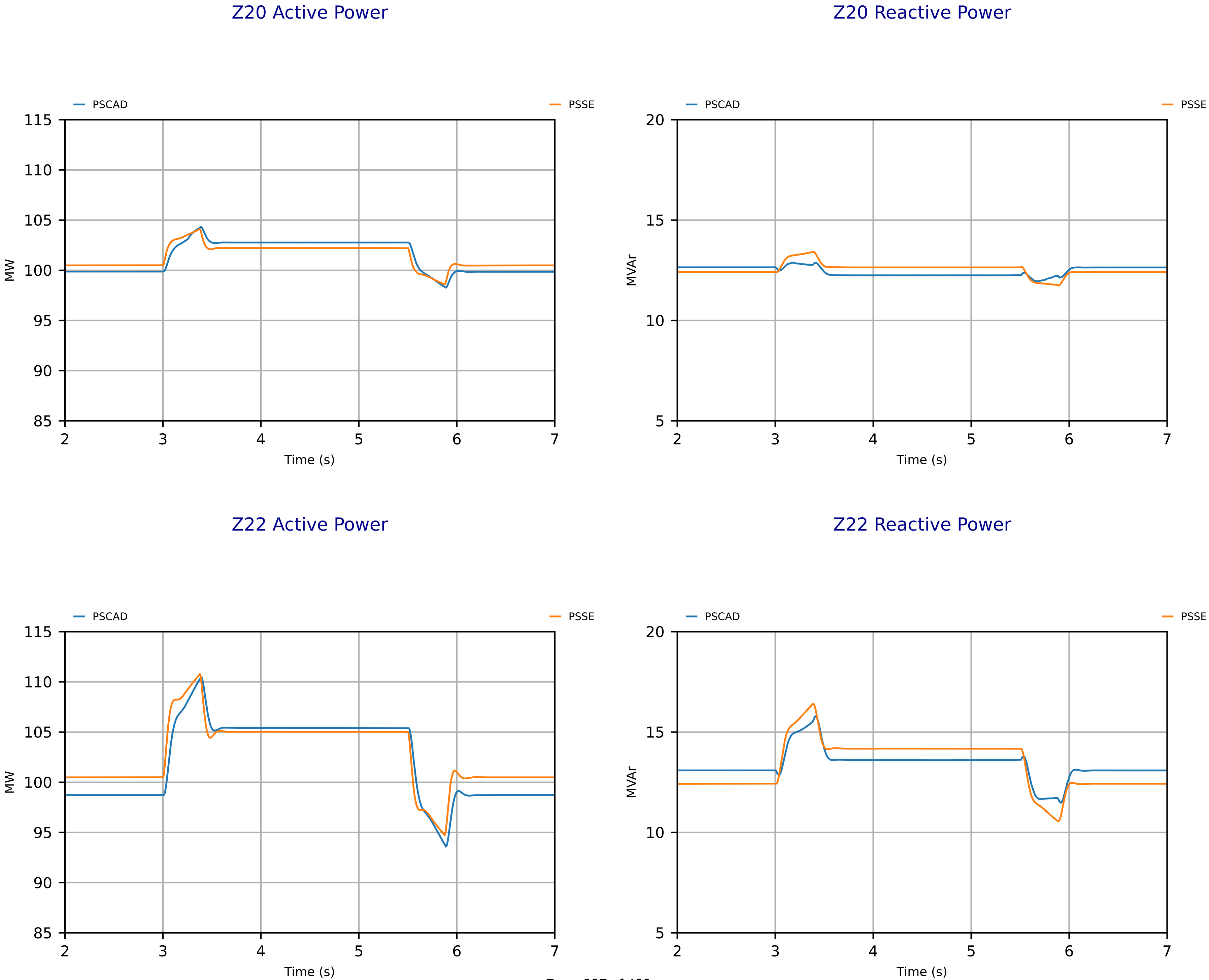
Test #7:

51.5 Hz frequency step for 2.5 sec (4 Hz/s)

CMLD_SMIB_SCR_10_XR_14_T7_1

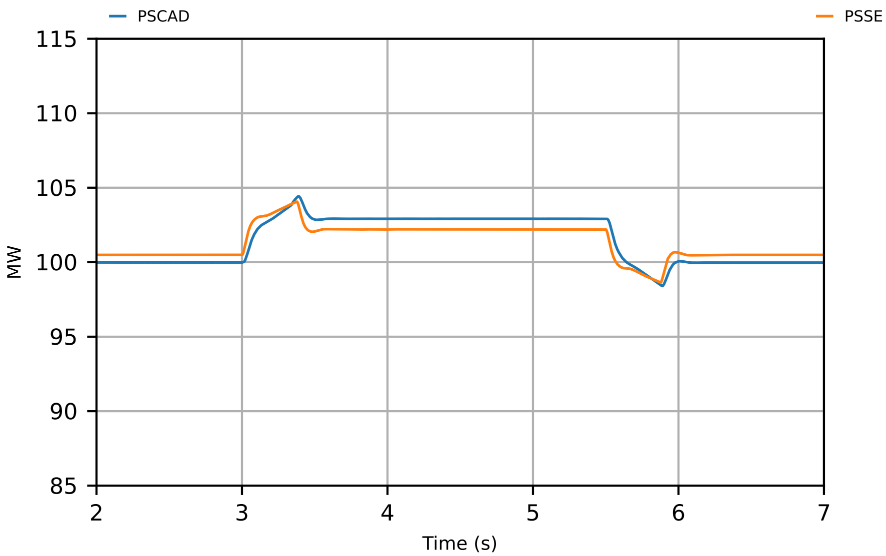


CMLD_SMIB_SCR_10_XR_14_T7_2

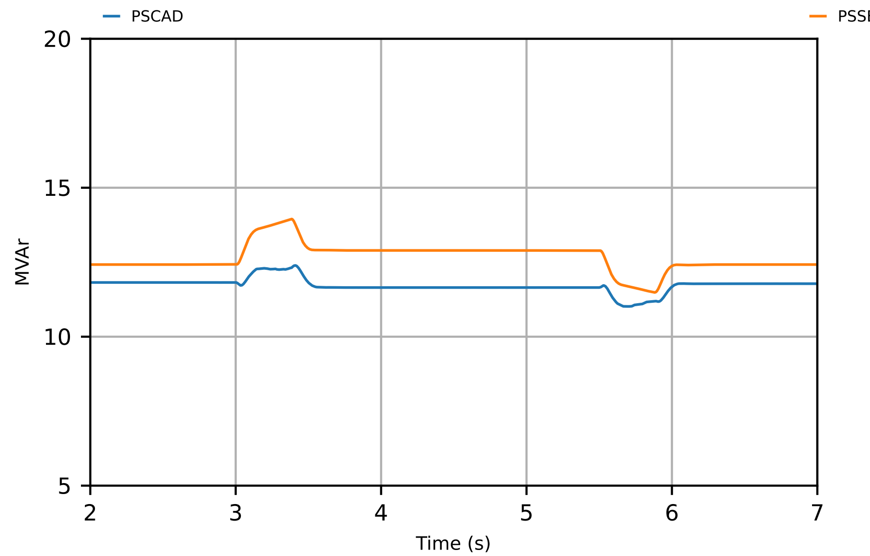


CMLD_SMIB_SCR_10_XR_14_T7_3

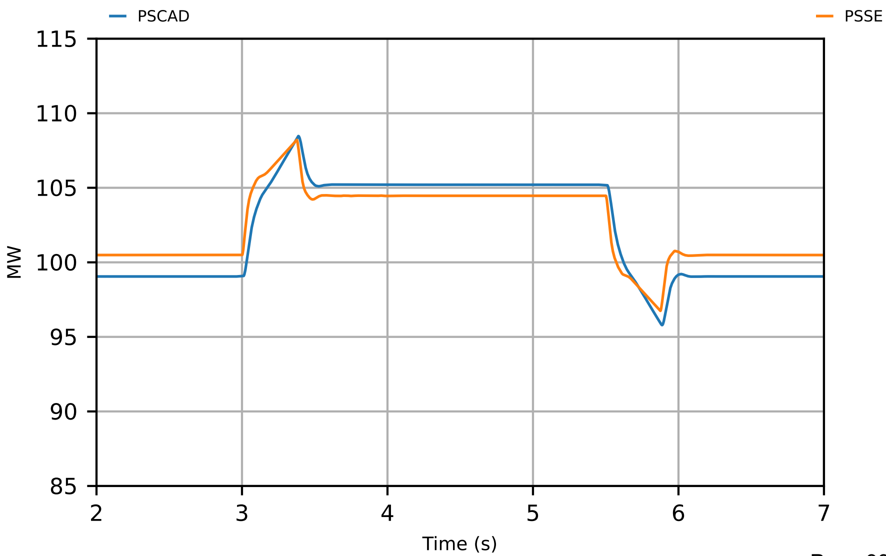
Z29 Active Power



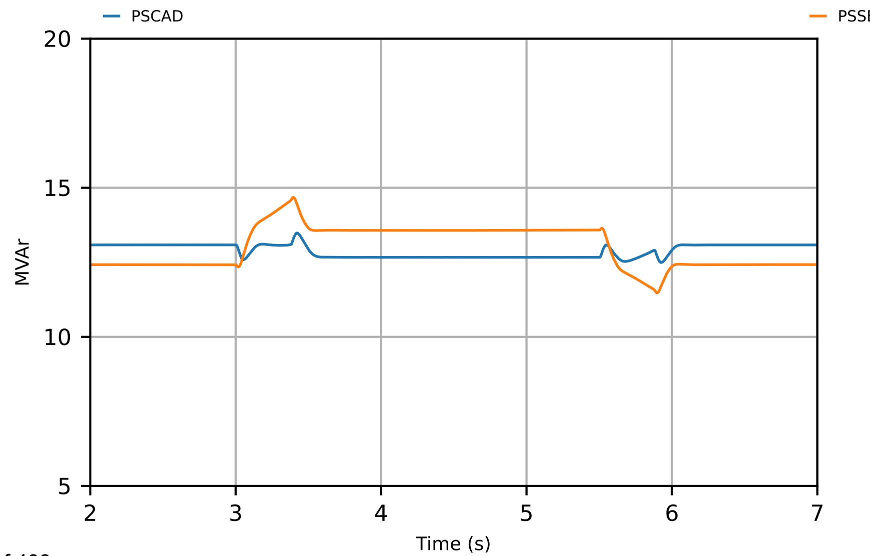
Z29 Reactive Power



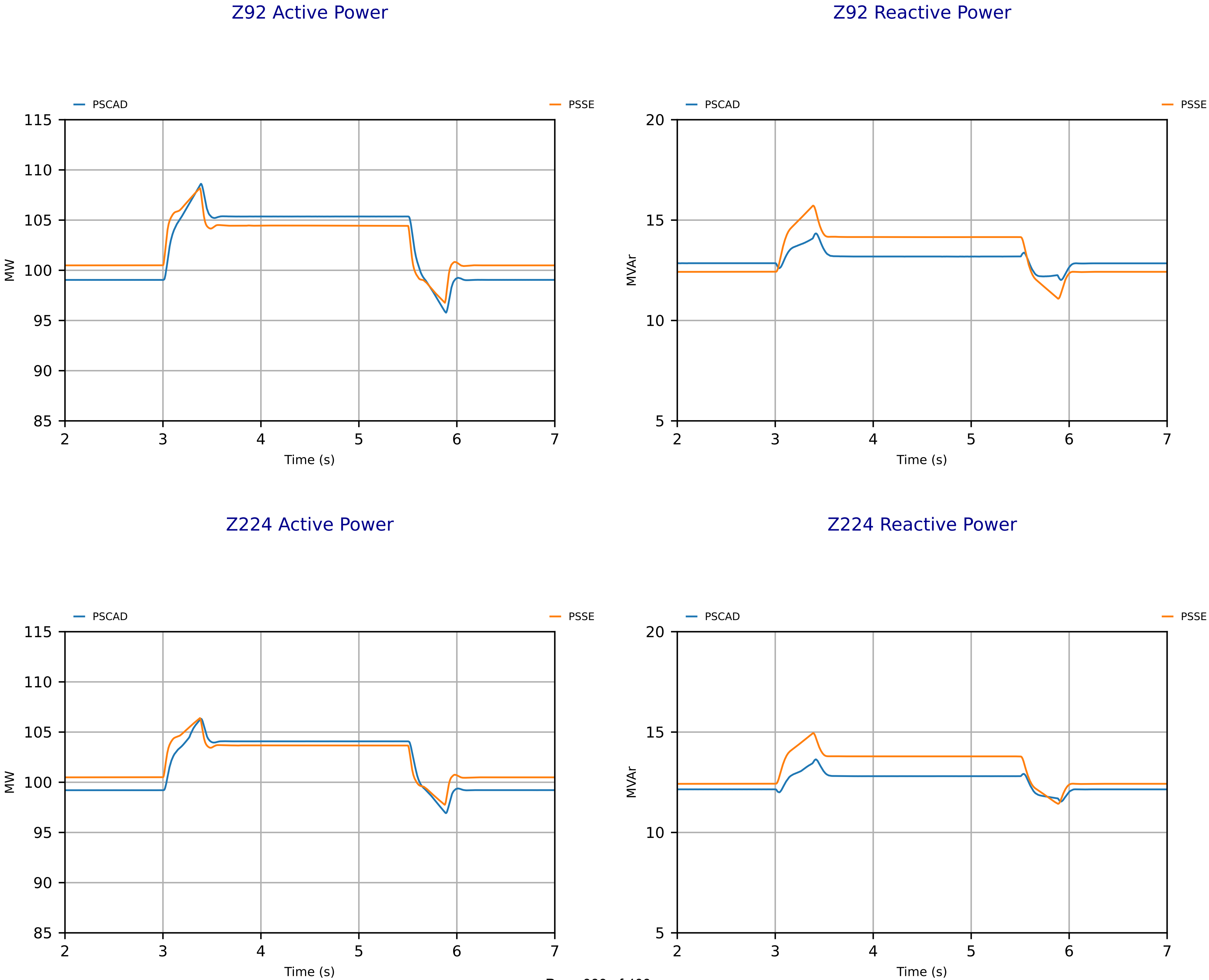
Z82 Active Power



Z82 Reactive Power



CMLD_SMIB_SCR_10_XR_14_T7_4



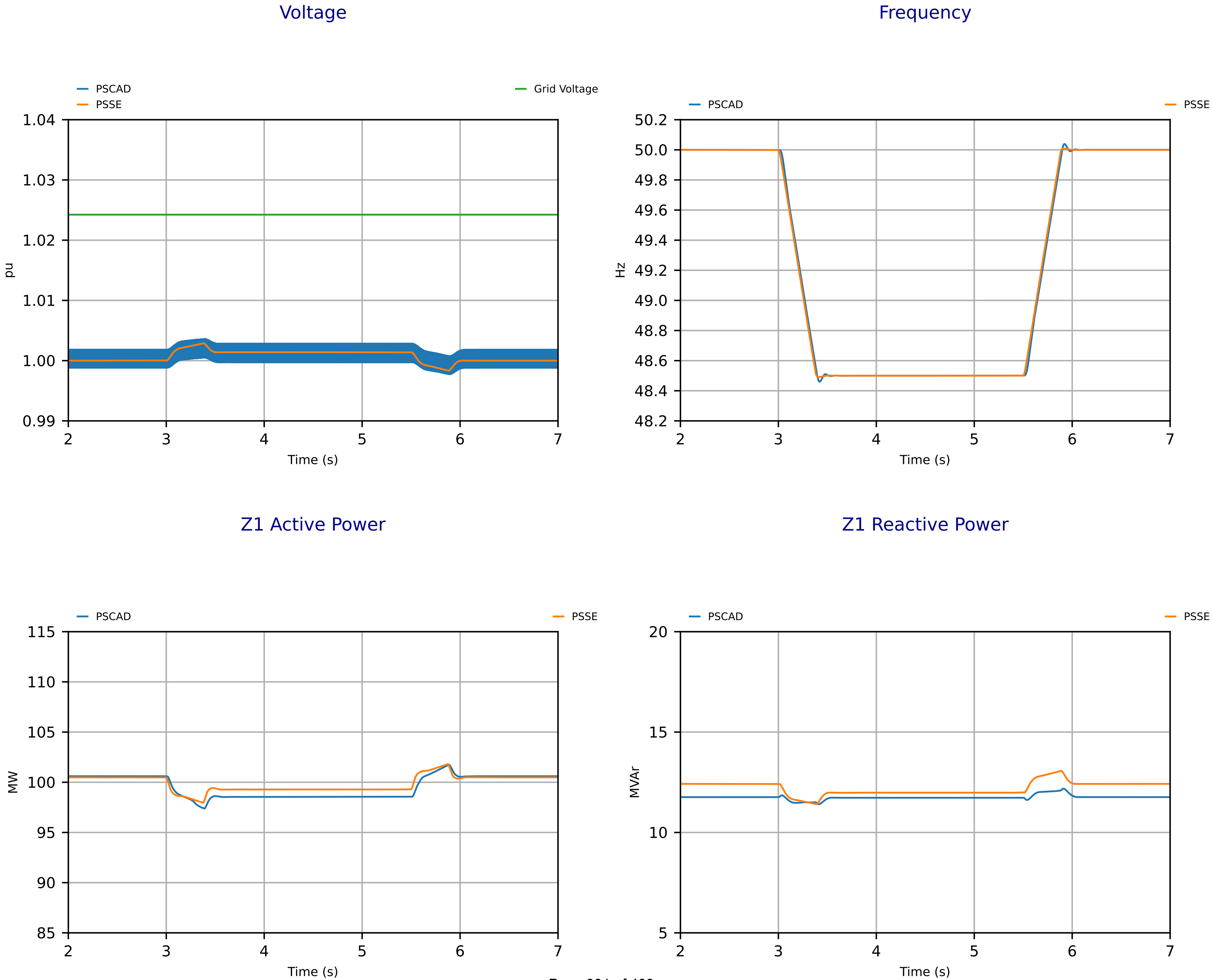
CMLD SMIB

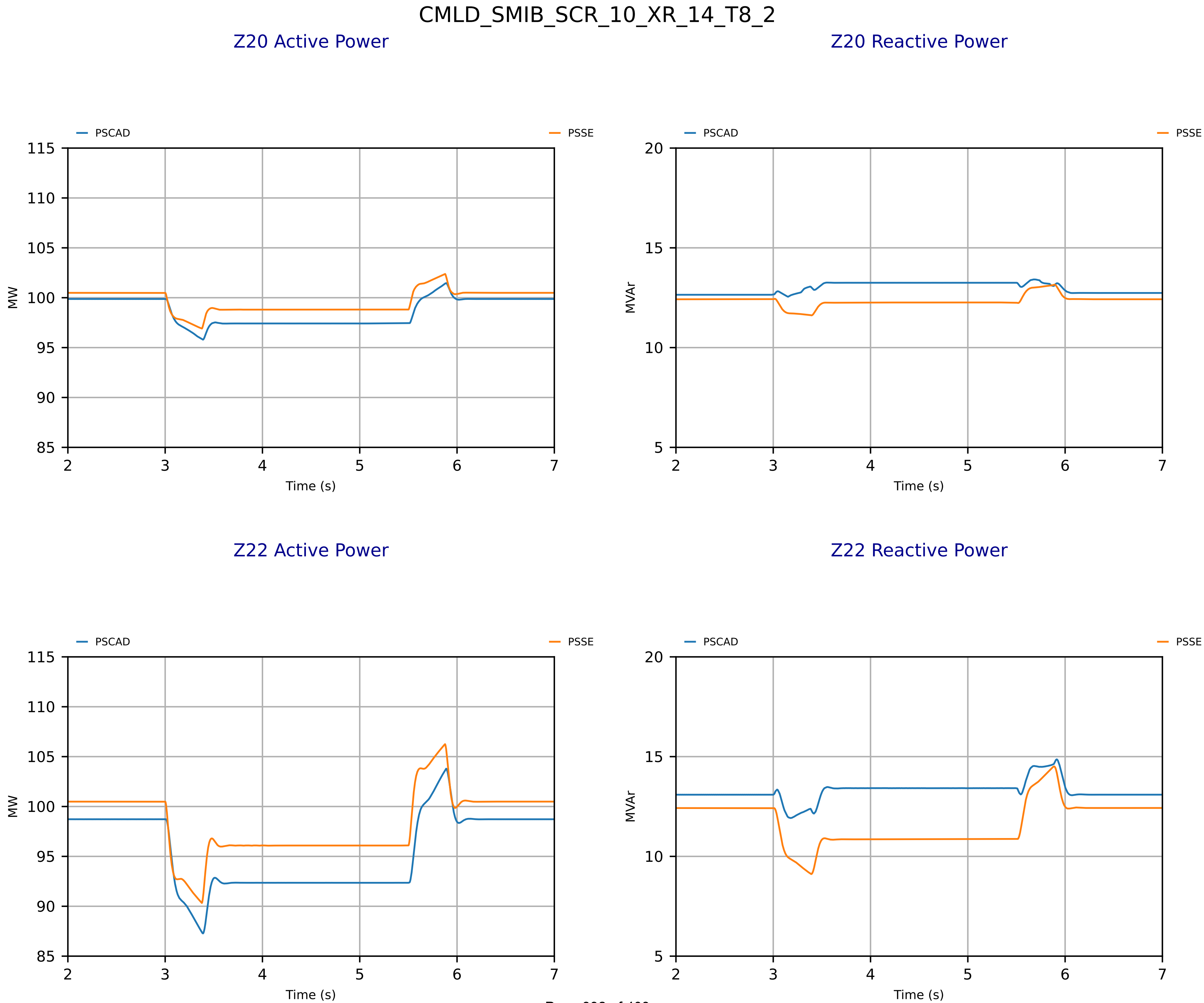
SCR = 10, X/R = 14

Test #8:

48.5 Hz frequency step for 2.5 sec (4 Hz/s)

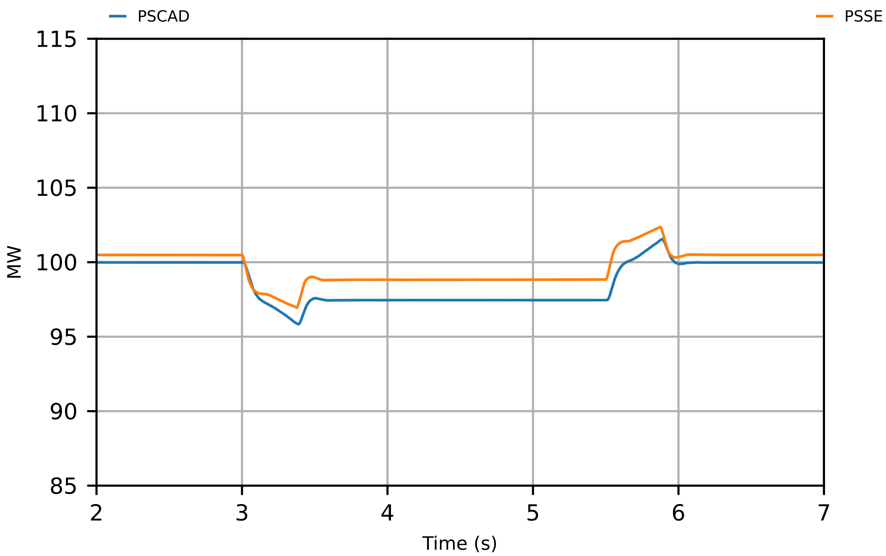
CMLD_SMIB_SCR_10_XR_14_T8_1



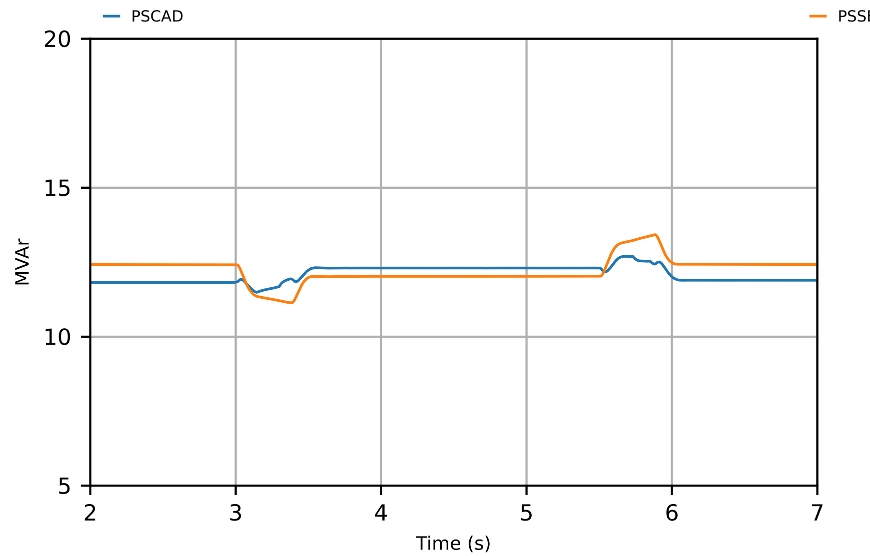

CMLD_SMIB_SCR_10_XR_14_T8_2
Z20 Active Power
Z20 Reactive Power
Z22 Active Power
Z22 Reactive Power
PSCAD
PSSE
MW
MVAr
Time (s)

CMLD_SMIB_SCR_10_XR_14_T8_3

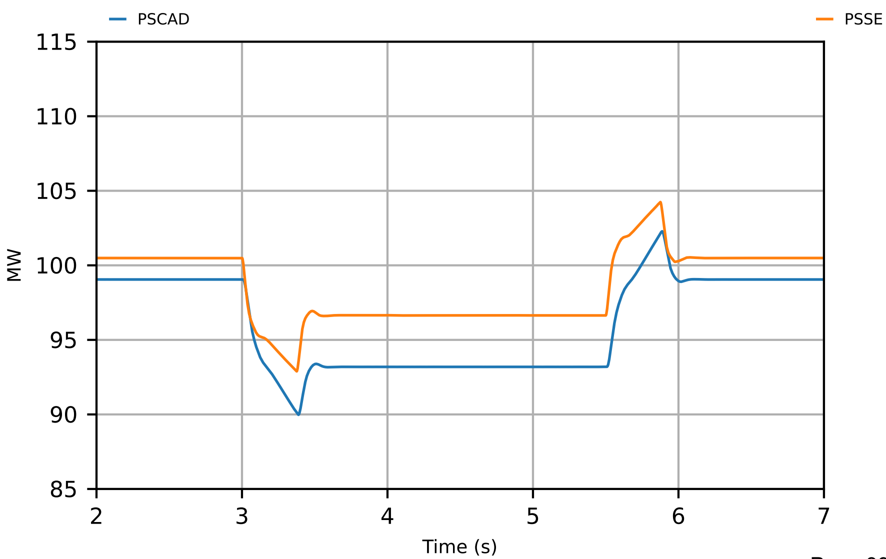
Z29 Active Power



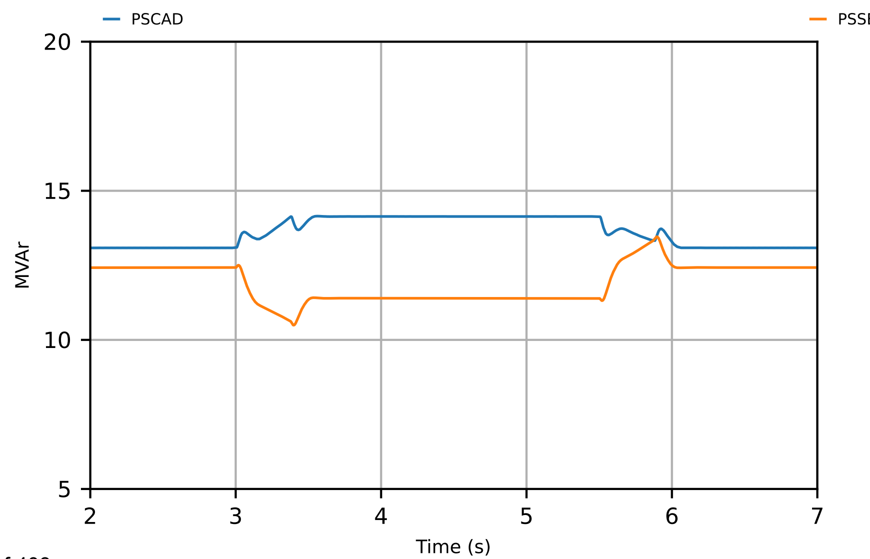
Z29 Reactive Power



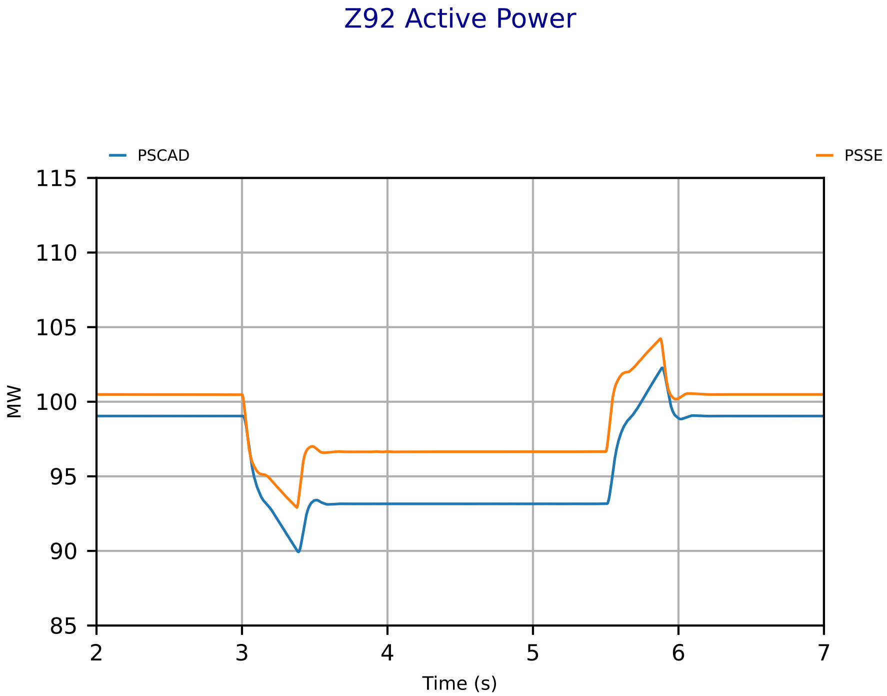
Z82 Active Power

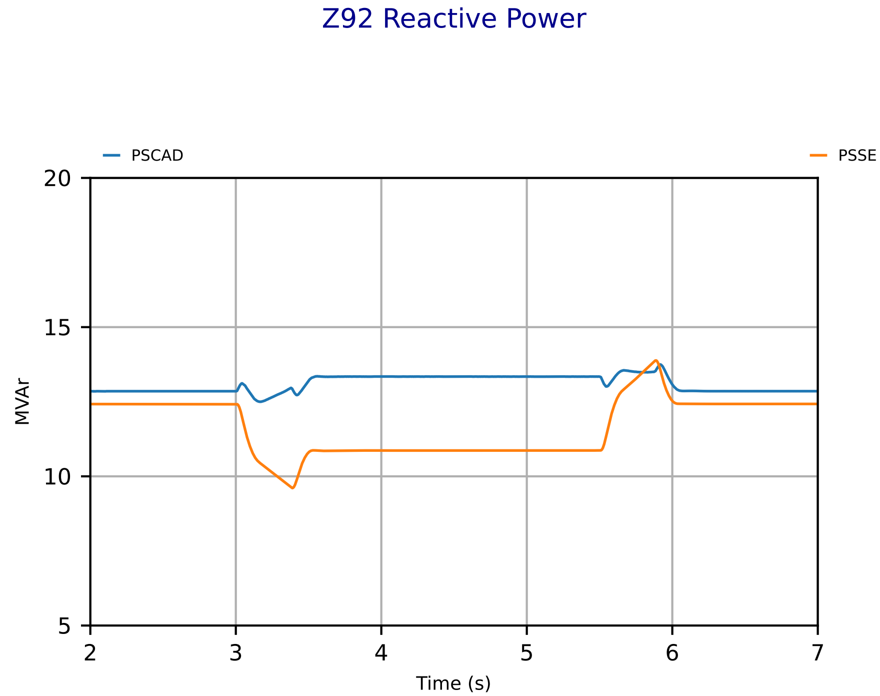


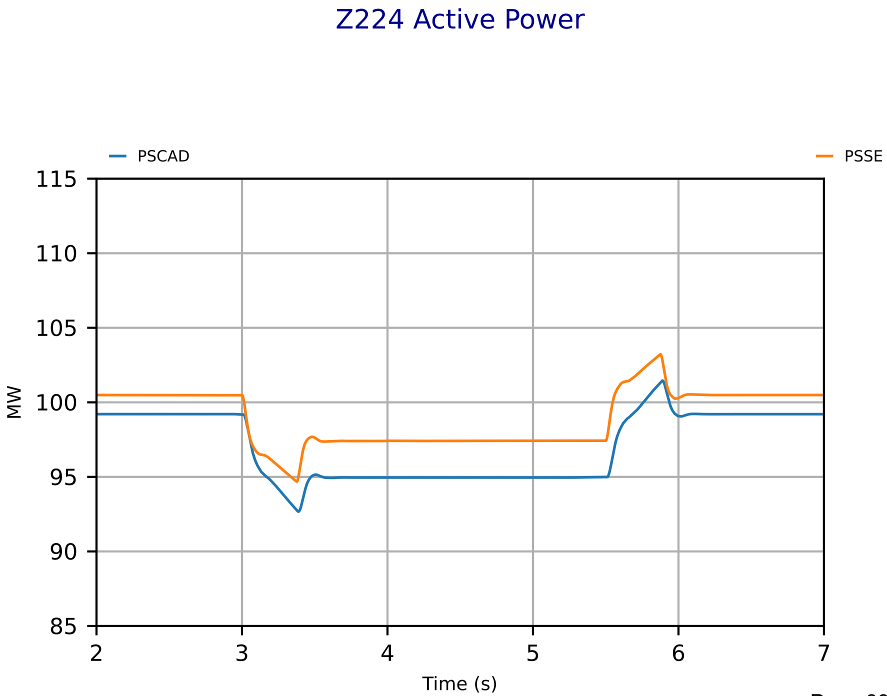
Z82 Reactive Power

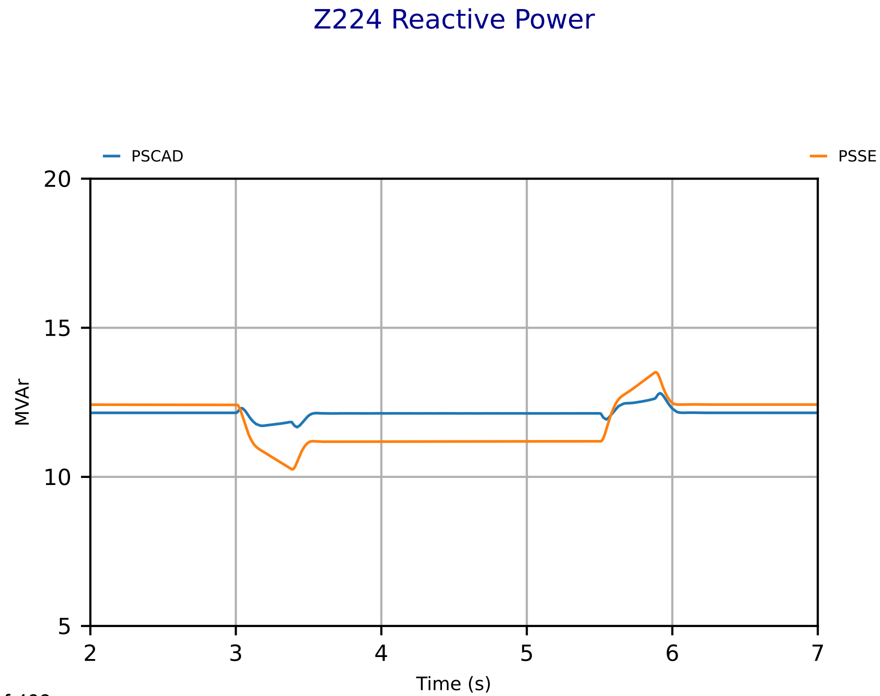


CMLD_SMIB_SCR_10_XR_14_T8_4









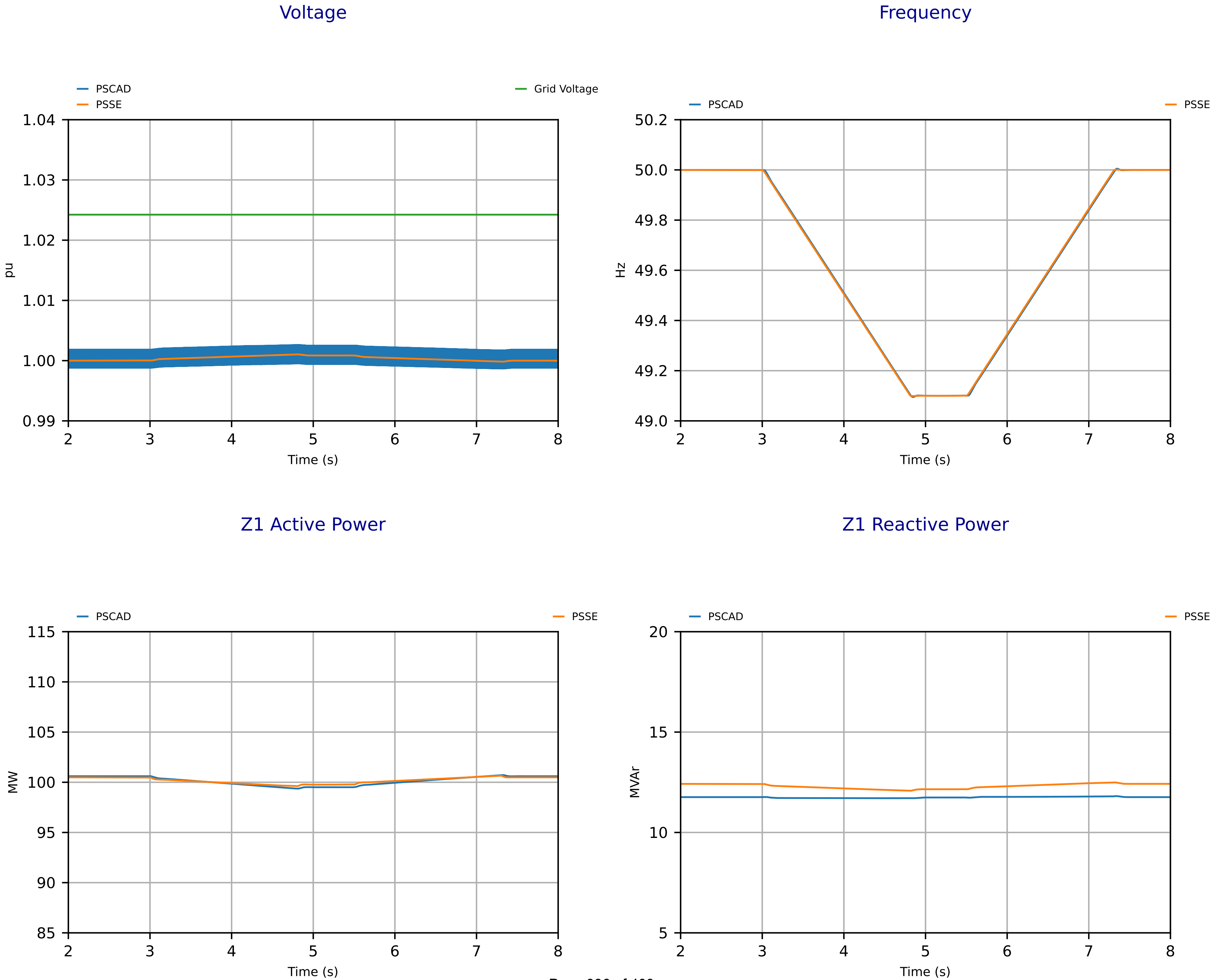
CMLD SMIB

SCR = 10, X/R = 14

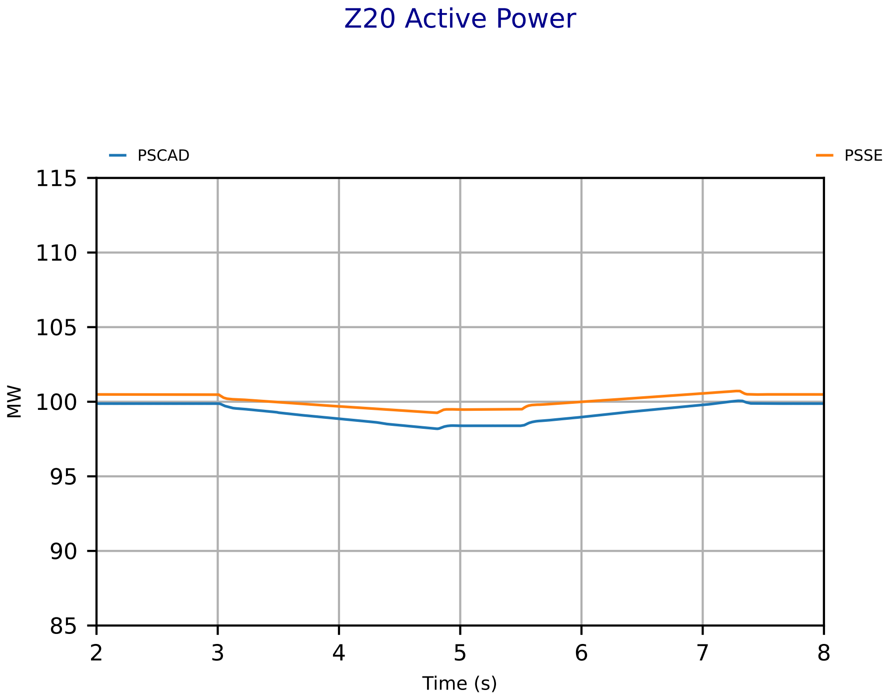
Test #9:

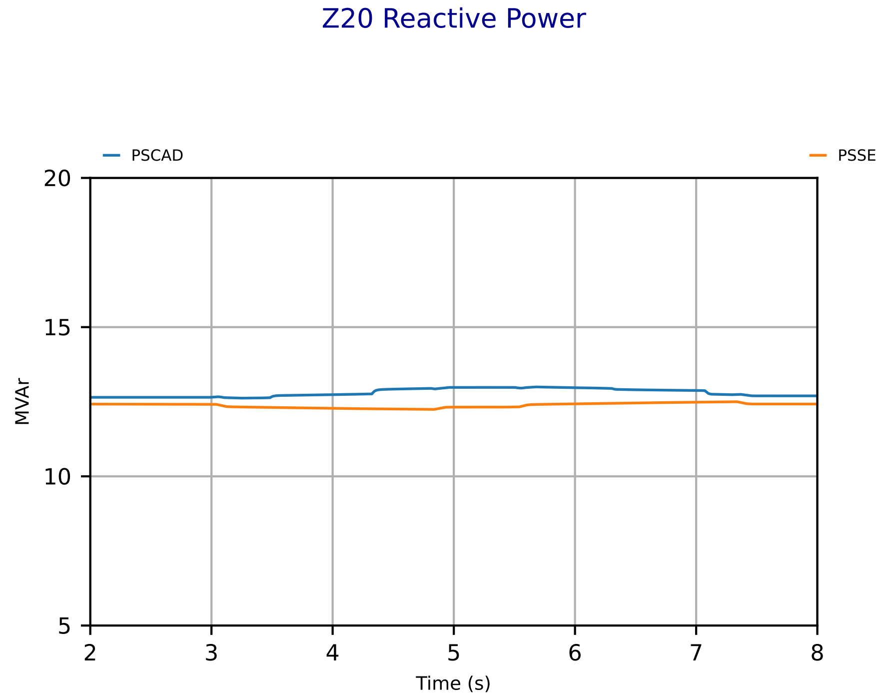
49.1 Hz slow frequency ramp (0.5 Hz/s)

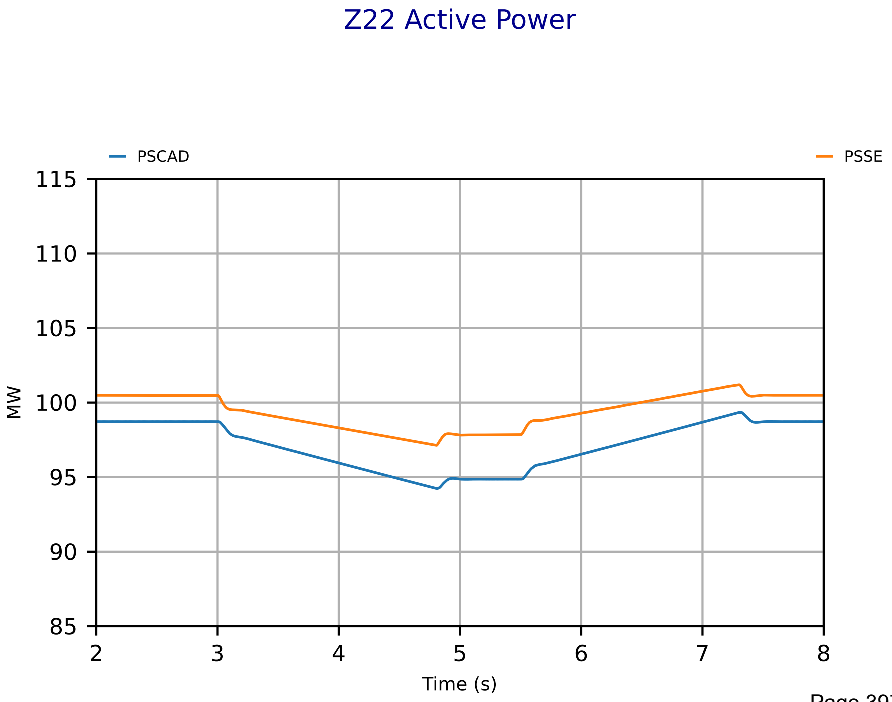
CMLD_SMIB_SCR_10_XR_14_T9_1

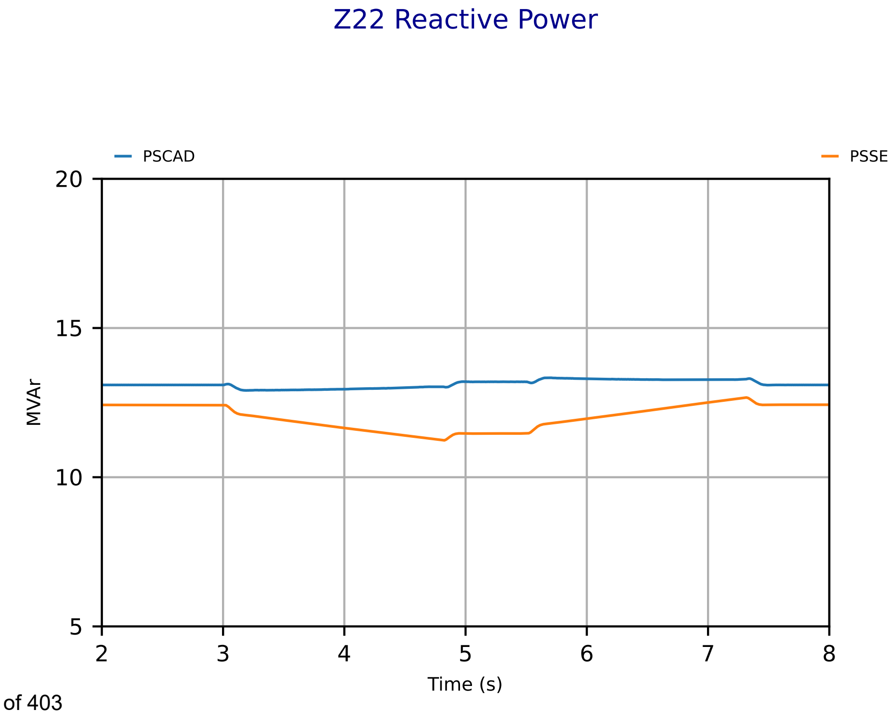


CMLD_SMIB_SCR_10_XR_14_T9_2

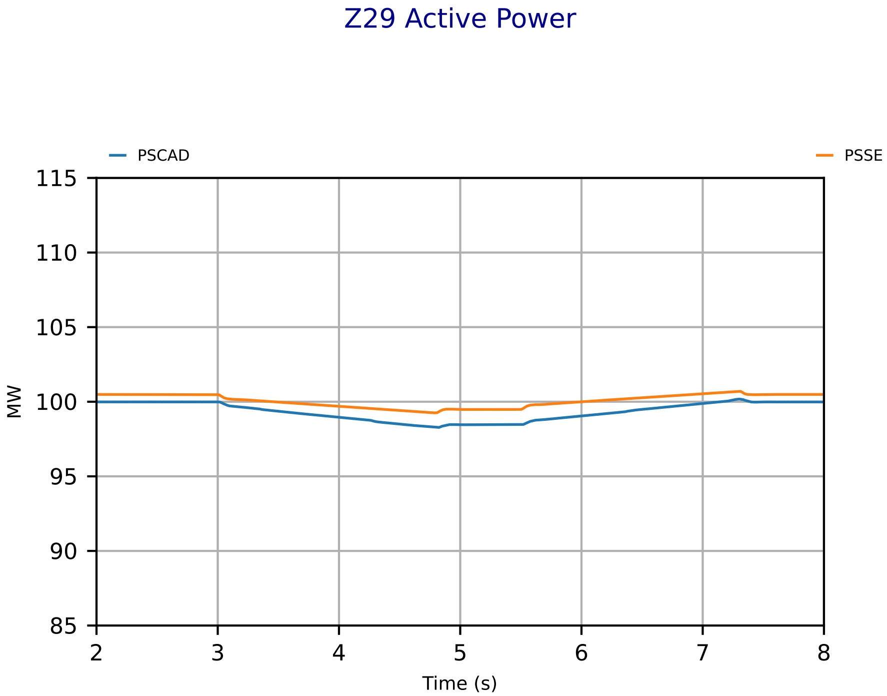


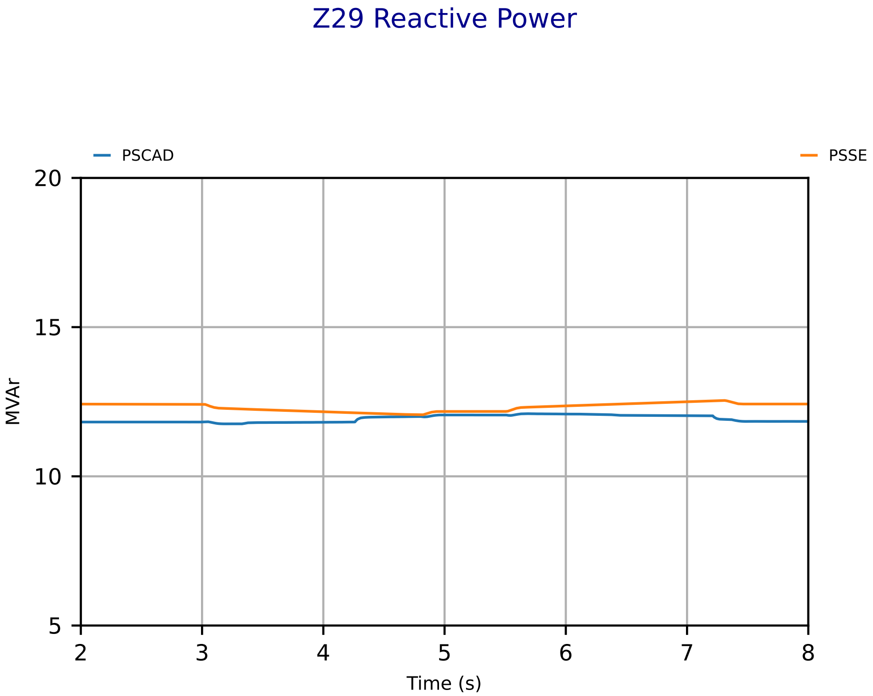


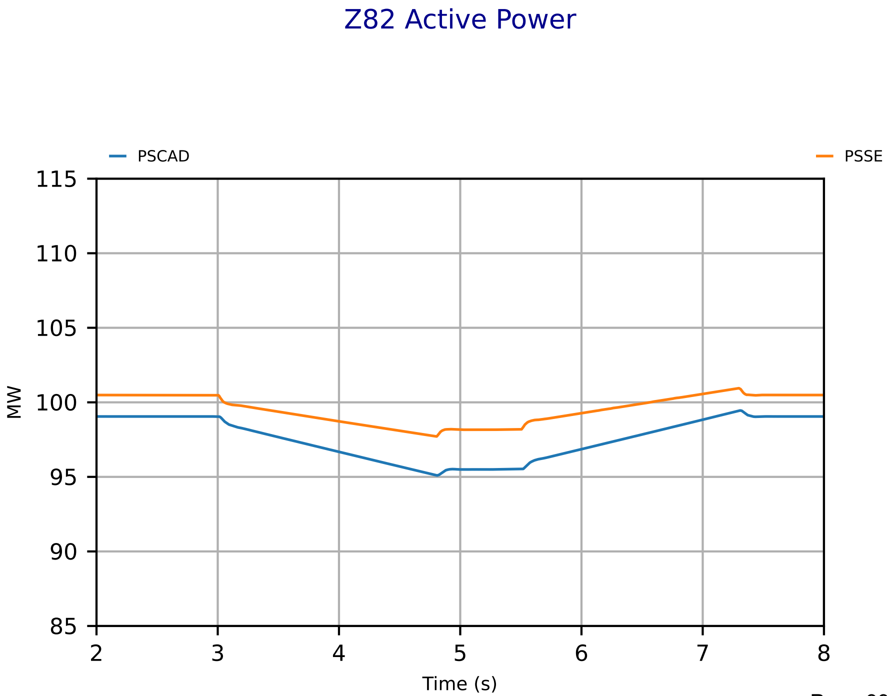


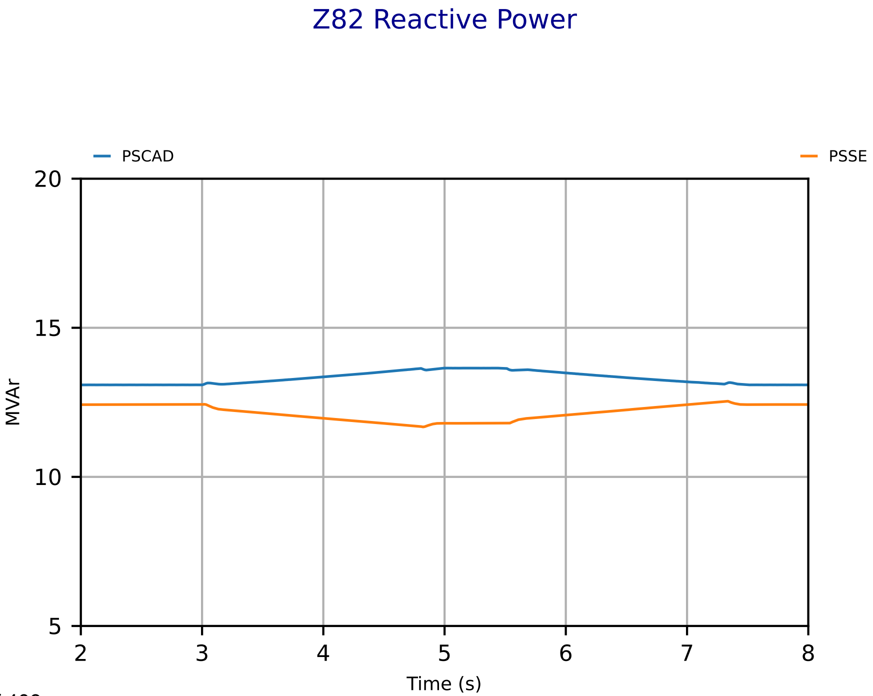


CMLD_SMIB_SCR_10_XR_14_T9_3

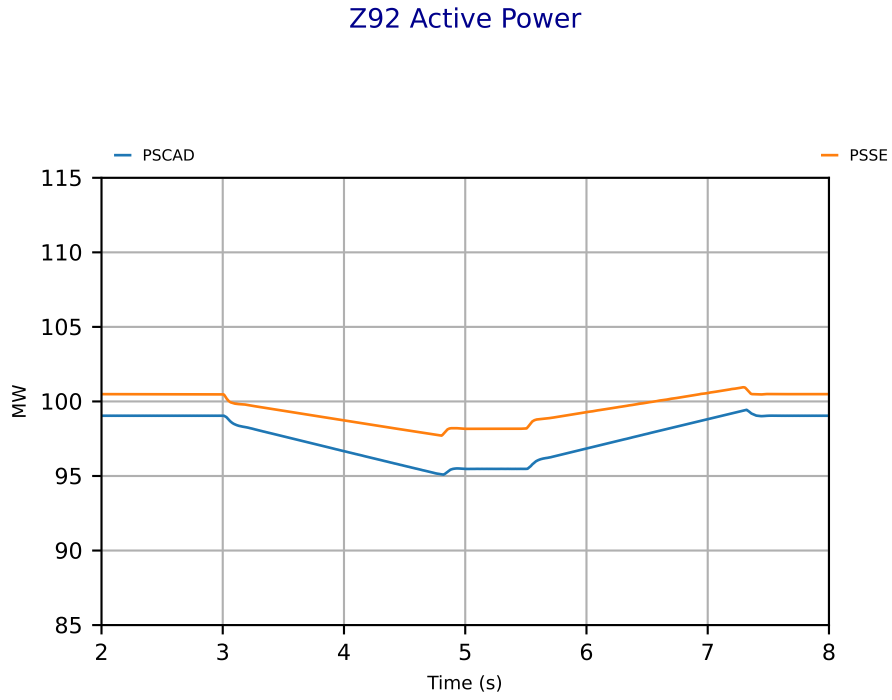


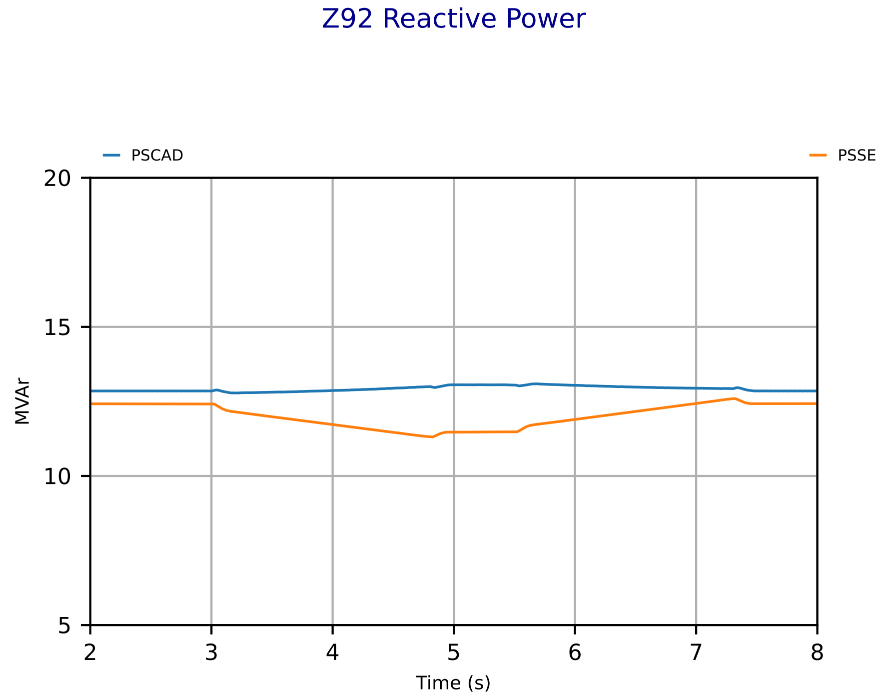


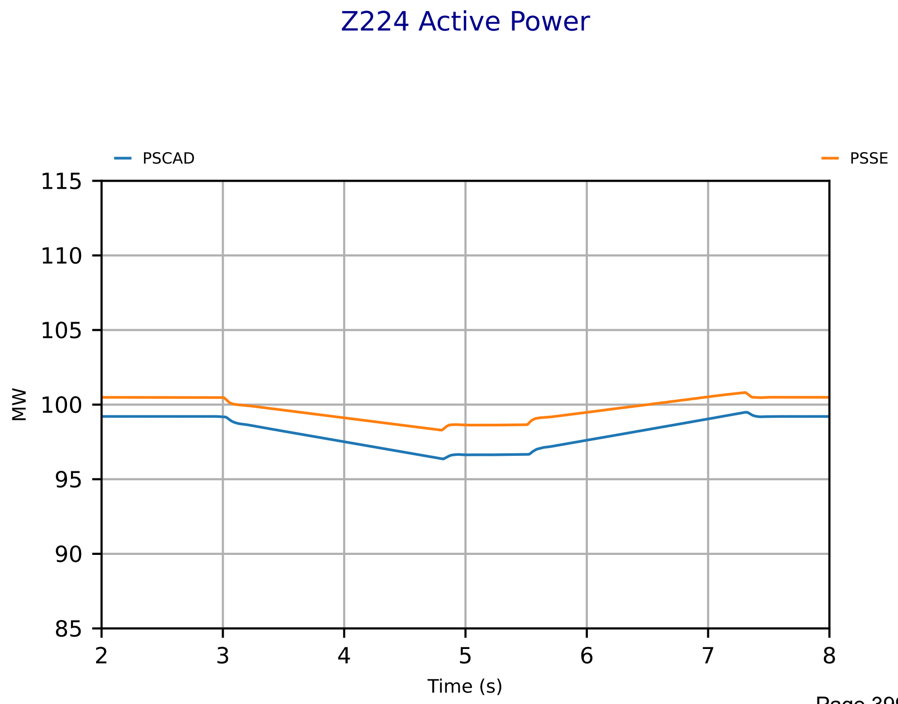


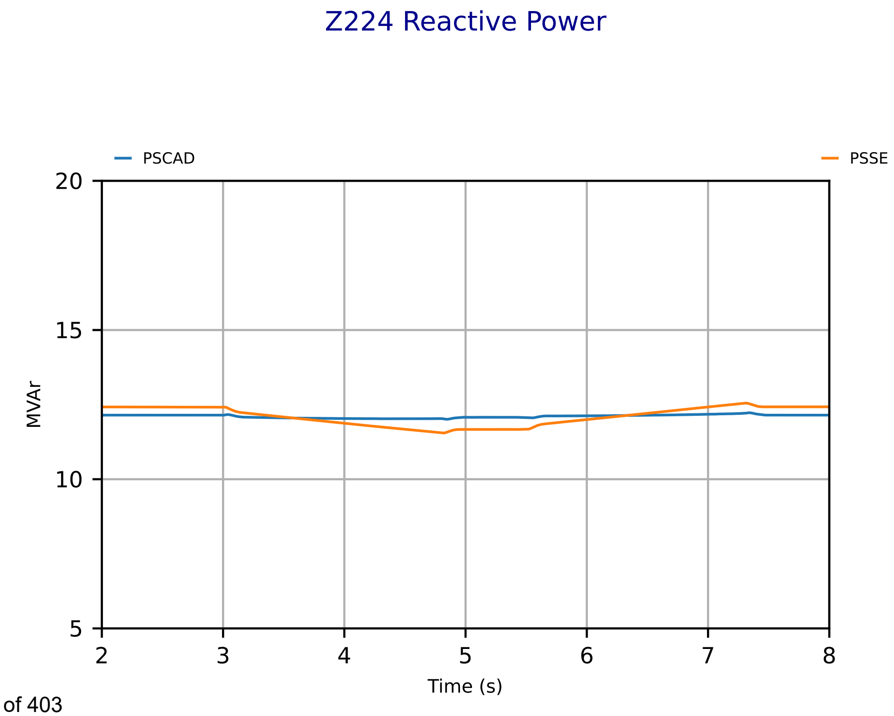


CMLD_SMIB_SCR_10_XR_14_T9_4









9 Appendix D: Discussion of PSS®E frequency spike for 3PH-G fault on DER SMIB model

The PSS®E DER model takes the bus frequency measurement from the PSS®E engine as an input. In PSS®E, the bus frequency is measured by taking the derivative of the bus voltage phase angle and applying a frequency filter time constant.

Figure 10 shows the result of a solid 3PH-G fault (Test No. 3) on the SMIB case with SCR = 3 and X/R = 3. Additional curves are included to show the impact of the frequency filter time constant (PSS®E dynamic simulation parameter) on the frequency measurement.

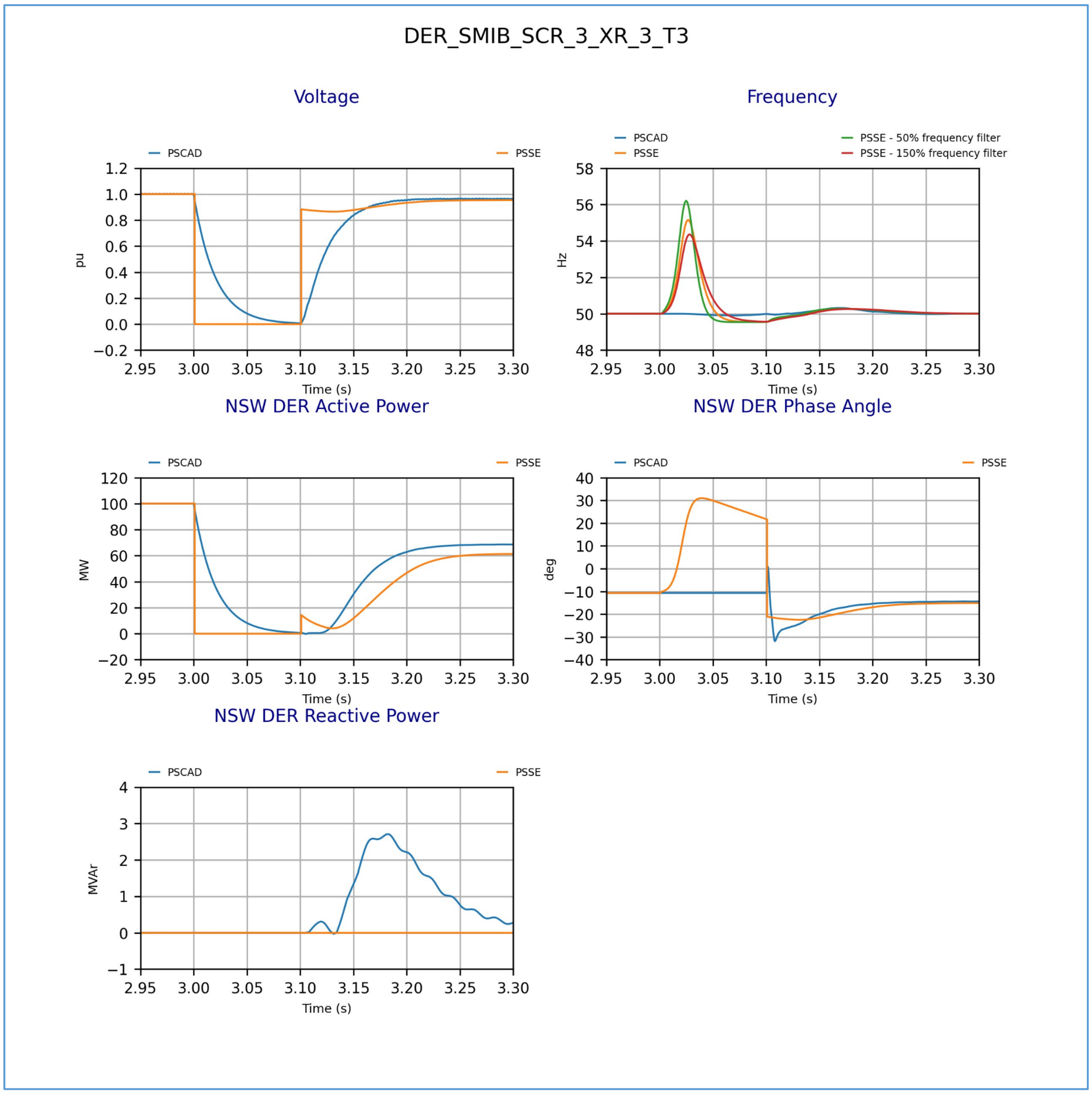


Figure 10: Result of a solid 3PH-G fault (Test No. 3) on the SMIB case with SCR = 3 and X/R = 3

As shown in Figure 10, the PSS®E bus voltage phase angle sharply increases when the fault is applied, and then jumps from +20° to -20° when the fault is cleared. The frequency measurement in PSS®E is the result of the derivative of this phase angle, which shows a large spike in frequency to about 55 Hz which leads to a decrease in the DER model active power output compared to the PSCAD™/EMTDC™ model due to the frequency droop. The PSCAD™/EMTDC™ model does not experience this spike in frequency since it uses an improved frequency measurement model.

Figure 11 shows the result of a 3PH-G fault with 5% remaining voltage on the SMIB case with SCR = 3 and X/R = 3.

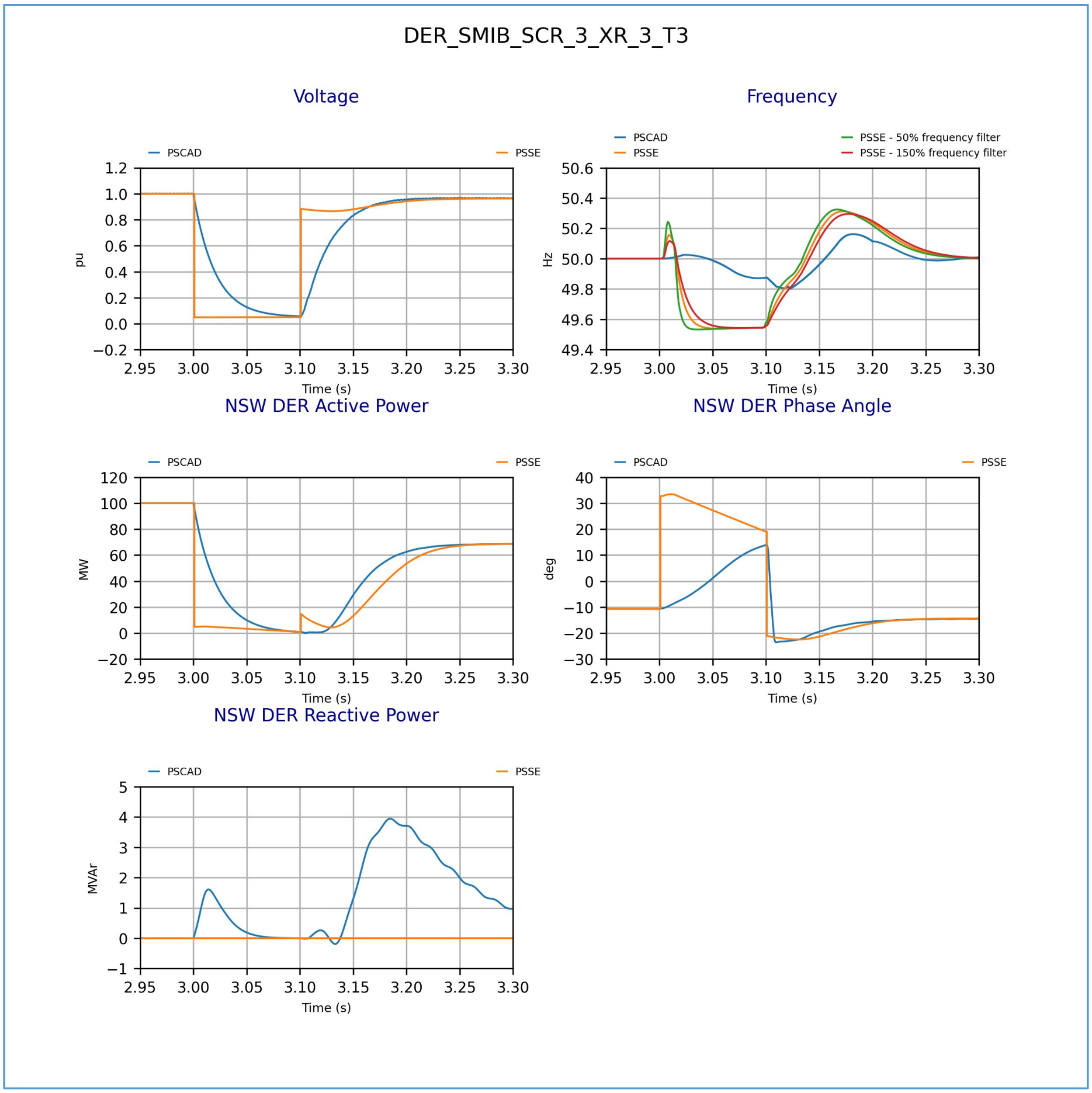


Figure 11: Result of a 3PH-G fault with 5% remaining voltage on the SMIB case with SCR = 3 and X/R = 3

Since there is a small amount of remaining voltage, the frequency measurement in PSS®E does not show a large spike, leading to a better match in active power response between PSS®E and PSCAD™/EMTDC™ models.

10 Appendix E: CMLD Model Updates

The CMLD model in PSCAD™/EMTDC™ was updated in order to improve the initialization of the cases and match the behavior of the CMLD models in PSS®E. The update to the CMLD model is shown in Figure 12.

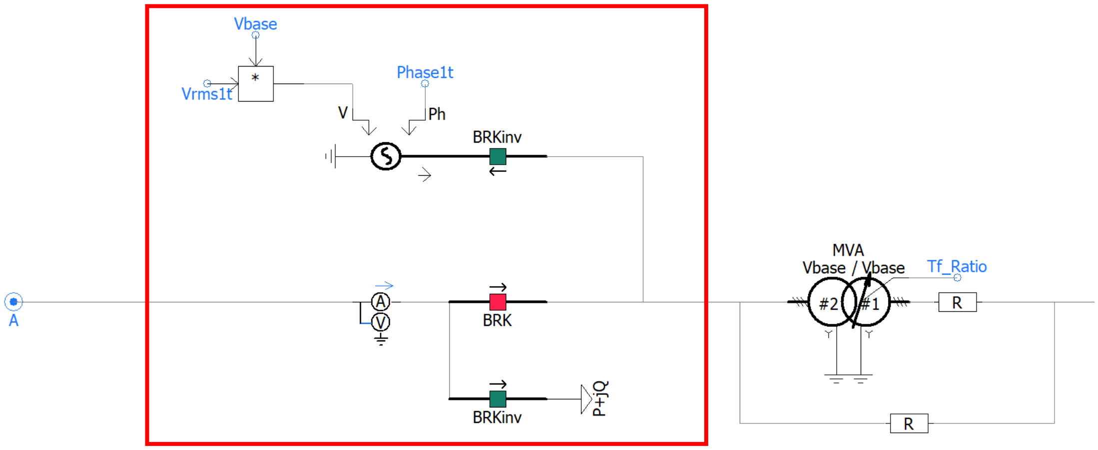


Figure 12: Updates to the CMLD model (shown in red box)

As shown in Figure 12, a series of breakers have been added to either connect the CMLD model to the network (node ‘A’) or connect the CMLD model to an infinite source and a fixed load to the network. The inputs to the source are the voltage magnitude and phase measured by the multimeter on the network side, and the fixed load P and Q are the expected total P and Q from the CMLD model.

At initialization, the CMLD was connected to the infinite source and the fixed load was connected to the network. This was done so that the network can initialize without interactions from the CMLD model.

The new breaker logic uses the existing parameter “T_init” (Time for the load terminal voltage to reach a value close to the steady state voltage) and three new timing parameters that were added to the model:

1. T_init_win: Time window for three phase induction motors transition time from speed to torque control. The output of the performance models is adjusted based on the terminal voltage at this time as well.
2. T_tran_win: Threshold check measurement (V, P and Q) window before the model transition from fixed load to detailed CMLD model.
3. T_tran: Model transition should only happen after all the other dynamic devices settled after the initialization (T_tran should also be equal or greater than the sum of T_init, T_init_win and T_tran_win).

The logic for the CMLD breakers is as follows:

- After "T_init" + "T_init_win" seconds, two actions are performed:
    - A comparator checks that the voltage at the terminal (network side of the open breaker) is above a threshold (eg. 0.9 pu).
    - A comparator checks that the difference between the active and reactive power measured by the multimeter (network side) and the active and reactive power of the infinite source (CMLD side) is below a threshold.
- After "T_tran" seconds, if the two above points are true, then the breakers will disconnect the fixed load and the infinite source and connect the CMLD model to the network.

Note: this logic was adapted from the CMLD models used in PSS®E.